PRACTICAL WORK BOOK

For Academic Session 2018

INDUSTRIAL ELECTRONICS (EL-301) For T.E (EL)

Name: ______________________________

Roll Number: ______________________________

Batch: ______________________________

Department: ______________________________

Year: ______________________________

Department of Electronic Engineering
NED University of Engineering & Technology, Karachi

LABORATORY WORK BOOK

FOR THE COURSE

Industrial Electronics (EL-301)

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Reviewed By:
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Approved By:
The Board of Studies of Department of Electronic Engineering

Introduction

This work book provides comprehensive hands on knowledge on Industrial Electronics which is dealing with sensing, processing and controlling of different processes involved in industry.

First portion of the workbook is targeting different kind of sensors and their use in industry. This portion comprises of first four labs which are dealing with theoretical knowledge of temperature, force and range sensors and their experimental verification.

Second portion of the workbook is introducing Siemens Programmable Logic Controller (PLC) which is internationally recognized popular industrial controller to control various processes. This portion comprises of middle five labs which are dealing with theoretical knowledge of PLC and its programming components.

Third and last portion of the workbook is dealing with realistic industrial controlling tasks and students are invited to build their own processing code for such tasks on PLC. This portion comprises of last five labs which are dealing with industrial sensors and actuators interfacing with PLC and its programming components.

By acquiring knowledge of all portions, students can get a thorough overview about sensing and control of different industrial processes.

Industrial Electronics Laboratory

CONTENTS

S. No.	Dated	Psycho motor Level	CLO	List of Experiments	Signature
1		**P3**	**3**	To determine characteristics of RTD (Resistive Temperature Detector) temperature sensor	
2		**P3**	**3**	To determine characteristics of NTC & PTC Thermistor. To determine the characteristic of thermocouple.	
3		**P3**	**3**	To analyze and verify the principle of Piezo resistive force transducers	
4		**P3**	**3**	To verify the principle of Ultrasonic sensors and its application as range sensor	
5		**P3**	**4**	To implement two and three input logic gates in Siemens Simatic Step 7 software	
6		**P3**	**4**	To implement two and three input logic gates in Siemens S7-300 PLC	
7		**P3**	**4**	To design and implement the operation and application of SR and RS Flip Flops in Siemens S7-300 PLC	
8		**P3**	**4**	To design and implement the operation and application of various timers in Siemens S7-300 PLC	
9		**P3**	**4**	To design and analyze the operation and application of various counters in Siemens S7-300 PLC	
10		**P3**	**4**	To develop PLC Ladder Logic Diagram for controlling operation of an overhead tank	
11		**P3**	**4**	To develop PLC Ladder Logic Diagram for controlling operation of a conveyer belt	
12		**P3**	**4**	To develop PLC Ladder Logic Diagram for controlling operation of an industrial tank unit	
13		**P3**	**4**	To develop PLC Ladder Logic Diagram to interface and to control industrial actuator (AC/DC motors)	
14		**P3**	**4**	To develop PLC Ladder Logic Diagram to interface and to control industrial actuator (valves/pumps)	

LAB SESSION 01

To determine characteristics of RTD (Resistive Temperature Detector) temperature sensor

Student Name: ______________________________
Roll no.:________________ Batch: _____________
Semester: _____________ Year: _______________

Total Marks	Marks Obtained

Remarks (if any):_______________________________

Instructor Name: _______________________________

Instructor Signature: _____________ Date: ________

Lab. No.1

Objective:

- To determine characteristics of RTD (Resistive Temperature Detector) temperature sensor.

Equipmentrequired:

- Base unit for the IPES system.
- Experiment module MCM14/EV.
- Digital multimeters, breadboards/Vero board
- Power supply Mod. PSUIEV (+12V & -12V)

Theory:

RTD

To measure the temperature, RTD exploits the “Resistance Variation” of an electrical conductor, at variation of the same temperature.
The relation between resistance and temperature is approximately the following:

$$\mathbf{R_T = Ro \times (1 + \alpha\Delta T)}$$

Ro = resistance at 0° Celsius= 100Ω

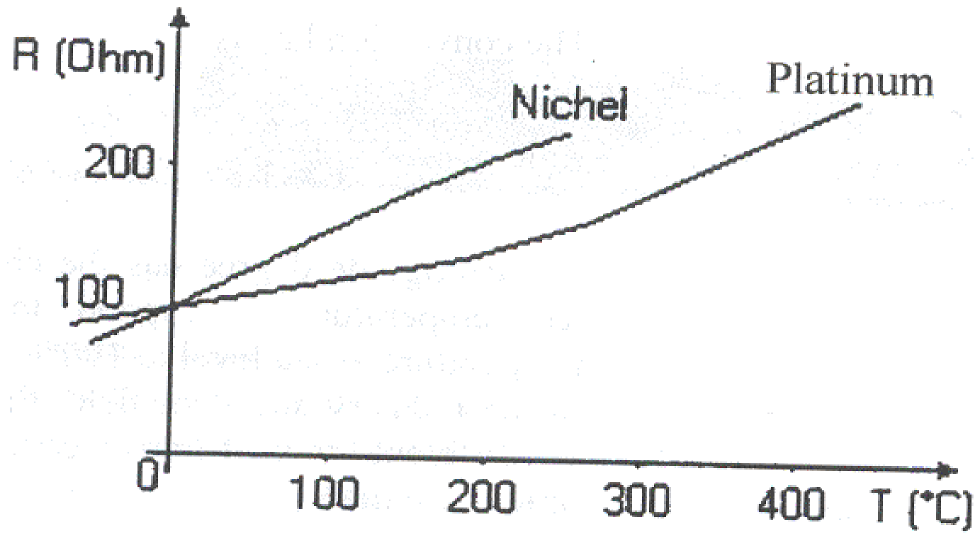
Where the temperature coefficient **α** is given its average value in the measurement field.
The RTD has the following main characteristics:

- Constance of the characteristics in time.
- Characteristics repeatability.
- Good variation of the resistance as function of temperature.

Two kinds of RTD’s have been standardized:

- Nickel
- Platinum.

A platinum RTD is mounted in the module.
The platinum RTD has a coefficient of temperature **α**= 3.85 x 10-3 $^{o}C^{-1}$.
The characteristic curves of these two RTD’s are shown in figure



Normally used RTD's have a resistance of 100 **Ω** at0°C and a tolerance of (+/-0.1)°C. They usually consist of a wire of the above materials wounded around a cylindrical insulating material or a plate resistant to high temperatures (ceramic, glass).
For their constitution, as they have a very high thermal constant, they are relatively slow in following the process temperature variations.

Heating source

The heat necessary to the tests on the temperature transducers is provided by two resistors in parallel. Two resistors heat the aluminum plate on which the transducers are inserted. The temperature range goes from ambient temperature to about 110°C.

Range of RTD:

RTD has a resistance of 100 Ω at 0°C and The RTD has a resistance of 138.5 Ω at 100°C. After calibration, voltage changes between 0V and 1 V from 0°C to 100°C. The Coefficient of 10 m V /°C enables a direct temperature reading: e.g.450 mV correspond to 45°C.

<u>Procedure:</u>

RTD signal conditioner settings:

The RTD has a resistance of 100 Ω at 0°C and of 138.5 Ω at100°C.These resistance values are the two calibration points of the conditioner with two sample resistors to be inserted into the proper jumpers.

1. Disconnect all jumpers of the "TEMPERATURE RANSDUCERS" circuit.
2. Connect jumper J3.

3. With J4 connect the 100-Ω resistance and with Potentiometer **RVI** adjust voltage so to obtain OV on point 7(OUT).
4. Disconnect jumper J4, with jumper J5 connect the 138.5-Ω resistance, and with potentiometer **RV2** adjust the voltage so to obtain 1 V of full scale on point7 (OUT)
5. Disconnect jumper J5.
6. Connect jumper J2 to connect the RTD (keep jumper J3 inserted).
7. Activate the heating element with the I1/HEATER switch.
8. Measure the voltage and then the temperature between OUT (7) and ground.
9. Draw the graph

Observation:

Corresponding Temperature	Output Signal (mV)	RTD resistance measured (Ω)	Resistance $R_T=R_O(1+\alpha T)$
30			
35			
40			
45			
50			
55			
60			
65			
70			
75			

InterfacingRTDwithself-designedcircuit:

Interface RTD with your own circuit on breadboard/Vero board. Provide circuit diagram below and fill out observation table:

Corresponding Temperature	Output Signal (V) ($0 \leq V_o \leq 5$)	RTD resistance measured (Ω)	Resistance $R_T = R_O(1+\alpha T)$
30			
35			
40			
45			
50			
55			
60			
65			
70			
75			

Result:

RTD's temperature versus resistance graph indicates good variation of resistance as the function of temperature.

LAB SESSION 02

To determine characteristics of NTC & PTC Thermistor. To determine the characteristic of thermocouple.

Student Name: ______________________________

Roll no.:________________ Batch: _____________

Semester: _____________ Year: _______________

Total Marks	Marks Obtained

Remarks (if any):_______________________________

Instructor Name: _______________________________

Instructor Signature: _____________ Date: ________

Lab No. 2

Objective:

To determine characteristics of NTC & PTC Thermistor. To determine the characteristic of thermocouple.

Equipmentrequired:

- Base unit for the IPES system.
- Experiment module MCM14/EV.
- Digital Multimeters, breadboards/Vero board
- Power supply Mod. PSUIEV (+/-12V).

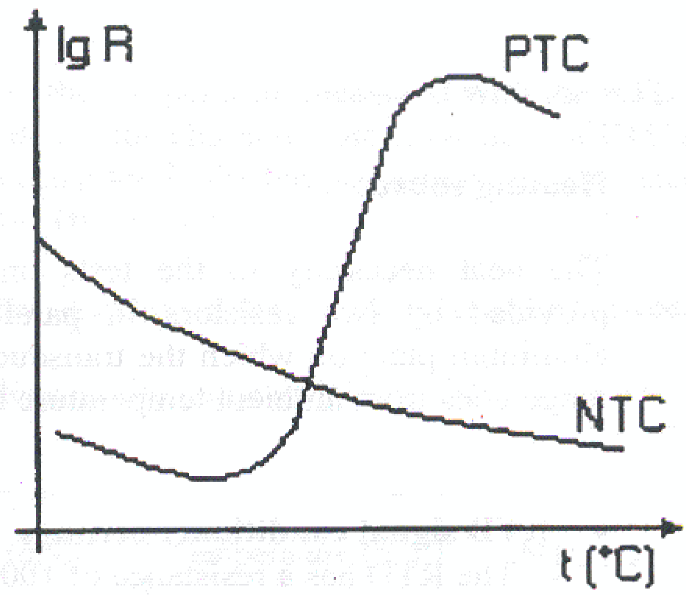
Theory:

NTCandPTCThermistor:

These semiconductor transducers exploit high sensibility of semiconductor materials toward temperature.
The coefficient of temperature is much higher than the one of RTD and is much cheaper but it has a temperature range which is narrower and with less linearity. The law for the variation of the resistance as function of Temperature, with a first approximation, is the following:

$$\mathbf{R_T = R_o \times (1 + \alpha \Delta T)}$$

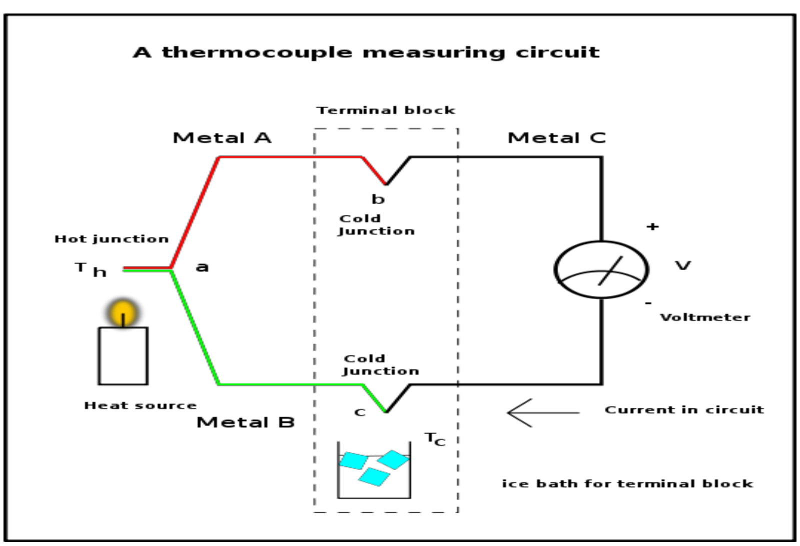
Although this formula is equal to the one found for RTD, the error in this approximation is much greater.
The transducers of semi-conductor kind analyzed with module MCM14 are **NTC** and **PTC.**
NTC (**Negative Temperature Coefficient) Thermistor** drops its resistance when the temperature increases. PTC **(Positive Temperature Coefficient)** Thermistor increases its resistance when the temperature increases. At constructive level, the difference between the two transducers is determined during the semiconductor realization.



Curves of thermistors PTC and NTC

Thermocouples:

A thermocouple consists of two dissimilar conductors in contact, which produces a voltage when heated. The voltage produced is dependent on the difference of temperature of the junction to other parts of the circuit. Thermocouples are a widely used type of temperature sensor for measurement and control and can also be used to convert a temperature gradient into electricity. Commercial thermocouples are inexpensive, interchangeable, are supplied with standard connectors, and can measure a wide range of temperatures. In contrast to most other methods of temperature measurement, thermocouples are self-powered and require no external form of excitation. The main limitation with thermocouples is accuracy; system errors of less than one degree Celsius (°C) can be difficult to achieve.



Procedure:

RTD signal conditioner settings:

RTD has a resistance of 100 **Ω** at 0^0C and of 138.5 **Ω** at100°C.These resistance values are the two calibration points of the conditioner with two sample resistors to be inserted into the proper jumpers.

1. Disconnect all jumpers of the "TEMPERATURE TRANSDUCERS" circuit.
2. Connect jumper J3.
3. With J4 connect the 100-Ω resistance and with the potentiometer **RVI** adjust the voltage so to obtain OV on point 7(OUT).
4. Disconnect jumper J4, with jumper J5 connect the 138.5-Ω resistance, with the Potentiometer **RV2** adjust the voltage so to obtain 1 V of full scale on point 7 (OUT).
5. Measure the voltage and then the temperature between OUT (7) and ground.
6. Disconnect jumper J5.
7. Connect jumper J2 to connect the RTD (keep jumper J3 inserted).
8. Activate the heating element with the I1/HEATER switch.
9. Measure the voltage and then the temperature between OUT (7) and ground.
10. Use the temperature measured with the RTD as sample variable to detect the characteristic resistance of PTC and NTC Thermistor, in the temperature range.
11. Measure the value of NTC resistance between terminals 1-2.
12. Measure the value of PTC resistance between terminals 3-4.

Observation:

RTD (mV)	Temperature (^{o}C) T	NTC R2(Ω)	PTC R1(Ω)	Log R1	Log R2

InterfacingThermistorwithself-designedcircuit:

Interface Thermistor with your own circuit on breadboard/Vero board. Provide circuit diagram below and fill out observation table:

Corresponding Temperature	Output Signal (V) $(0 \leq Vo \leq 5)$	Thermistor resistance measured (Ω)	Resistance $R_T = R_O(1+\alpha T)$
30			
35			
40			
45			
50			
55			
60			
65			
70			
75			

<u>Interfacingthermocouplewithself-designedcircuit:</u>

Interface thermocouple with your own circuit on breadboard/Vero board. Provide circuit diagram below and fill out observation table:

Corresponding Temperature (^{O}C)	Output Signal (V) ($0 \leq Vo \leq 5$)	Thermocouple output (mV)
30		
35		
40		
45		
50		
55		
60		
65		
70		
75		

Results:

The characteristic curves of NTC and PTC Thermistor are successfully studied and Verified through graphs

The characteristics of thermocouples are studied and verified

LAB SESSION 03

To analyze and verify the principle of Piezoresistive force transducers

Student Name: ______________________________
Roll no.:________________ Batch: _____________
Semester: _____________ Year: _______________

Total Marks	Marks Obtained

Remarks (if any):_______________________________

Instructor Name: _______________________________

Instructor Signature: _____________ Date: ________

Lab. No. 3

Objective:

- To analyze and verify the principle of Piezoresistive force transducers
- Characteristic parameters
- Calibration of the conditioner
- Experimental tests

Equipmentrequired:

- Basic unit for IPES system, module holder frame Mod.MUIEV,
- Individual control unit mod. SIS3.
- Power supply Mod.PSUIEV.
- Experiment module mod. MCMl4IEV
- Digital Multimeter, breadboards/Vero board

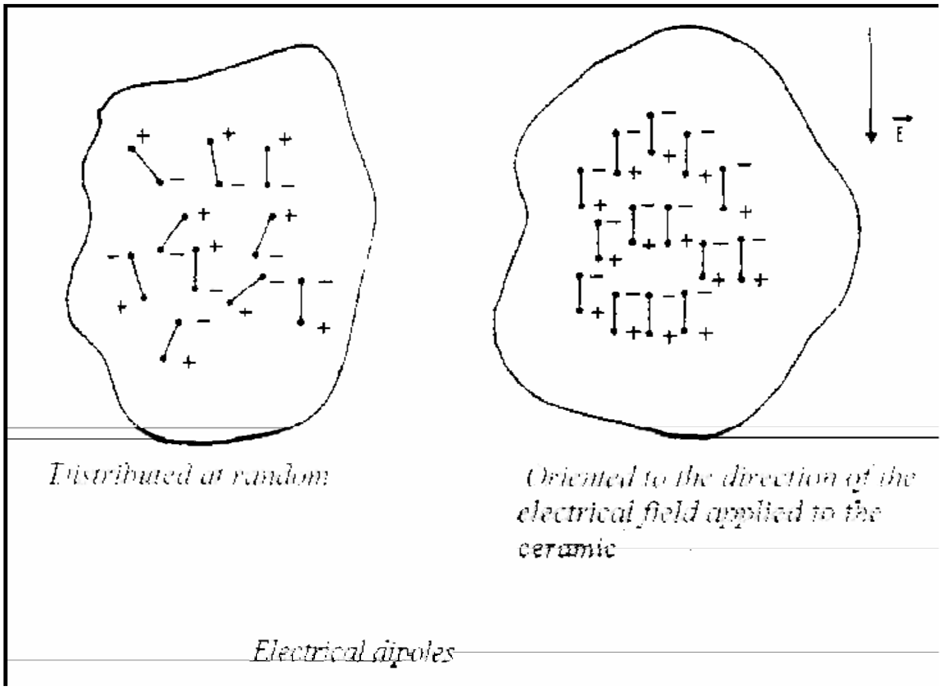
Theory:

Piezoelectricity:

Many electromechanical transducers use piezoelectric ceramics which can change their geometrical dimensions as function of the electrical field applied to them.
Inversely, these piezoelectric ceramics can be a source of electrical signal if under mechanical stresses. This propriety is used in force transducers as the one in module MCMl4/EV.

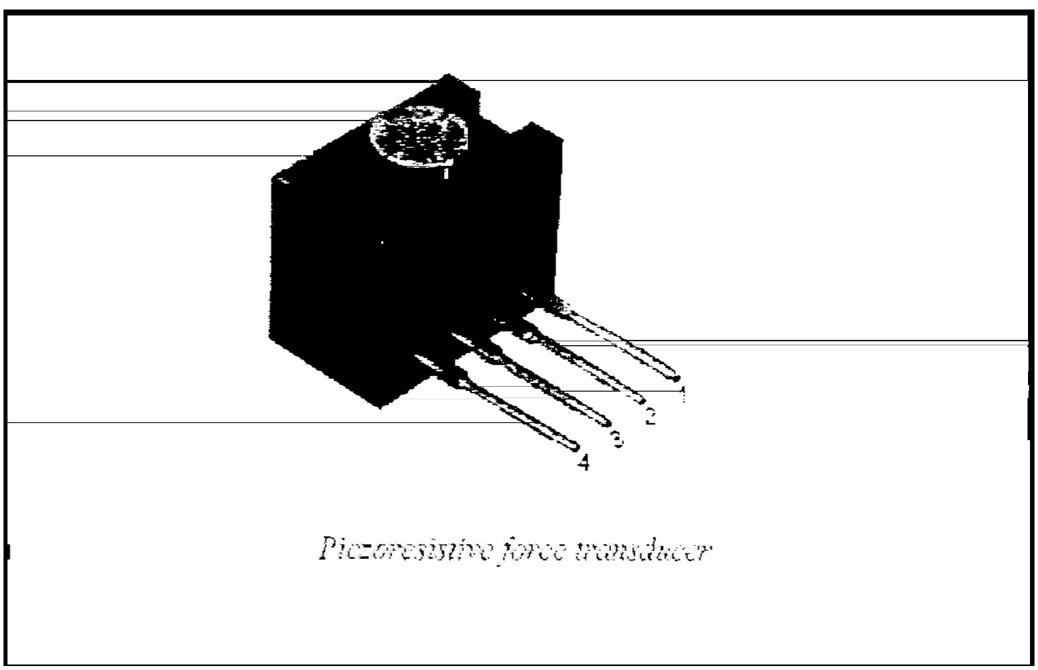
The ceramic piece cut in the shape of a disk, has an inner structure composed by electrical dipoles at random and results in the electrically neutral unit.
Applying an intense electrical field to the ceramic disk (high temperature), the electrical dipoles set preferentially in the direction of the electrical field.
Making the temperature and the electrical field drop, the dipoles keep their preferential orientation and the totally neutral electrical state. The ceramic becomes permanently Piezoelectric.

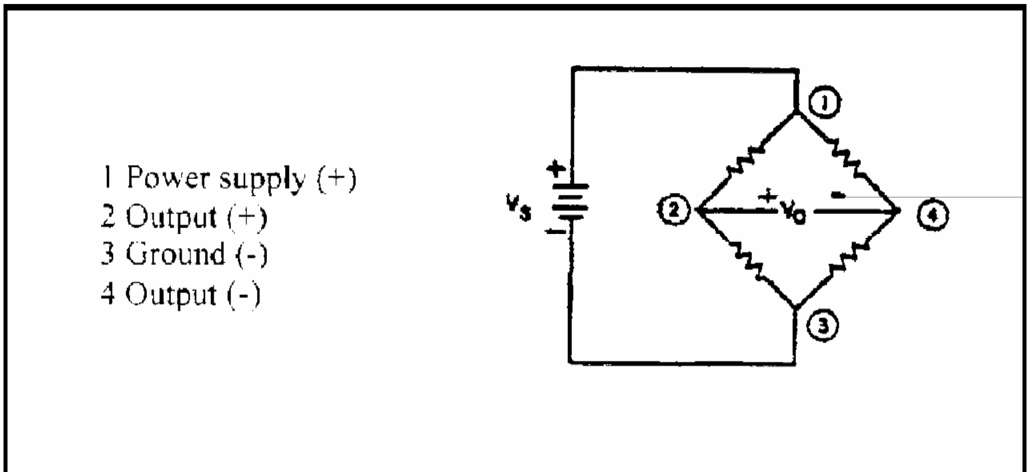
Metal contacts are deposited on the surfaces of the ceramic transducer disk in order to apply and measure signals.
For this kind ceramic-piezoelectric transducer, a mechanical stress deforming the surface causes a loads shift, causing a measurable electrical voltage.



Characteristicparameters:

The force sensor set in the module MCM14/EV, has the following characteristics:
The Piezoresistive sensor is inserted into a Wheatstone bridge enabling a stable output (millivolt) for a range of: <u>0 to 1500</u> grams





Electrical diagram

Procedure:

- Disconnect all jumpers.
- Turn all switches OFF.

Calibrationoftheforcesensorconditioner

1. The reference voltage of the sensor is about + 10V dc, to be measured on the pins of the regulation diode.
2. The amplifier IC3 carries out an impedance matching.
3. The amplifier IC4 fixes the output variation range OUT (9).
4. The potentiometer RV3 is used to calibrate the 0 V= 0 gr.
5. The potentiometer RV 4 is used to calibrate the full scale 250m V = 250 gr (with sample weight)
6. The coefficient of the conditioner is 1 mV/gr.

- Set the weight supplied with the module on the weighting support and measure the value across the output OUT(9).
- Center the load on the measurement support.
- Check the measured weight corresponds to 250 mV, on the contrary proceed with the calibration.

Fault:

1. The voltage at the Terminal 9 is change.
2. The voltage at the Terminal 9 is zero.

Observation:

The sensibility of the sensor is 0.24mV/g.
The voltage at the Terminal 9 was changed because the regulation diode is faulty.
The voltage at the Terminal 9 was zero because IC 4 input is short-circuited to the ground.

Interfacingcommerciallyavailablesensorwithself-designedcircuit:

Interface commercially available force/load sensor with your own circuit on breadboard or Vero board. Provide circuit diagram below and fill out observation table:

Load (g)	Output Signal (mV)	Measured error (g)

Result:

- The principle of the Piezoresistive Force transducer is successfully studied and its characteristic parameters are experimentally verified.

LAB SESSION 04

To verify the principle of Ultrasonic sensors and its application as range sensor

Student Name: ______________________________

Roll no.:________________ Batch: _____________

Semester: _____________ Year: _______________

Total Marks	Marks Obtained

Remarks (if any):_______________________________

Instructor Name: _______________________________

Instructor Signature: _____________ Date: ________

Lab No. 4

Objective:

- To verify the principle of Ultrasonic sensors and its application as range sensor.
- Characteristics of the ultrasonic emitter and the receiver.
- Experimental analysis of the signals.

Equipmentrequired:

- Base unit for the IPES system.
- Individual control unit mod. SIS3.
- Experiment module MCM14/EV.
- Digital multimeter, breadboard/Vero board
- Power supply MOD.PSUIEV.

Theory:

CharacteristicsoftheUltrasonicComponents:

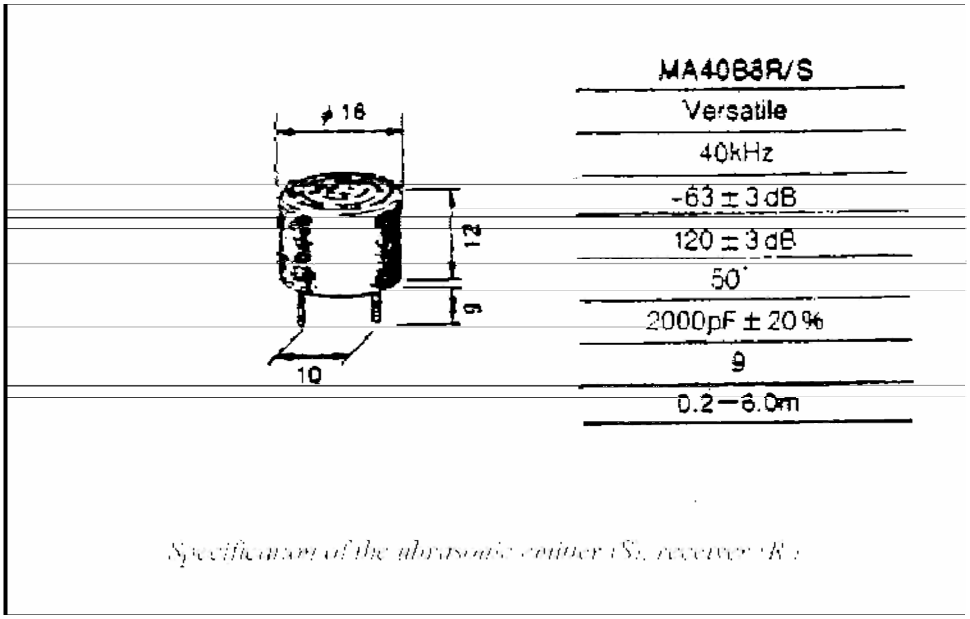
- These components are made with ceramic piezoelectric materials (piezoelectricity), which can operate as generators and as ultrasonic wave's receivers, especially for measuring the systems or for alarm systems.

- The ultrasonic vibrations **(>20 KHz)** sent by the transmitter, controlled by an oscillator, propagate in axial mode.

- Across the receiver you can detect a voltage which amplitude depends on the intensity of the waves radiated by the transmitter. The received voltage signal amplitude ranges between 10^{-6} V and 0.1 V.

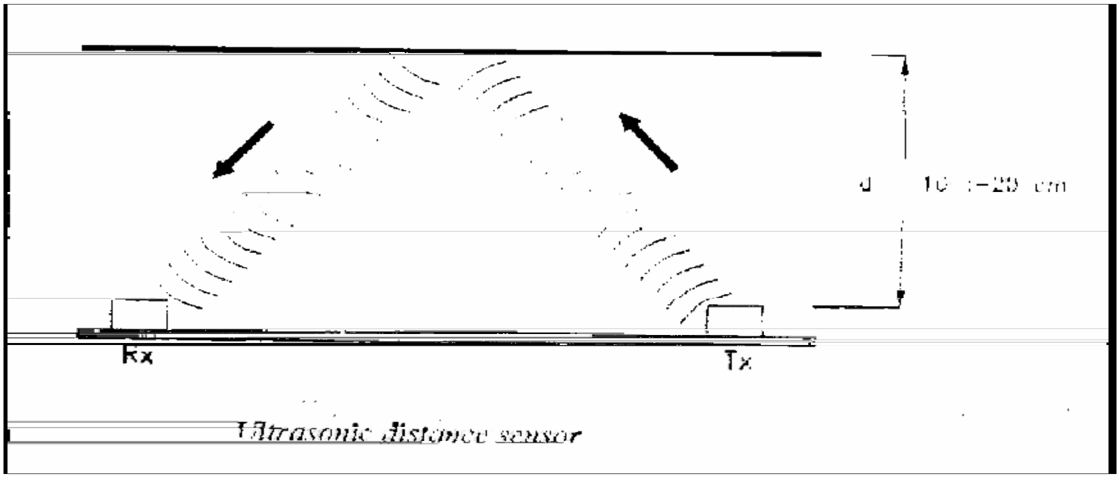
- A short ultrasonic pulse is transmitted by a transducer, and it is received by another after a time $T = L/v$, where v is the sound speed (in the air = 334 m/s) which is supposed to be constant at variation of the distance L between the two transducers, it is easy to calculate L measuring the transit time T.

- In Module MCM 14/EV an ultrasonic emitter (TX) and receiver (RX) are used.



Procedure:

1. Disconnect all the jumpers.
2. Turn all switches OFF.
3. Turn on the power supply.
4. With the oscilloscope measure the signal on the base of T1.
5. With the oscilloscope, measure the control frequency of the transmitter (TX) on the resistor R31.
6. Vary the frequency and note the amplitude of the signal at transmitter at different frequencies.
7. Set jumper J7 to connect the buzzer.
8. Set your hand or a sheet of paper over the transmitter and the receiver so to point out the ultrasonic wave reception.
9. Determine the reception pulse at different frequencies by connecting the oscilloscope at the base of the transistor T2 and also determine the time of reception.



Observation:

The frequency of the Transmitter (TX) is found to be__________KHz.
The time of transmission = T= _____μs.
The distance between the transmitter and receiver is L = V*T = ______m.
V = velocity of sound in air = 334m/s.
T = time between transmission and reception.

Sr.No	Frequency (KHz)	Amplitude (V)
1		
2		
3		

Interfacingcommerciallyavailablesensorwithself-designedcircuit:

Interface commercially available ultrasonic sensor with your own circuit on breadboard or Vero board. Provide circuit diagram below and fill out observation table:

Actual Range (cm)	Output Signal (mV)	Measured error (cm)

Result:

- The principle of the Ultrasonic Sensors is successfully studied and the characteristic of ultrasonic emitter and the receiver is verified through experiments.

LAB SESSION 05

To implement two and three input logic gates in Siemens Simatic Step 7 software.

Student Name: ______________________________
Roll no.:________________ Batch: _____________
Semester: _____________ Year: _______________

Total Marks	Marks Obtained

Remarks (if any):_______________________________

Instructor Name: _______________________________

Instructor Signature: _____________ Date: ________

Lab No. 5

Objective:

To implement two and three input logic gates in Siemens Simatic Step 7 software.

LearningOutcomes:

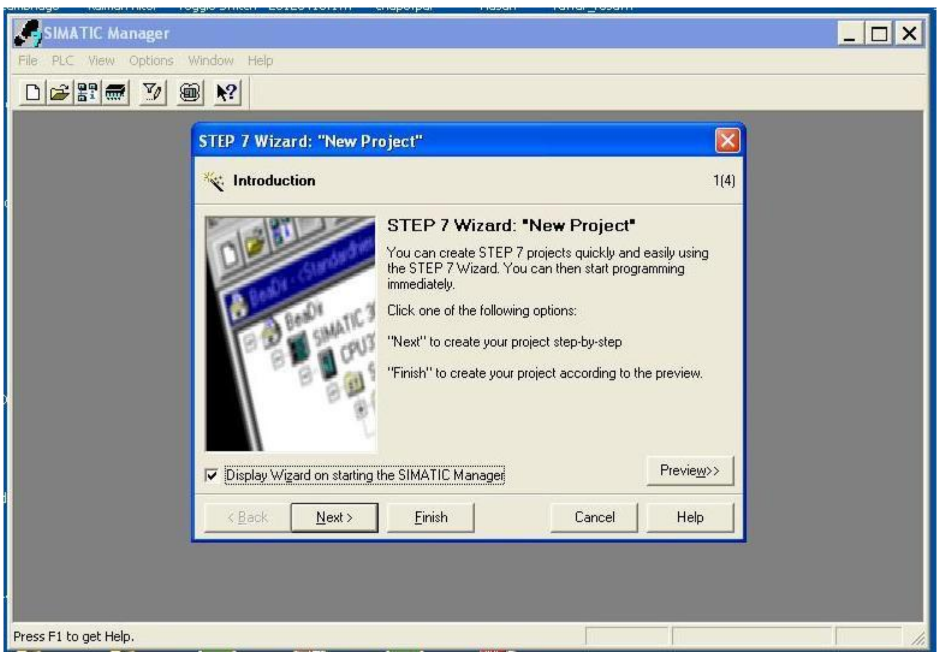
To implement the operation of logic gates in Siemens Simatic Step 7

Introduction:

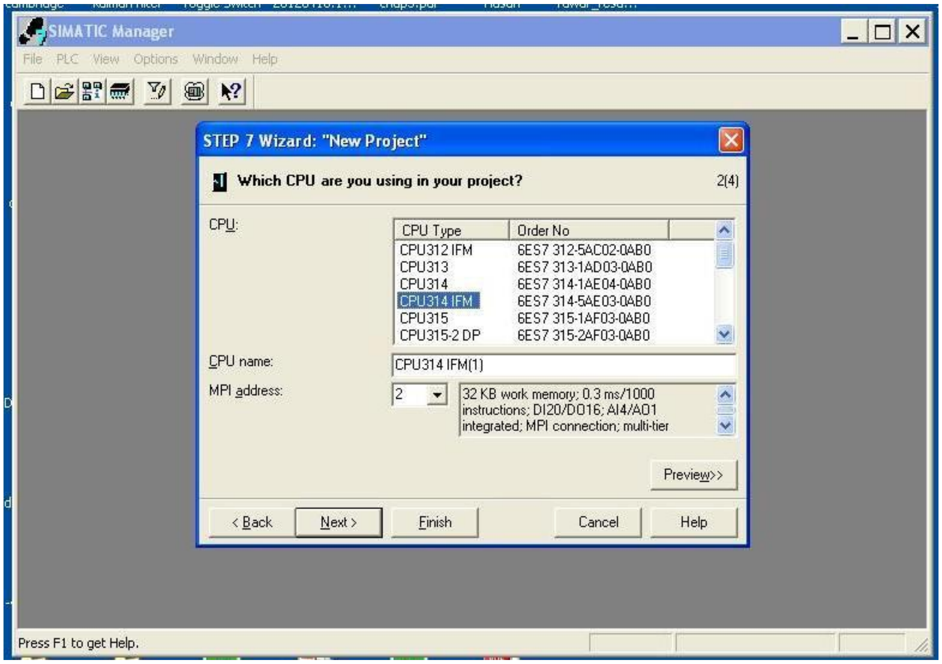
Simatic is a controller plus software developed by a German company. In Industrial Electronics labs, S300 PLCs with Step 7 (S7) software will be utilized.

Procedure:

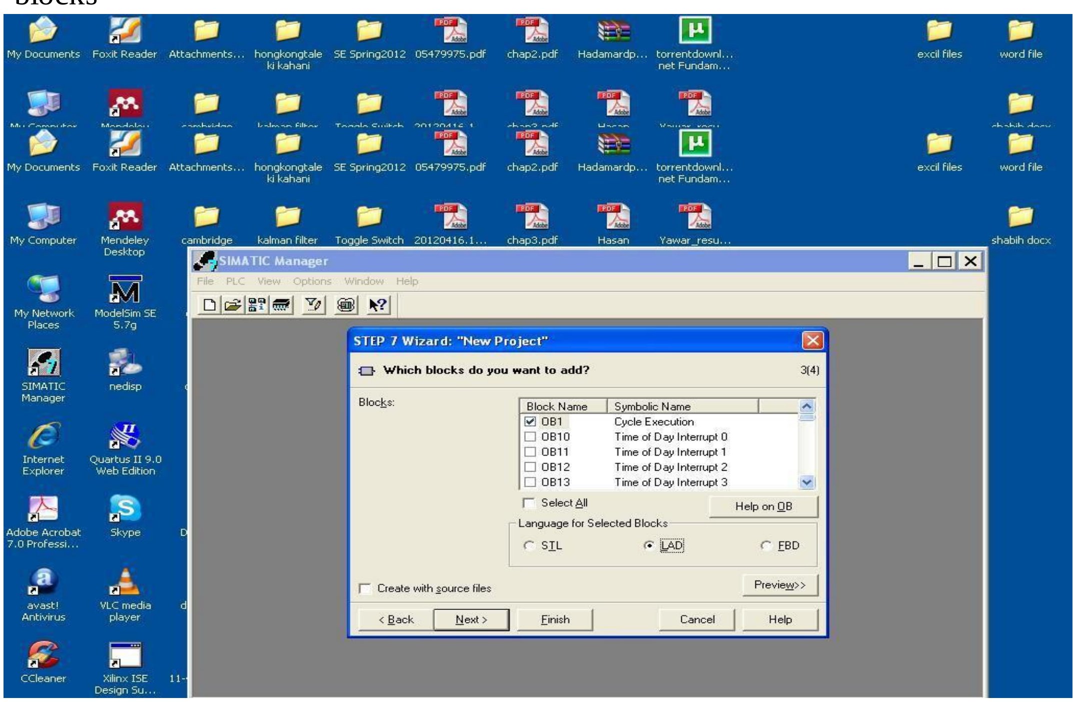
1. Double click the Simatic Manager icon once to open S7
2. Once the S7 is launched, screen similar as shown below will appear



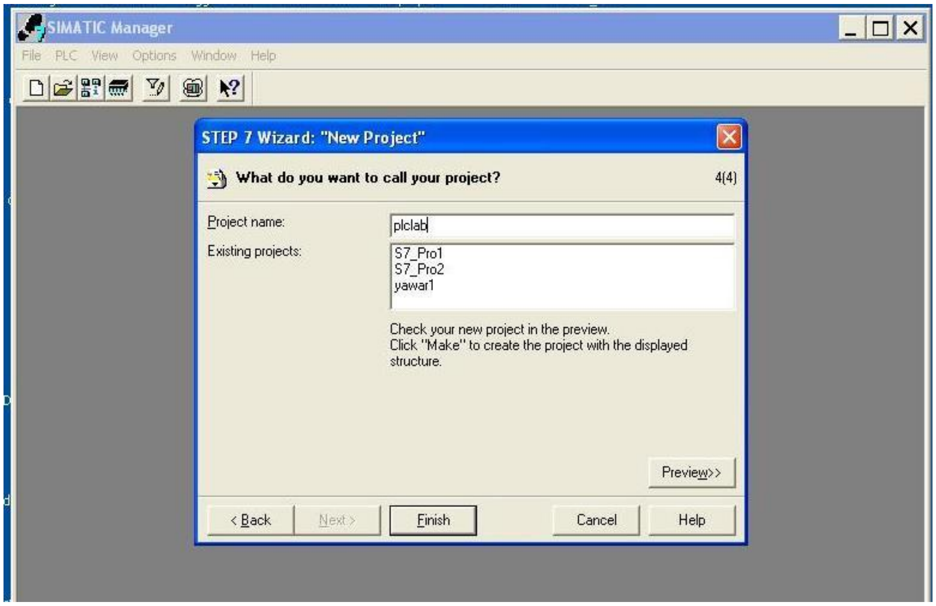
3. Click Next. Select CPU314IFM.

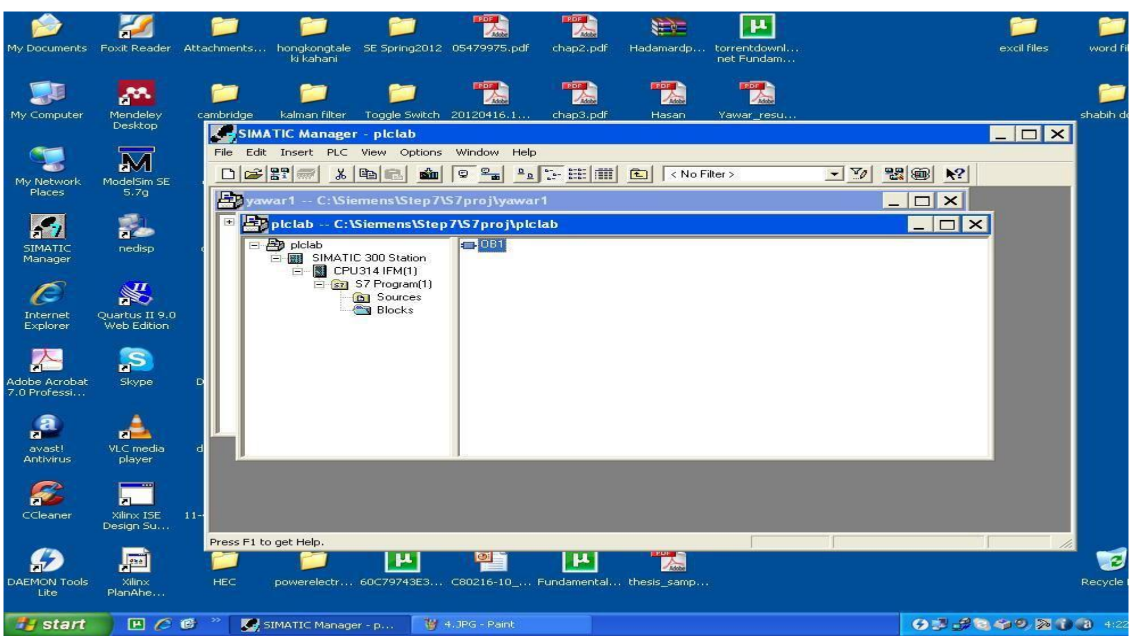


4. Click Next and select OB1 under Blocks. Select LAD as the language for selected blocks

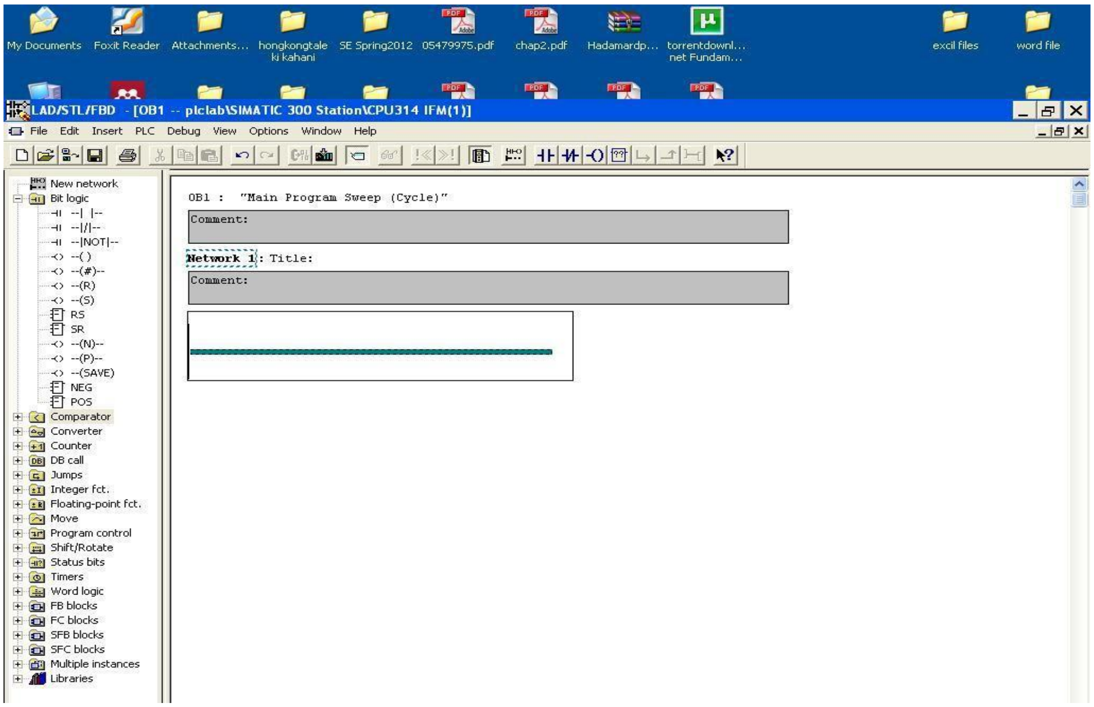


5. Click Next and name your project. Click Finish.

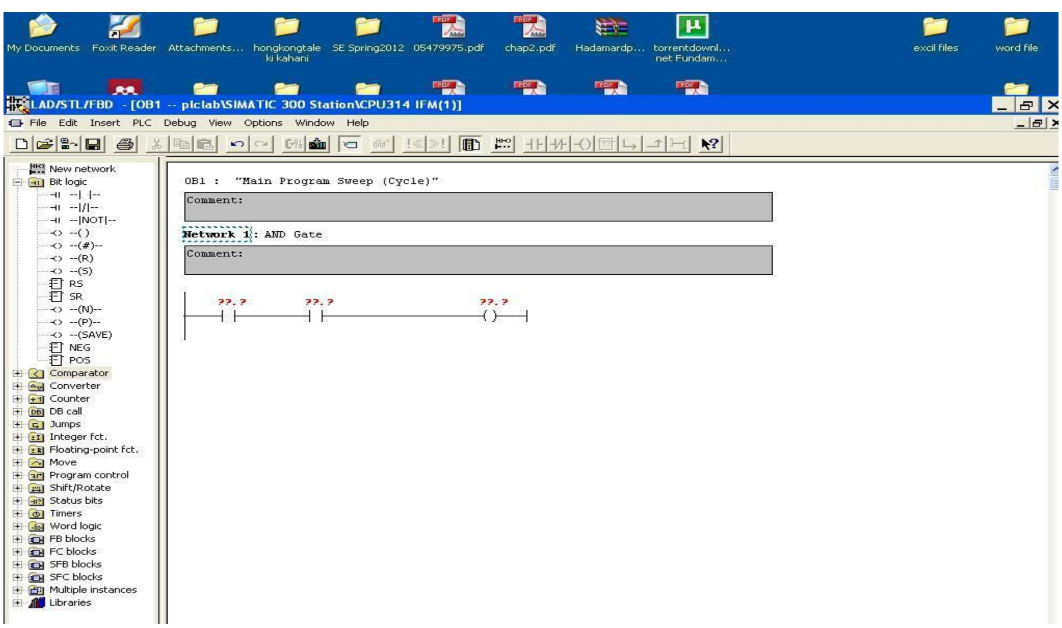




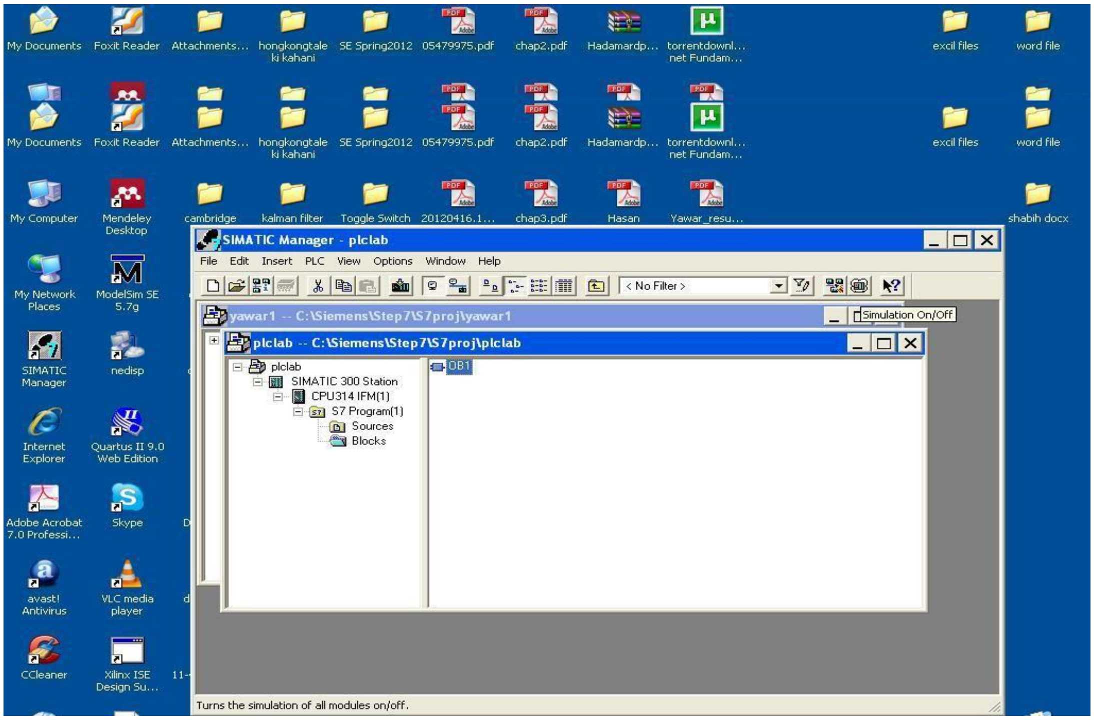
7


LAD/STL/FBD - [OB1 -- plclab\SIMATIC 300 Station\CPU314 IFM(1)]
File Edit Insert PLC Debug View Options Window Help
OB1 : "Main Program Sweep (Cycle)"
Comment:
Network 1: Title:
Comment:

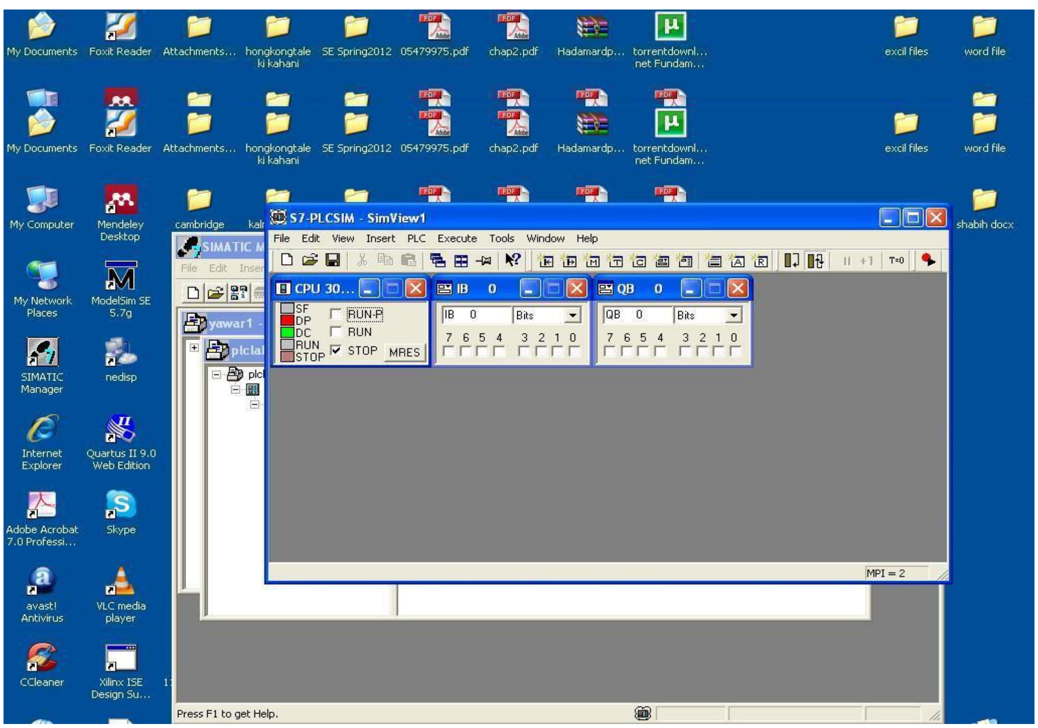
8.


LAD/STL/FBD - [OB1 -- plclab\SIMATIC 300 Station\CPU314 IFM(1)]
File Edit Insert PLC Debug View Options Window Help
OB1 : "Main Program Sweep (Cycle)"
Comment:
Network 1: AND Gate
Comment:
??.?
??.?
??.?

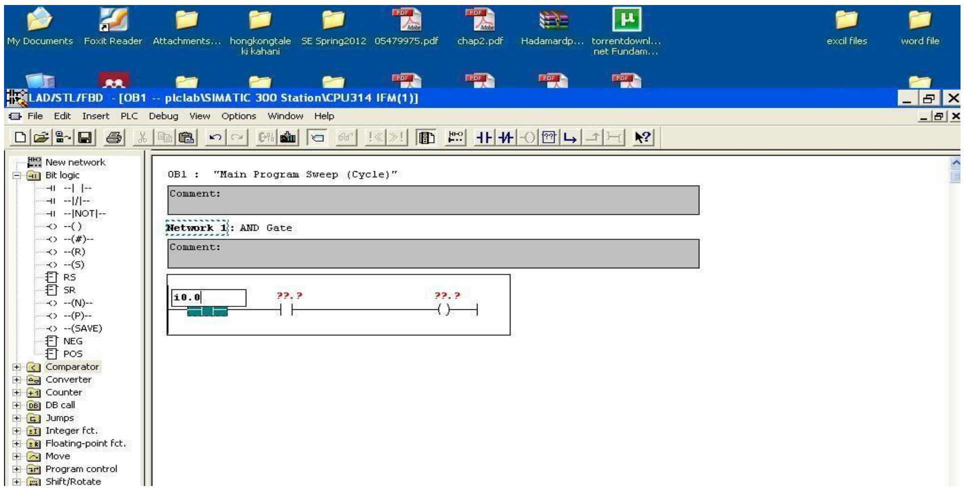
9. For Soft simulation turn Simulator ON from the Simatic manager window as follows



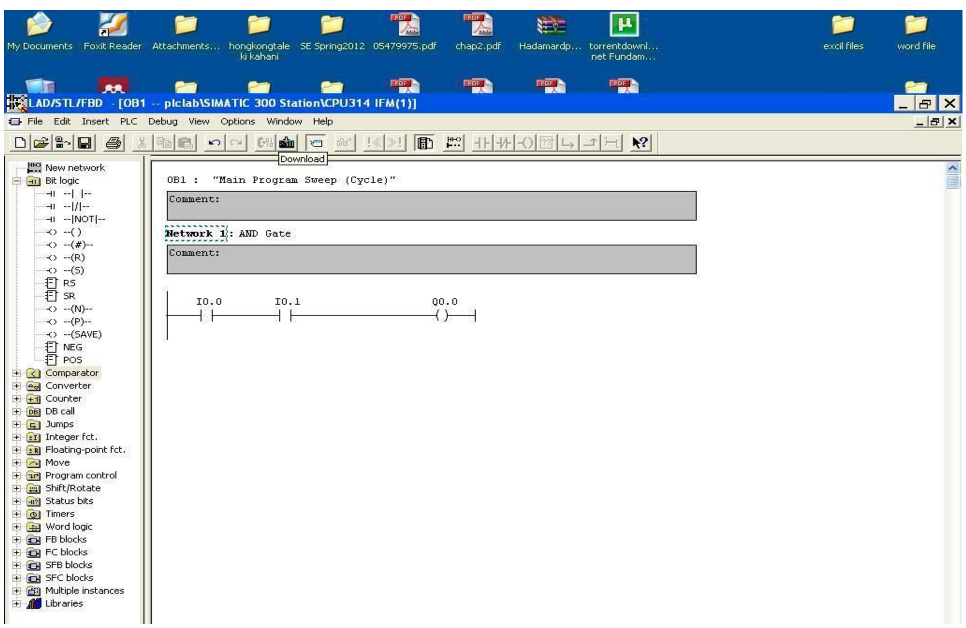
10. Add input and output variables in the simulator window



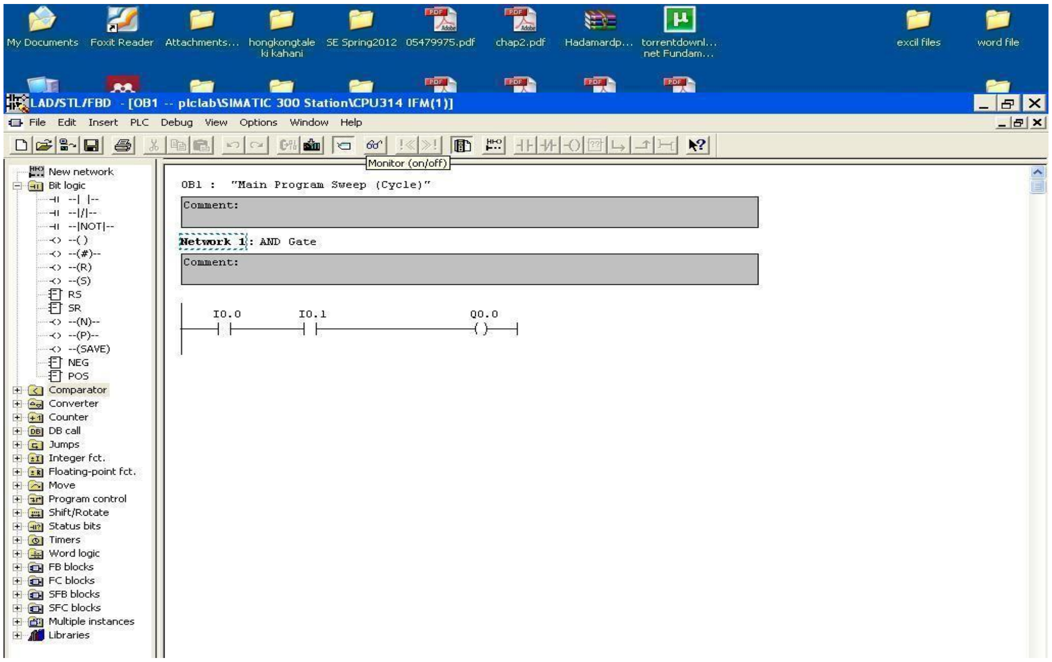
11. Assign addresses to the input and output as follows



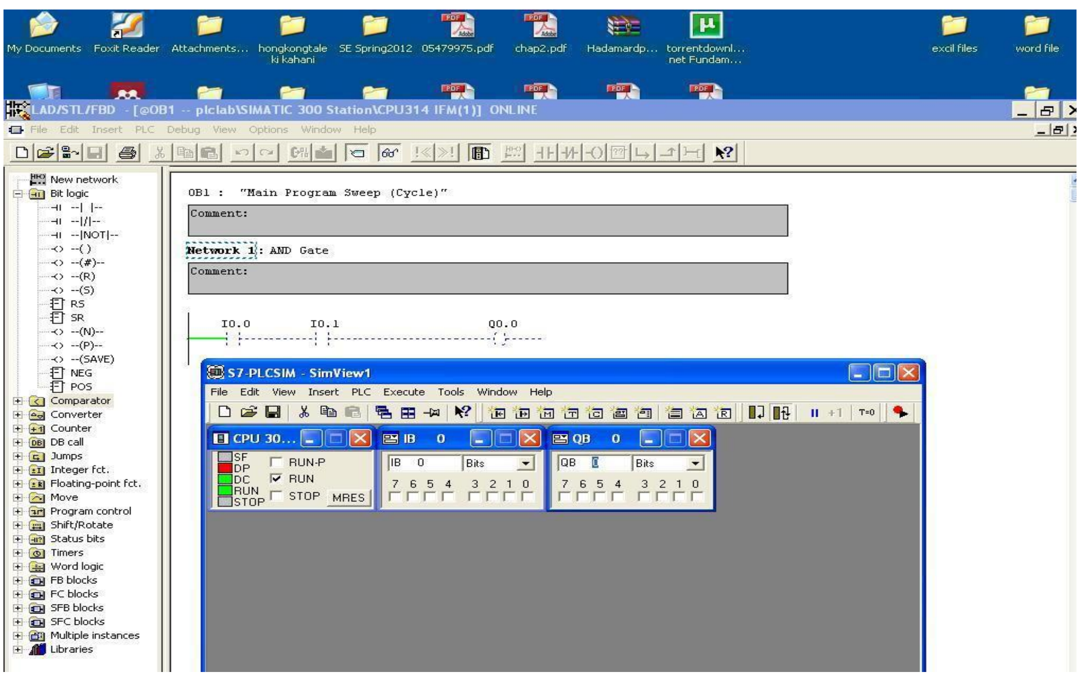
12. Click Download



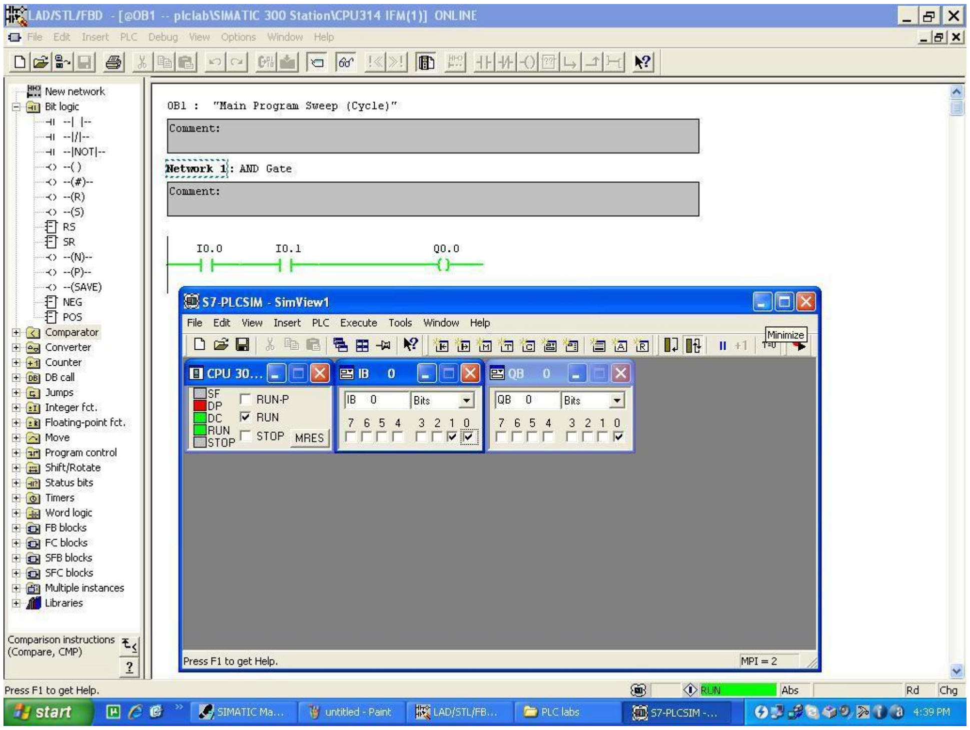
13. Click Monitor



14. Select Run in the simulator window



15. Select bit for Logic 1 and unselect for Logic 0. Verify the AND logic.



Post Lab:

Draw and soft simulate the ladder logic of following gates:

OR Gate
NOR Gate
NAND Gate
XOR Gate
NOT Gate
XNOR Gate

LAB SESSION 06

To implement two and three input logic gates in Siemens S7-300 PLC

Student Name: ______________________________

Roll no.:________________ Batch: _____________

Semester: _____________ Year: _______________

Total Marks	Marks Obtained

Remarks (if any):_______________________________

Instructor Name: _______________________________

Instructor Signature: _____________ Date: ________

Lab No. 6

Objective:

To implement two and three input logic gates in Siemens S7-300 PLC

LearningOutcomes:

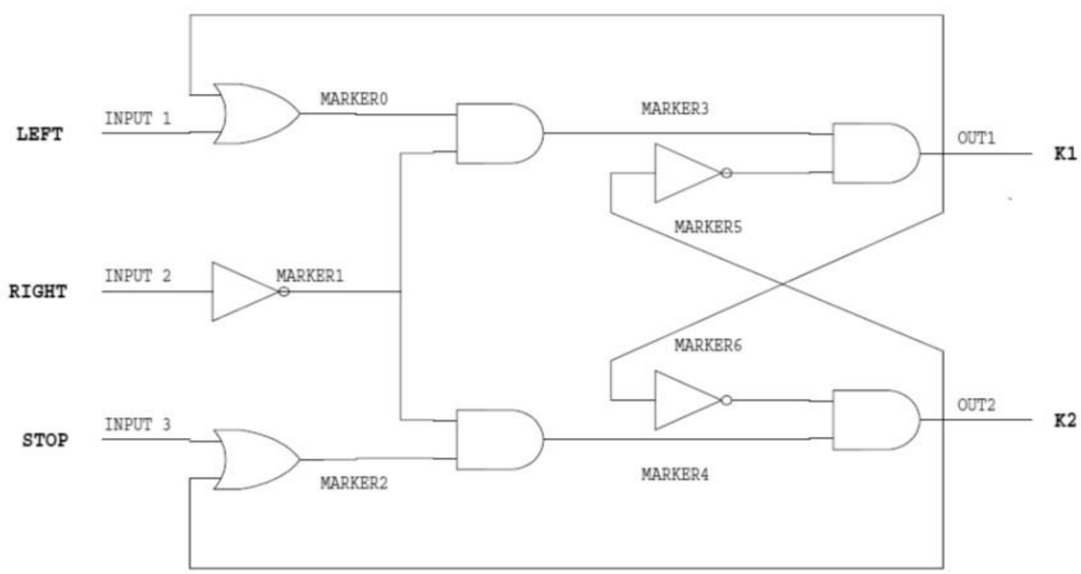
To learn how to download a program in a PLC
To understand operation of Siemens S7-300 PLC

Procedure:

1. Draw AND logic gate in software as described in lab 3.
2. Be careful in addressing the input and output. Byte address can be seen on the PLC (e.g.: I 124.0 and Q 124.0).
3. Turn on the PLC and click Download in software. This will download the program in the PLC. Do NOT turn the simulator on as in Lab 3; else the program will download in it and not the PLC. Click Monitor.
4. Now turn the knob on PLC from Stop to Run.
5. Change input logic with the help of switches on the PLC. An LED will turn on for logic 1 and will turn off for logic 0. Observe the output.
6. Repeat the procedure for OR, NOR, NAND, XOR and XNOR gates.

Post Lab:

Design ladder logic for the following circuit:



LAB SESSION 07

To design and implement the operation and application of SR and RS Flip Flops in Siemens S7-300 PLC

Student Name: ______________________________
Roll no.:_______________ Batch: _____________
Semester: ____________ Year: ______________

Total Marks	Marks Obtained

Remarks (if any):______________________________

Instructor Name: ______________________________

Instructor Signature: ____________ Date: ________

Lab No. 7

Objective:

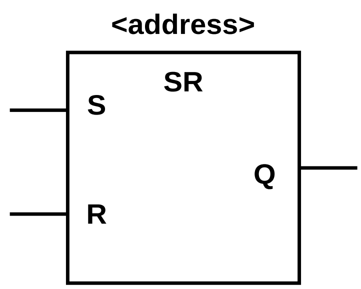
To design and implement the operation and application of SR and RS Flip Flops in Siemens S7-300 PLC

LearningOutcomes:

To understand the logical operation of PLC
To implement the operation and application of SR & RS Flip flops
To simulate their behavior in software Step 7 and implement in Siemens S7-300 PLC

SR(Set-Reset)FlipFlop:

Symbol

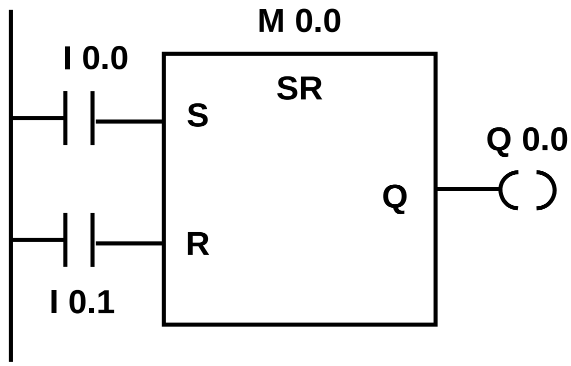


Parameter	Data Type	Memory Area	Description
<address>	BOOL	I,Q,M,L,D	Set or reset bit
S	BOOL	I,Q,M,L,D	Enabled set instruction
R	BOOL	I,Q,M,L,D	Enabled reset instruction
Q	BOOL	I,Q,M,L,D	Signal state of <address>

Description:

SR (Set-Reset Flip Flop) is set if the signal state is "1" at the S input, and "0" at the R input. Otherwise, if the signal state is "0" at the S input and "1" at the R input, the flip flop is reset. If the RLO (result of logic operation) is "1" at both inputs, the order is of primary importance. The SR flip flop executes first the set instruction then the reset instruction at the specified <address>, so that this address remains reset for the remainder of program scanning. The S (Set) and R (Reset) instructions are executed only when the RLO is "1". RLO "0" has no effect on these instructions and the address specified in the instruction remains unchanged.

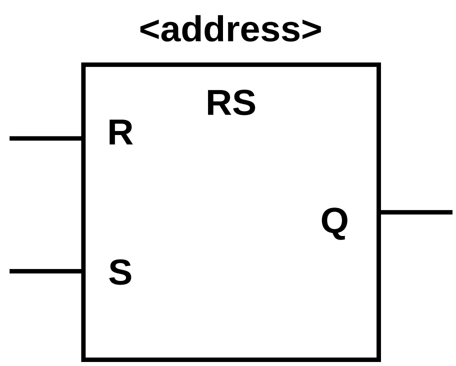
Example:



If the signal state is "1" at input I0.0 and "0" at I0.1, memory bit M0.0 is set and output Q0.0 is "1". Otherwise, if the signal state at input I0.0 is "0" and at I0.1 is "1", memory bit M0.0 is reset and output Q0.0 is "0". If both signal states are "0", nothing is changed. If both signal states are "1", the reset instruction dominates because of the order; M0.0 is reset and Q0.0 is "0".

RS (Reset-Set) Flip Flop:

Symbol

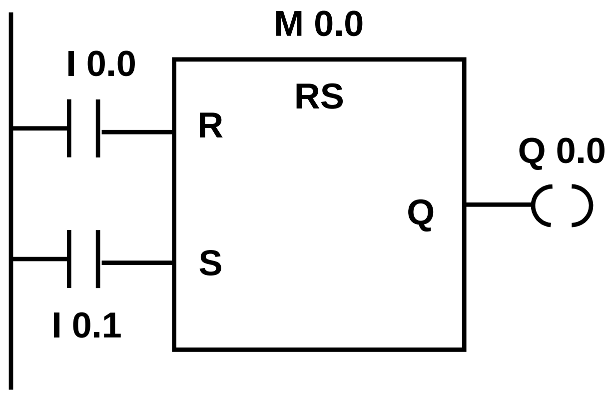


Parameter	**Data Type**	**Memory Area**	**Description**
<address>	BOOL	I,Q,M,L,D	Set or reset bit
S	BOOL	I,Q,M,L,D	Enabled set instruction
R	BOOL	I,Q,M,L,D	Enabled reset instruction
Q	BOOL	I,Q,M,L,D	Signal state of <address>

Description:

RS (Reset-Set Flip Flop) is reset if the signal state is "1" at the R input, and "0" at the S input. Otherwise, if the signal state is "0" at the R input and "1" at the S input, the flip flop is set. If the RLO is "1" at both inputs, the order is of primary importance. The RS flip flop executes first the reset instruction then the set instruction at the specified <address>, so that this address remains set for the remainder of program scanning. The S (Set) and R (Reset) instructions are executed only when the RLO is "1". RLO "0" has no effect on these instructions and the address specified in the instruction remains unchanged.

Example:



If the signal state is "1" at input I0.0 and "0" at I0.1, memory bit M0.0 is set and output Q0.0 is "0". Otherwise, if the signal state at input I0.0 is "0" and at I0.1 is "1", memory bit M0.0 is reset and output Q0.0 is "1". If both signal states are "0", nothing is changed. If both signal states are "1", the set instruction dominates because of the order; M0.0 is set and Q0.0 is "1".

Post Lab:

Design a control system for a refrigerator using one input ‘A’ such that its light ‘L’ is turned off when the door is closed and turns on when it is open. Use SR or RS flip flop to implement the logic.

Please attach flowchart of your program indicating inputs and outputs (ladder diagram code must also be included).

LAB SESSION 08

To design and implement the operation and application of various timers in Siemens S7-300 PLC

Student Name: ______________________________

Roll no.:________________ Batch: _____________

Semester: _____________ Year: _______________

Total Marks	Marks Obtained

Remarks (if any):_______________________________

Instructor Name: _______________________________

Instructor Signature: _____________ Date: ________

Lab No. 8

Objective:

To design and implement the operation and application of various timers in Siemens S7-300 PLC

LearningOutcomes:

To implement the operation and application of timers
To simulate their behavior in software Step 7 and implement in Siemens S7-300 PLC

Timers in Siemens S7-300:

The following timer instructions are available:

S_PULSE	Pulse S5 Timer
S_PEXT	Extended Pulse S5 Timer
S_ODT	On-Delay S5 Timer
S_ODTS	Retentive On-Delay S5 Timer
S_OFFDT	Off-Delay S5 Timer

Time Value

Bits 0 through 9 of the timer word contain the time value in binary code. The time value specifies a number of units. Time updating decrements the time value by one unit at an interval designated by the time base. Decrementing continues until the time value is equal to zero. The time range is from 0 to 9,990 seconds.

You can pre-load a time value using either of the following formats:

W#16#wxyz

– Where w = the time base (that is, the time interval or resolution)
– Where xyz = the time value in binary coded decimal format

S5T# aH_bbM_ccS_ddMS

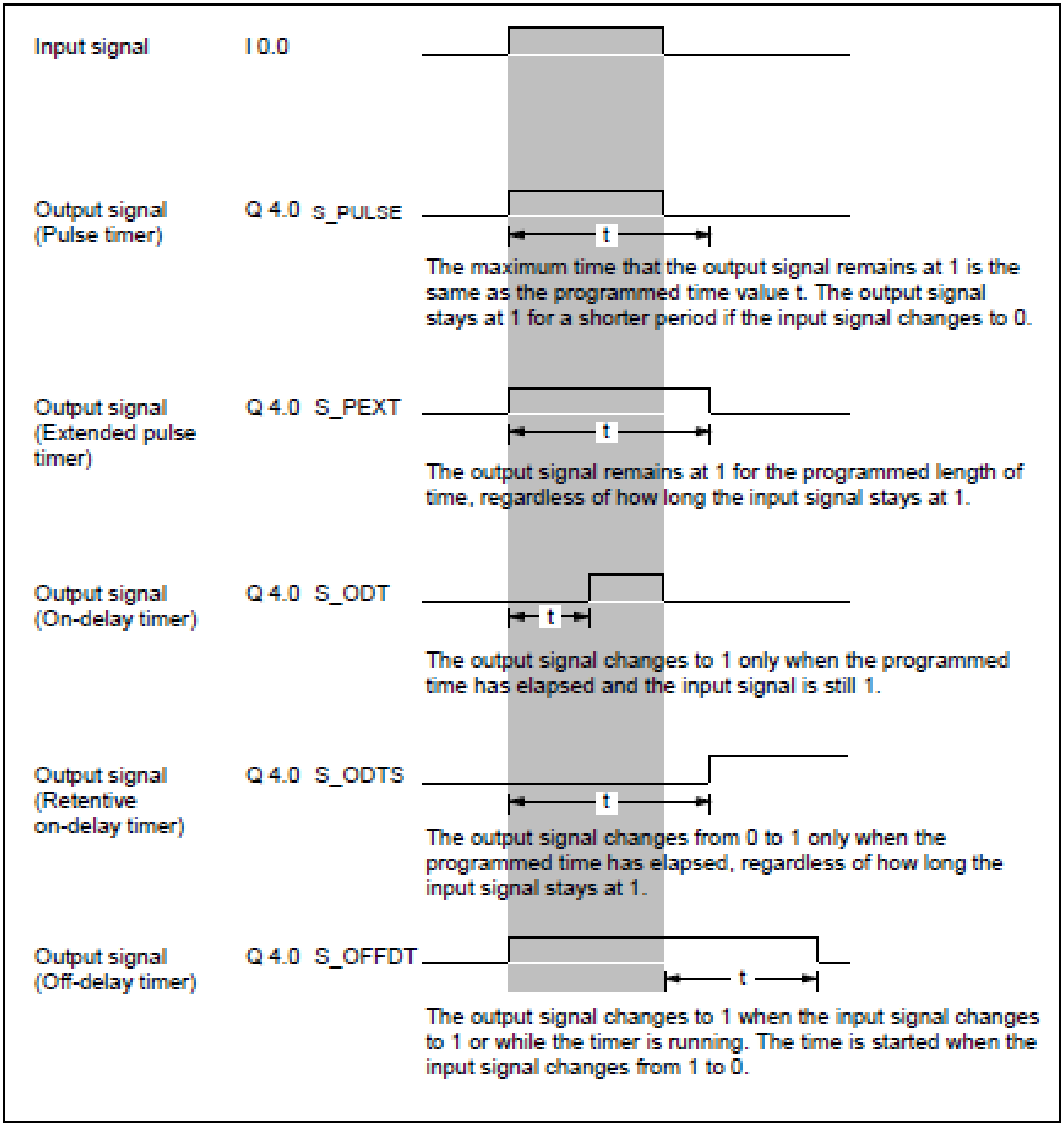
– Where a = hours, bb = minutes, cc = seconds, and dd = milliseconds

For example:

- S5TIME#4S = 4 seconds
- s5t#2h_15m = 2 hours and 15 minutes
- S5T#1H_12M_18S = 1 hour, 12 minutes, and 18 seconds

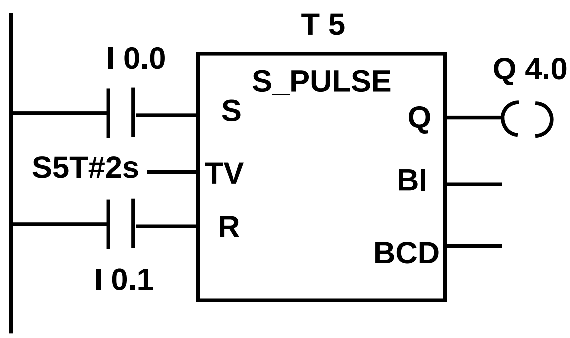
– The time base is selected automatically, and the value is rounded to the next lower number with that time base.
The maximum time value that you can enter is 9,990 seconds, or 2H_46M_30S.

Choosing the Right Timer
This overview is intended to help you choose the right timer for your timing job.



Parameter	Data Type	Memory Area	Description
T no.	TIMER	T	Timer identification number; range depends on CPU
S	BOOL	I, Q, M, L, D	Start input
TV	S5TIME	I, Q, M, L, D	Preset time value
R	BOOL	I, Q, M, L, D	Reset input
BI	WORD	I, Q, M, L, D	Remaining time value, integer format
BCD	WORD	I, Q, M, L, D	Remaining time value, BCD format
Q	BOOL	I, Q, M, L, D	Status of the timer

Example:



If the signal state of input I0.0 changes from "0" to "1" (positive edge in RLO), the timer T5 will be started. The timer will continue to run for the specified time of t wo seconds (2 s) as long as I0.0 is "1". If the signal state of I0.0 changes from "1" to "0" before the timer has expired, the timer will be stopped. If the signal state of input I0.1 changes from "0" to "1" while the timer is running, the time is reset. The output Q4.0 is logic "1" as long as the timer is running and "0" if the time has elapsed or was reset.

Post Lab:

Draw ladder diagram for the following:

1. If the signal state of input I0.0 changes from "0" to "1" (positive edge in RLO), the timer T5 will be started. The timer will continue to run for the specified time of two seconds (2 s) without being affected by a negative edge at input S. If the signal state of I0.0 changes from "0" to "1" before the timer has expired the timer will be re-triggered. The output Q4.0 is logic "1" as long as the timer is running.

2. If the signal state of I0.0 changes from "0" to "1" (positive edge in RLO), the timer T5 will be started. If the time of two seconds elapses and the signal state at input I0.0 is still "1", the output Q4.0 will be "1". If the signal state of I0.0 changes from "1" to "0", the timer is stopped and Q4.0 will be "0" (if the signal state of I0.1 changes from "0" to "1", the time is reset regardless of whether the timer is running or not).
3. If the signal state of I0.0 changes from "1" to "0", the timer is started. Q4.0 is "1" when I0.0 is "1" or the timer is running. (if the signal state at I0.1 changes from "0" to "1" while the time is running, the timer is reset).
4. If the signal state of I0.0 changes from "0" to "1" (positive edge in RLO), the timer T5 will be started. The timer runs without regard to a signal change at I0.0 from "1" to "0". If the signal state at I0.0 changes from "0" to "1" before the timer has expired, the timer will be re-triggered. The output Q4.0 will be "1" if the timer elapsed. (If the signal state of input I0.1 changes from "0" to "1", the time will be reset irrespective of the RLO at S.).

LAB SESSION 09

To design and analyze the operation and application of various counters in Siemens S7-300 PLC

Student Name: ______________________________

Roll no.:________________ Batch: _____________

Semester: _____________ Year: _______________

Total Marks	Marks Obtained

Remarks (if any):_______________________________

Instructor Name: _______________________________

Instructor Signature: _____________ Date: ________

Lab No. 9

Objective:

To design and analyze the operation and application of various counters in Siemens S7-300 PLC

LearningOutcomes:

To implement the operation and application of counters
To simulate their behavior in software Step 7 and implement in Siemens S7-300 PLC

Counters in Siemens S7-300:

The following counter instructions are available:

Up Counter
Down Counter
Up-Down Counter

Count Value

Bits 0 through 9 of the counter word contain the count value in binary code. The count value is moved to the counter word when a counter is set. The range of the count value is 0 to 999. You can vary the count value within this range by using the Up-Down Counter, Up Counter, and Down Counter instructions.

Bit Configuration in the Counter

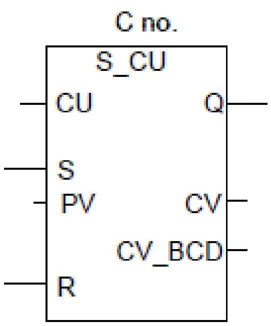
You provide a counter with a preset value by entering a number from 0 to 999, for example 127, in the following format:

C#127

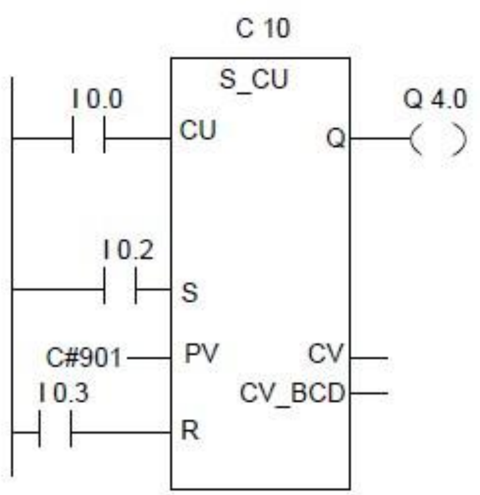
The C# stands for binary coded decimal format (BCD format: each set of four bits contains the binary code for one decimal value).

Up Counter:

A positive edge (i.e. a change in signal state from 0 to 1) at input S of the Up Counter instruction sets the counter with the value at the Preset Value (PV) input. With a positive edge, the counter is reset at input R. The resetting of the counter sets the count value to 0. With a positive edge, the value of the counter at input CU is increased by 1 when the count value is less than 999. A signal state check for 1 at output Q produces a result of 1 when the count is greater than 0; the check produces a result of 0 when the count is equal to 0.

LAD Box	Parameter	Data Type	Memory Area	Description
	no.	COUNTER	C	Counter identification number. The range depends on the CPU.
	CU	BOOL	I, Q, M, D, L	Count up input CU
	S	BOOL	I, Q, M, D, L	Set input for presetting counter
	PV	WORD	I, Q, M, D, L	Value in the range of 0 to 999 for presetting counter (entered as C#<value> to indicate BCD format)
	R	BOOL	I, Q, M, D, L	Reset input
	Q	BOOL	I, Q, M, D, L	Status of the counter
	CV	WORD	I, Q, M, D, L	Current counter value (integer format)
	CV_BCD	WORD	I, Q, M, D, L	Current counter value (BCD format)

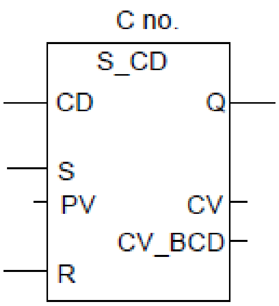
Example



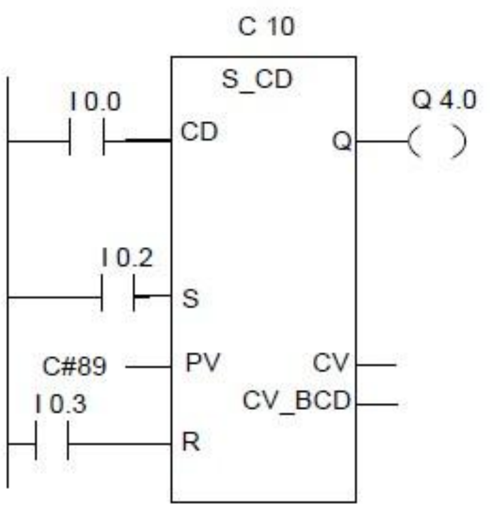
A change in signal state from 0 to 1 at input I 0.2 sets counter C 10 with the value 901 in binary coded decimal format. If the signal state of I 0.0 changes from 0 to 1, the value of counter C 10 is increased by 1, unless the value of C 10 is equal to 999. If I 0.3 changes from 0 to 1, the value of C 10 is set to 0. The signal state of output Q 4.0 is 1 if C 10 is not equal to 0.

Down Counter:

A positive edge (that is, a change in signal state from 0 to 1) at input S of the Down Counter instruction sets the counter with the value at the Preset Value (PV) input. With a positive edge, the counter is reset at input R. The resetting of the counter sets the count value to 0. With a positive edge, the value of the counter at the input is reduced by 1 when the count value is greater than 0. A signal state check for 1 at output Q produces a result of 1 when the count is greater than 0; the check produces a result of 0 when the count is equal to 0.

LAD Box	Parameter	Data Type	Memory Area	Description
	no.	COUNTER	C	Counter identification number. The range depends on the CPU.
	CD	BOOL	I, Q, M, D, L	Count down input CD
	S	BOOL	I, Q, M, D, L	Set input for presetting counter
	PV	WORD	I, Q, M, D, L	Value in the range of 0 to 999 for presetting counter (entered as C#<value> to indicate BCD format)
	R	BOOL	I, Q, M, D, L	Reset input
	Q	BOOL	I, Q, M, D, L	Status of the counter
	CV	WORD	I, Q, M, D, L	Current counter value (integer format)
	CV_BCD	WORD	I, Q, M, D, L	Current counter value (BCD format)

Example:

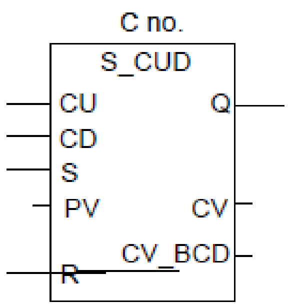


A change in signal state from 0 to 1 at input I 0.2 sets counter C 10 with the value 89 in binary coded decimal format. If the signal state of input I 0.0 changes from 0 to 1, the value of counter C 10 is decreased by 1, unless the value of counter C 10 is equal to 0. The signal state of output Q 4.0 is 1 if counter C 10 is not equal to 0. If I 0.3 changes from 0 to 1, the value of C 10 is set to 0.

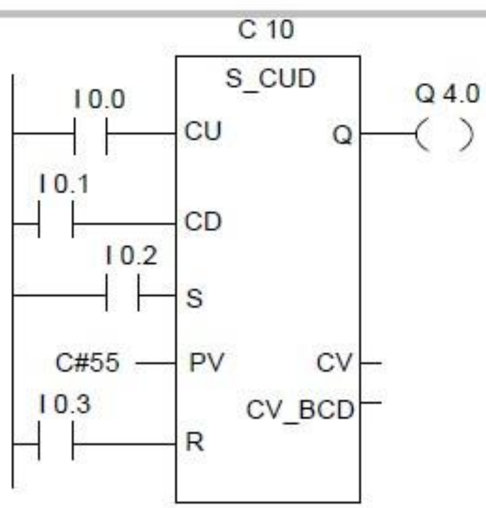
Up-Down Counter:

A positive edge (i.e. a change in signal state from 0 to 1) at input S of the Up-Down Counter instruction sets the counter with the value at the Preset Value (PV) input. A signal state of 1 at input R resets the counter. Resetting the counter places the value of the count at 0. The counter is incremented by 1 if the signal state at input CU changes from 0 to 1 (that is, there is a positive edge) and the value of the counter is less than 999. The counter is decremented by 1 if the signal state at input CD changes from 0 to 1 (that is, there is a positive edge) and the value of the counter is more than 0.

If there is a positive edge at both count inputs, both operations are executed and the count remains the same. A signal state check for 1 at output Q produces a result of 1 when the count is greater than 0; the check produces a result of 0 when the count is equal to 0.

LAD Box	Parameter	Data Type	Memory Area	Description
	no.	COUNTER	C	Counter identification number. The range depends on the CPU.
	CU	BOOL	I, Q, M, D, L	Count up input CU
	CD	BOOL	I, Q, M, D, L	Count down input CD
	S	BOOL	I, Q, M, D, L	Set input for presetting counter
	PV	WORD	I, Q, M, D, L	Value in the range of 0 to 999 for presetting counter (entered as C#<value> to indicate BCD format)
	R	BOOL	I, Q, M, D, L	Reset input
	Q	BOOL	I, Q, M, D, L	Status of the counter
	CV	WORD	I, Q, M, D, L	Current counter value (integer format)
	CV_BCD	WORD	I, Q, M, D, L	Current counter value (BCD format)

Example



A change in signal state from 0 to 1 at input I 0.2 sets counter C 10 with the value 55 in binary coded decimal format. If the signal state of input I 0.0 changes from 0 to 1, the value of counter C 10 is increased by 1, except when the value of counter C 10 is equal to 999. If input I 0.1 changes from 0 to 1, counter C 10 is decreased by 1, except when the value of counter C 10 is equal to 0. If I 0.3 changes from 0 to 1, the value of C 10 is set to 0.
Q 4.0 is 1, when C 10 is not equal to "0".

Post Lab:

Draw ladder diagram for the following:

1. Develop the ladder logic that will turn on a light, after switch A has been closed 10 times. Push button B will reset the counters.
2. A buffer can hold up to 10 parts. Parts enter the buffer on a conveyor controller by output conveyor. As parts arrive they trigger an input sensor *enter*. When a part is removed from the buffer they trigger the *exit* sensor. Write a program to stop the conveyor when the buffer is full. As normal, the system should also include a start and stop button

.

LAB SESSION 10

To develop PLC Ladder Logic Diagram for controlling operation of an overhead tank.

Student Name: ______________________________

Roll no.:________________ Batch: _____________

Semester: _____________ Year: _______________

Total Marks	Marks Obtained

Remarks (if any):_______________________________

Instructor Name: _______________________________

Instructor Signature: _____________ Date: ________

Lab No. 10

Objective:

To develop PLC Ladder Logic Diagram for controlling operation of an overhead tank.

LearningOutcomes:

To put to practice the concepts learnt so far.
To simulate the program in software Step 7 and implement in Siemens S7-300 PLC.

Task:

Consider an overhead tank. One pump is used to fill the tank and second pump is used to empty it. Mixer is used to mix the chemical in the tank. Design a PLC based ladder diagram to control the system by understanding the following conditions:

System will be on if momentary main switch SW1 is pressed once and will be off if shutdown momentary switch SW2 is pressed once.

Pump P1 will be on if level of chemical is going down from lower level sensor LS1 and will be off if level of chemical is going up from upper level sensor LS2.

Mixer M1 will be on for 5 seconds if pump P1 is not activated and level of chemical is just above from LS1

Pump P2 will be on after stoppage of mixer M1 and will be off when level of LS1 is achieved

.

LAB SESSION 11

To develop PLC Ladder Logic Diagram for controlling operation of a conveyer belt.

Student Name: ______________________________
Roll no.:________________ Batch: _____________
Semester: _____________ Year: _______________

Total Marks	Marks Obtained

Remarks (if any):_______________________________

Instructor Name: _______________________________

Instructor Signature: _____________ Date: ________

Lab No 11

Objective:

To develop PLC Ladder Logic Diagram for controlling operation of a conveyer belt.

LearningOutcomes:

- To put to practice the concepts learnt so far
- To simulate the program in software Step 7 and implement in Siemens S7-300 PLC

Task:

Design a Conveyor belt system which contains a DC motor, a limit switch, an optocoupler to count objects on the belt and Enable push switch to activate counting. Draw a PLC ladder diagram for this system such that:

- Conveyor belt should not move if limit switch is activated and it should not move if count value of objects sensed by the optocoupler is reached to 40.
- Counting of objects should be enabled by the Enable switch.

<u>LAB SESSION 12</u>

To develop PLC Ladder Logic Diagram for controlling operation of an industrial tank unit

Student Name: ______________________________

Roll no.:________________ Batch: _____________

Semester: _____________ Year: _______________

Total Marks	Marks Obtained

Remarks (if any):________________________________

Instructor Name: ________________________________

Instructor Signature: _____________ Date: ________

Lab No. 12

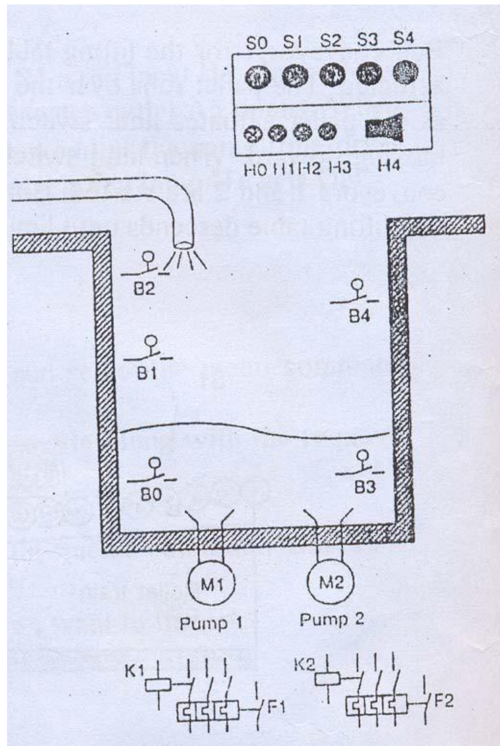
Objective:

To develop PLC Ladder Logic Diagram for controlling operation of an industrial tank unit

- To develop a function and to program its call
- To understand the SR function
- To Create and use variable table

Task:

A collecting basin for waste water is emptied using two pumps. The system is started when ENABLE button E0 is pressed.



Pump P1:

Start: The pump is started either manually by pressing momentary contact push button S2 or automatically by float switch B1. When the water level is exceeded

STOP: if the water level falls below float switch B0, the pump switch off automatically at any time by pressing push button S1 or by thermal over current release F1

Pump P2:

Start: The pump is started either manually by pressing momentary contact push button S4 or automatically by float switch B4 When the water level is exceeded.

Stop: If the water level falls below float switch B3, the pump switch off automatically at any time by pressing push button S3 or by thermal over current release F2.

Lamp H0 to H3 indicates the operating state of the pups. Whole of the system is shut down when stop push button S0 is pressed. Hooter H4 must sound when the water level reaches float switch B2 or when a pump fails because the associated thermal over current release has tripped.

LAB SESSION 13

To develop PLC Ladder Logic Diagram to interface and to control industrial actuator (AC/DC motors or as provided)

Student Name: ______________________________
Roll no.:________________ Batch: _____________
Semester: _____________ Year: _______________

Total Marks	Marks Obtained

Remarks (if any):_______________________________

Instructor Name: _______________________________

Instructor Signature: _____________ Date: ________

Lab No.13

Objective:

To develop PLC Ladder Logic Diagram to interface and to control industrial actuator (AC/DC motors or as provided)

Task:

Build hardware and interfacing circuitry for the interfacing of given actuator
Build PLC logic to control given actuator

Interfacingcircuit:

Provide your interfacing circuitry diagram below:

PLCLogic:

Provide your PLC logic for given task:

Results:

Following results are observed:

LAB SESSION 14

To develop PLC Ladder Logic Diagram to interface and to control industrial actuator (valves/pumps or as provided)

Student Name: ______________________________
Roll no.:________________ Batch: _____________
Semester: _____________ Year: _______________

Total Marks	Marks Obtained

Remarks (if any):_______________________________

Instructor Name: _______________________________

Instructor Signature: _____________ Date: ________

Lab No. 14

Objective:

To develop PLC Ladder Logic Diagram to interface and to control industrial actuator (valves/pumps or as provided)

Task:

Build hardware and interfacing circuitry for the interfacing of given actuator
Build PLC logic to control given actuator

Interfacingcircuit:

Provide your interfacing circuitry diagram below:

PLCLogic:

Provide your PLC logic for given task:

Results:

Following results are observed