



Department of Electronic Engineering

N.E.D. University of Engineering & Technology,

PRACTICAL WORK BOOK

For the course

ELECTRONICS DEVICES & CIRCUITS (EDC)

(EL - 236) For S.E (EL)

Instructors name: _____

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

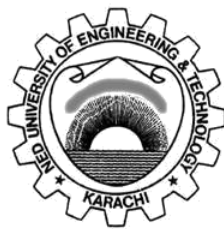
Department: _____

LABORATORY WORK BOOK

FOR THE COURSE

Electronics Devices & Circuit (EDC) (EL-236)

Prepared By:
Ayesha Akhtar (Lecturer)



Approved By:
The Board of Studies of Department of Electronic Engineering

Electronics Devices & Circuits laboratory

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LAB SESSION 01

- A. Identify the type of transistor.
- B. Implement the voltage divider bias circuit and find DC voltages and current values. Also determine its mode of operation.

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Skill Sets	Psychomotor Domain Assessment Rubric-Level P3				
	Extent of Achievement				
	0	1	2	3	4
Equipment Identification Sensual ability to identify equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
Procedural Skills Displays skills to act upon sequence of steps in lab work	Unable to either learn or perform lab work procedure	Able to slightly understand lab work procedure and perform lab work	Able to somewhat understand lab work procedure and perform lab work	Able to moderately understand lab work procedure and perform lab work	Fully understands lab work procedure and perform lab work
Response Capability to imitate the lab work on his/her own	Unable to imitate the lab work	Able to slightly imitate the lab work	Able to somewhat imitate the lab work	Able to moderately imitate the lab work	Fully imitates lab work
Observation's Use Displays skills to perform related mathematical calculations using the observations from lab work	Unable to use lab work observations for mathematical calculations	Able to slightly use lab work observations for mathematical calculations	Able to somewhat use lab work Observations for mathematical calculations	Able to moderately use lab work Observations for mathematical calculations	Fully use lab work observations for mathematical calculations
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 01

Objective:

- A. Identify the type of transistor.
- B. Implement the voltage divider bias circuit and find DC voltages and current values. Also determine its mode of operation.

Equipment Required:

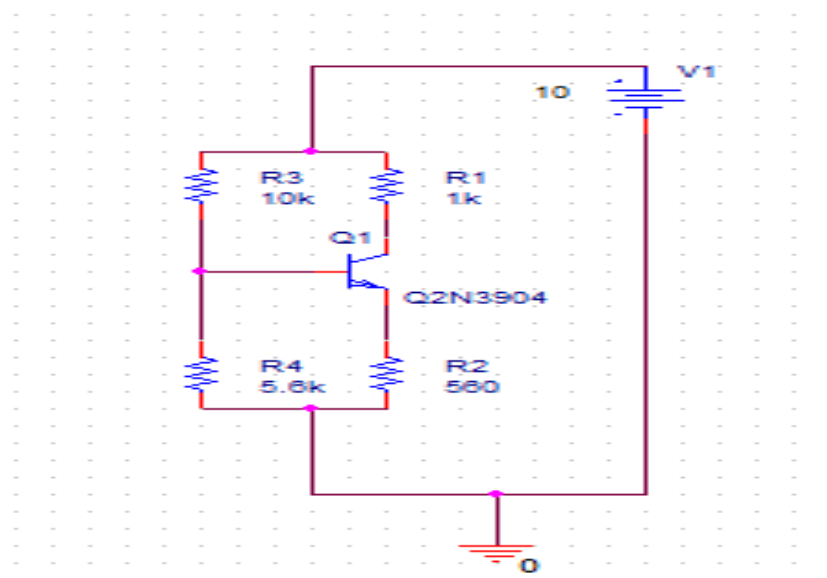
- Protoboard
- DC supply
- Resistors
- BJT
- Digital Multimeter

Theory:

A transistor is a solid state device made from semiconductor material with connections made at three or more points where the electrical characteristics are different. The term transistor comes from the words transfer and resistor. The term was adopted because it best describes the actual operation of transistor, the transfer of an input signal current from a low resistance circuit to a high resistance output circuit.

A transistor must be properly biased in order to operate as an amplifier. DC biasing is used to establish a steady level of transistor current and voltage called the dc operating point (Q-Point). Voltage divider bias provides good Q-point stability with a single polarity supply voltage. It is the most common bias circuit.

Circuit Diagram



Observations:

Parameters	Measured value	Expected value
I_C		
V_E		
V_B		
V_C		
V_{CE}		

Mode of operation: _____

Calculations:

LAB SESSION 02

A. To investigate the operation of Common Emitter Amplifier

B. To describe the purpose of components present in Common Emitter Amplifier

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Skill Sets	Psychomotor Domain Assessment Rubric-Level P3				
	Extent of Achievement				
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Equipment Identification Sensual ability to identify equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 02

Objective::

- A. To investigate the operation of Common Emitter Amplifier
- B. To describe the purpose of components present in Common Emitter Amplifier

Equipment Required:

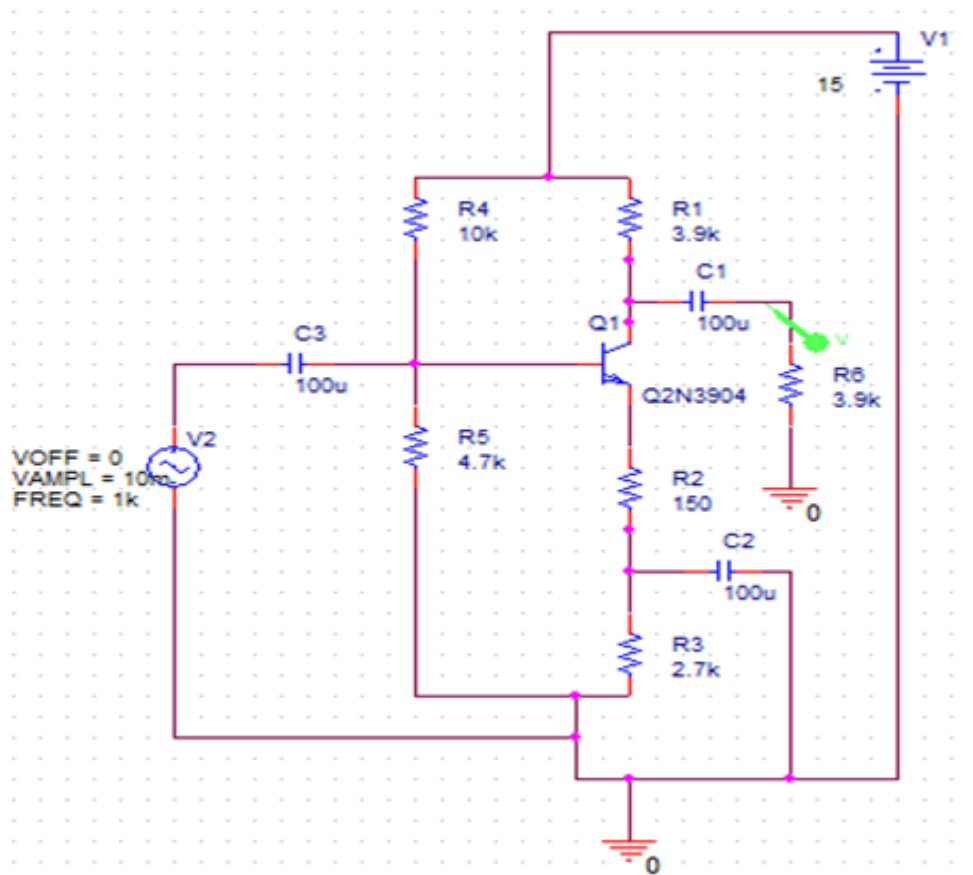
- Protoboard
- 0-15 V dc power supply
- Resistors , Capacitors
- BJT
- Digital Multimeter
- Oscilloscope
- Function generator

Theory:

The CE Amplifier is one of the three basic transistor amplifier circuit used in electronic industry. In this configuration input is applied at the base lead while its output is taken at collector, which is in 180° phase shift. The CE Amplifier exhibits high voltage and current gain.

The term “common emitter “comes from the fact that the emitter node of the transistor is connected to a “common” power rail, usually the ground. The collector node goes to the output of the circuit and the base node is an input here is design of the circuit as shown in figure. The resistor R_C is used to load the circuit via V_{cc} , other elements are used to bias the transistor. R_E and R_C seems to break the term “common emitter” because the emitter is not connected anymore directly to the ground but the point is that for all the frequencies we used, C_E acts as a low impedance capacitor so the transistor emitter is decoupled to the ground. R_E does a negative feedback which increases the stability of the transistor; this is called the emitter degeneration. In order to ensure the common emitter transistor amplifier configuration, the transistor has to be in active mode otherwise, the output is distorted due to a clipping in the negative part of the input signal. To do so, R_1 & R_2 must be chosen to have a base emitter voltage of around 0.7V, the “on” voltage of a transistor.

Circuit Diagram



Observations:

1. DC analysis

Parameters	Measured value	Expected value
V_E		
V_B		
V_C		

2. AC Analysis

V_{out} (with by-pass capacitor)	V_{out} (without by-pass capacitor)

3. Determine voltage gain

4. Draw input and output voltage waveform

Calculations:

Result:

The gain of the common emitter amplifier with load is: _____

The gain of the common emitter amplifier without load is: _____

The phase shift between input and output signal of common emitter amplifier is _____.

LAB SESSION 03

To analyse the frequency response of Common Emitter Amplifier

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Skill Sets	Psychomotor Domain Assessment Rubric-Level P3 Extent of Achievement				
	0	1	2	3	4
Equipment Identification Sensual ability to identify equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 03

Objective::

To analyse the frequency response of Common Emitter Amplifier

Equipment Required:

- Protoboard
- 0-15 V dc power supply
- Resistors , Capacitors
- BJT
- Digital Multimeter
- Oscilloscope
- Function generator

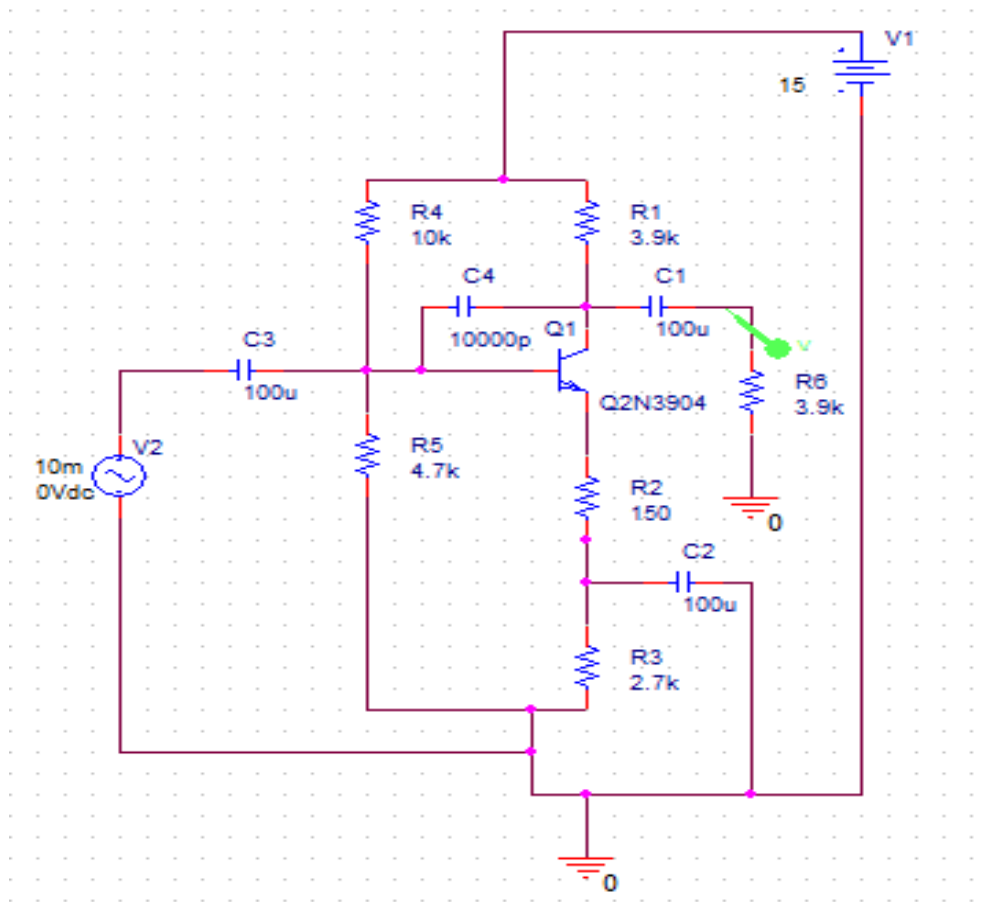
Theory:

A Common-Emitter amplifier is one of three basic single-stage bipolar-junction-transistor (BJT) amplifier topologies, typically used as a voltage amplifier. In this circuit the base terminal of the transistor serves as the input, the collector is the output, and the emitter is common to both (for example, it may be tied to ground reference or a power supply rail), hence its name.

EMITTER DEGENERATION RESISTANCE R_E introduces negative feedback in the amplifier circuit. C_1 and C_3 are coupling capacitors while C_2 is bypass capacitor. Since $X_C = 1/2\pi fC$, hence at low frequencies the reactance is greater and it decreases as the frequency increases. At low frequencies the reactance of coupling capacitance is high (The coupling and bypass capacitances are usually in microfarads) , hence they act as almost open circuit .Therefore at low frequencies the coupling capacitances act as nearly as open circuit The bypass capacitance also acts as nearly open circuit at low frequency.

In mid range frequency the coupling and by-pass capacitance act as nearly short circuit. At high frequencies, the coupling and bypass capacitors become effective ac shorts and do not effect amplifier's response.

Circuit Diagram



Observations:

FREQUENCY RESPONSE

[illegible]

Calculations:

Result:

The bandwidth of the common emitter amplifier as measured comes out to be: _____

LAB SESSION 04

A. To investigate the operation of Common Base Amplifier

B. To describe the purpose of components present in Common Base Amplifier

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____
 Laboratory Session No. _____ Date: _____

Skill Sets	Psychomotor Domain Assessment Rubric-Level P3				
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Equipment Identification Sensual ability to identify equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 04

Objective:

- A. To investigate the operation of Common Base Amplifier
- B. To describe the purpose of components present in Common Base Amplifier

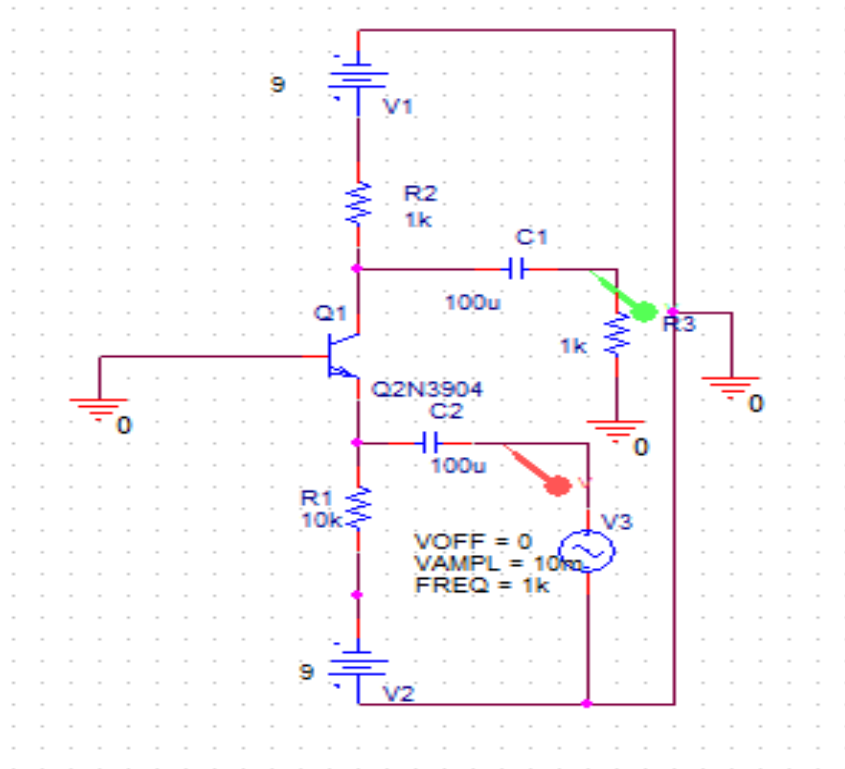
Equipment Required:

- Protoboard
- 0-15 V dc power supply
- Resistors , Capacitors
- BJT
- Digital Multimeter
- Oscilloscope
- Function generator

Theory:

In Common base amplifier input is provided at emitter lead while output is taken at Collector, so in common base both input and output signal are in phase. Voltage gain of common base is like that of common emitter. The common base amplifier has a very low input resistance but has an excellent high frequency response and thus can be combined with common emitter to obtain an excellent amplifier circuit.

Circuit Diagram



Observations:**1. DC analysis**

Parameters	Measured value	Expected value
V_E		
V_B		
V_C		

2. AC Analysis (Apply 20mV peak to peak sinusoidal input from function generator, measure output voltage)

$V_{out}(\text{with load resistor})$	$V_{out}(\text{without load resistor})$

3. Determine voltage gain**4. Draw input and output voltage waveform**

Calculations:

Results:

The gain of the common emitter amplifier with load is: _____

The gain of the common emitter amplifier without load is: _____

The phase shift between input and output signal of common emitter amplifier is _____.

LAB SESSION 05

- A. To investigate the operation of Common Collector Amplifier**
B. To describe the purpose of components present in Common Collector Amplifier

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	Extent of Achievement				
	0	1	2	3	4
Equipment Identification Sensual ability to identify equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 05

Objective:

- A. To investigate the operation of Common Collector Amplifier
- B. To describe the purpose of components present in Common Collector Amplifier

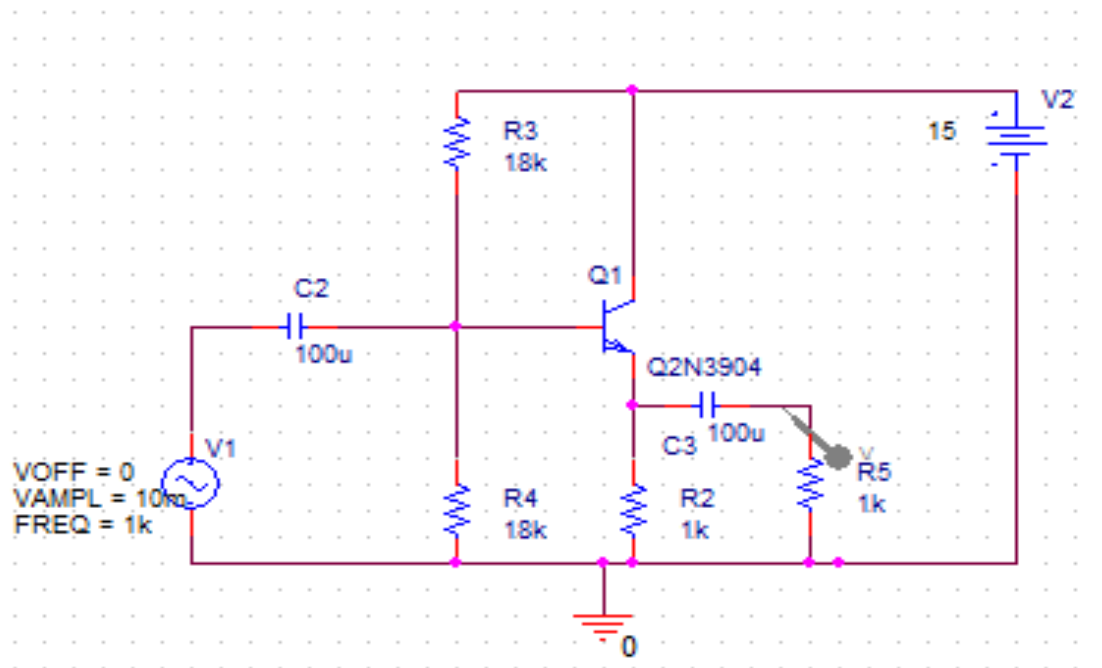
Equipment Required:

- Protoboard
- 0-15 V dc power supply
- Resistors , Capacitors
- BJT
- Digital Multimeter
- Oscilloscope
- Function generator

Theory:

The Common Collector amplifier is also known as 'Emitter Follower'. In CC Amplifier input is taken at base while output at emitter. In this configuration output follows input. The input impedance of CC amplifier is much higher than bipolar transistor amplifier.

Circuit Diagram



Observations:

1. DC Analysis

Parameters	Measured value	Expected value
V_E		
V_B		
V_C		

2. AC analysis (Apply 20mV peak to peak sinusoidal input from function generator, measure output voltage)

V_{out} (with load resistor)	V_{out} (without load resistor)

3. Determine voltage gain

4. Draw input and output voltage waveform

5. Calculations:

Results:

The gain of the common collector amplifier with load is: _____

The gain of the common collector amplifier without load is: _____

The phase shift between input and output signal of common collector amplifier is _____.

LAB SESSION 06

To demonstrate the operation of Combination of CE Amplifier and Emitter Follower (CC) Amplifier

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Skill Sets	Psychomotor Domain Assessment Rubric-Level P3				
	Extent of Achievement				
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Equipment Identification Sensual ability to identify equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 06

Objective:

To demonstrate the operation of Combination of CE Amplifier and Emitter Follower (CC) Amplifier

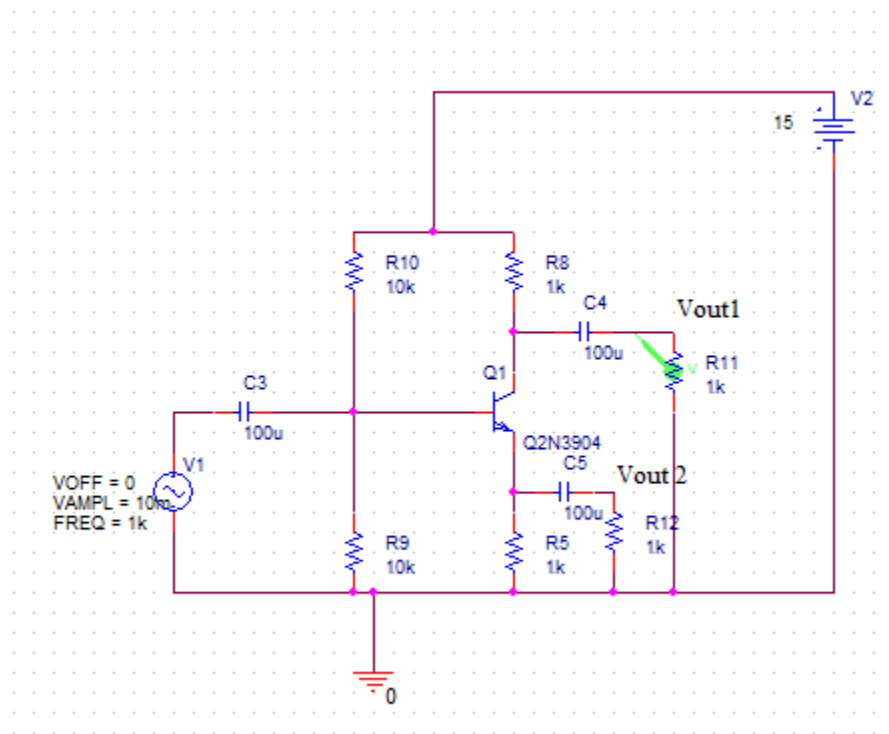
Equipment Required:

- Protoboard
- 0-15 V dc power supply
- Resistors , Capacitors
- BJT
- Digital Multimeter
- Oscilloscope
- Function generator

Theory:

Combination of CE and CC Amplifier is known as phase-splitter or paraphase amplifier which is capable of producing two identical output signals to identical loads except that they are 180° out-of-phase with each other. The output signal from the collector is simply a CE amplifier having unity voltage gain and also 180° out-of-phase with the input signal. Output is from the emitter-follower and is in-phase with the input signal.

Circuit Diagram



Observations:

1. DC analysis

Parameters	Measured value	Expected value
V_E		
V_B		
V_C		

2. AC analysis

V_{out1} (with load resistor)	V_{out1} (without load resistor)
V_{out2} (with load resistor)	V_{out2} (without load resistor)

3.Draw input and output voltage waveform

Calculations:

Result :

Vout1 with load resistor is: _____

Vout1 without load resistor is: _____

Vout2 with load resistor is: _____

Vout2 without load resistor is: _____

LAB SESSION 07

To demonstrate the operation of BJT as a Switch

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
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Course Code: _____ Course Name: _____
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 07

Objective:

To demonstrate the operation of BJT as a Switch

Equipment Required:

- Protoboard
- 0-15 V dc power supply
- Resistors
- BJT
- Digital Multimeter
- Oscilloscope
- Function generator
- LED

Theory:

Switches are needed in electronics to turn-on a voltage or current of sufficient power to operate a circuit. A bipolar junction transistor (BJT) can be used in many circuit configurations such as an amplifier, oscillator, filter, and rectifier or just used as an on-off switch. If the transistor is biased into the linear region, it will operate as an amplifier or other linear circuit, if biased alternately in the saturation and cut-off regions, then it is being used as a switch, allowing current to flow or not to flow in other parts of the circuit.

A switch consists of a BJT transistor that is alternately driven between the saturation and cut-off regions. A simple version of the switch is shown in figure. When the input equals $-V_{in}$, the base-emitter junction is reverse biased or off so no current flows in the collector. This is illustrated by the load line shown in the figure. When the BJT is in cut-off, the circuit (ideally) has the following values:

$$V_{CE} = V_{CC} \text{ and } I_C = 0 \text{ A}$$

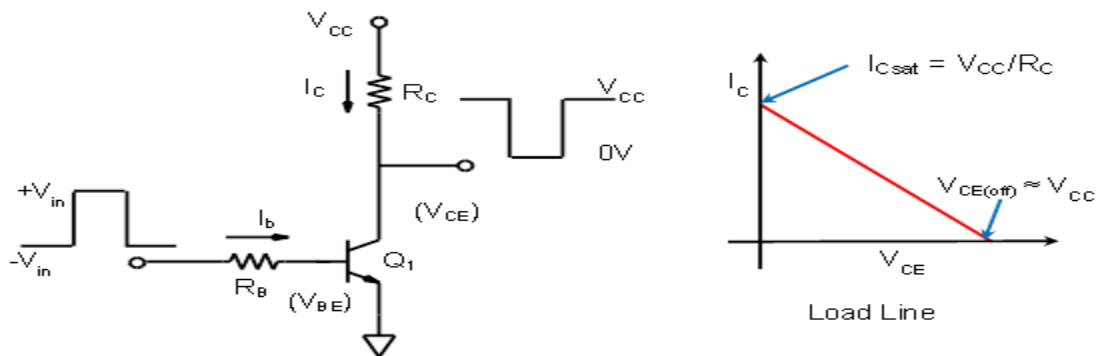
This state is similar to an open switch.

When the input equals $+V_{in}$, the transistor is driven into saturation and the following conditions occur:

$$V_{CE} \sim 0\text{V} \text{ and } I_{C\text{sat}} = V_{CC} / R_C$$

This state is similar to a closed switch connecting the bottom of R_C to ground.

Circuit Diagram



Observations:

Take $R_B = 6.8\text{k}\Omega$, $R_C = 100\Omega$, LED (any colour), $V_{CC} = 5\text{V}$

Connect an LED at the collector terminal such that its cathode should be connected to collector terminal. Observe the LED as the input goes low and high. Also measure voltages and current in the given circuit and write below:

Calculations:

Result :

When logic input is 0 the switch is: _____

When logic input is 1 the switch is: _____

LAB SESSION 08

To investigate the Operation of BJT Current Mirror

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Skill Sets	Psychomotor Domain Assessment Rubric-Level P3				
	0	1	2	3	4
Equipment Identification Sensual ability to identify equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 08

Objective:

To investigate the Operation of BJT Current Mirror

Equipment Required:

- Protoboard
- Q2N3904 BJT npn transistors
- Resistors, Capacitors
- Digital Multimeter
- Function Generator
- Oscilloscope
- Connecting wires

Theory:

The basic BJT Current Mirror is shown in figure. Neglecting base current, the reference Current I_{ref} is passes through the diode connected transistor Q_1 , & thus produces corresponding voltage V_{be} , which in turn is applied between base & emitter of Q_2 . If Q_2 is matched to Q_1 , then the collector current of Q_1 is equal to that of Q_2 .

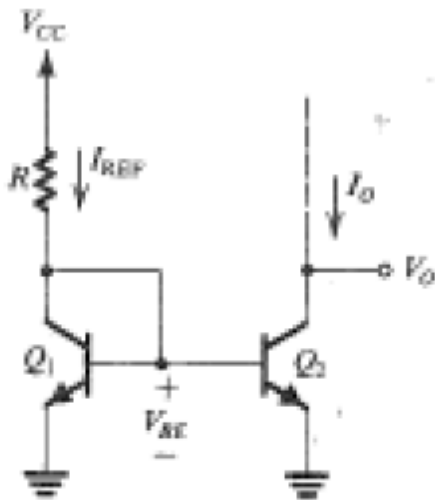


FIGURE 1

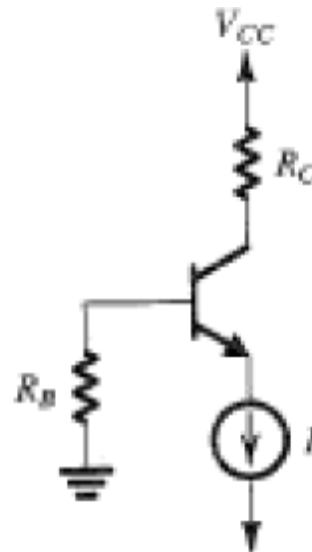


FIGURE 2

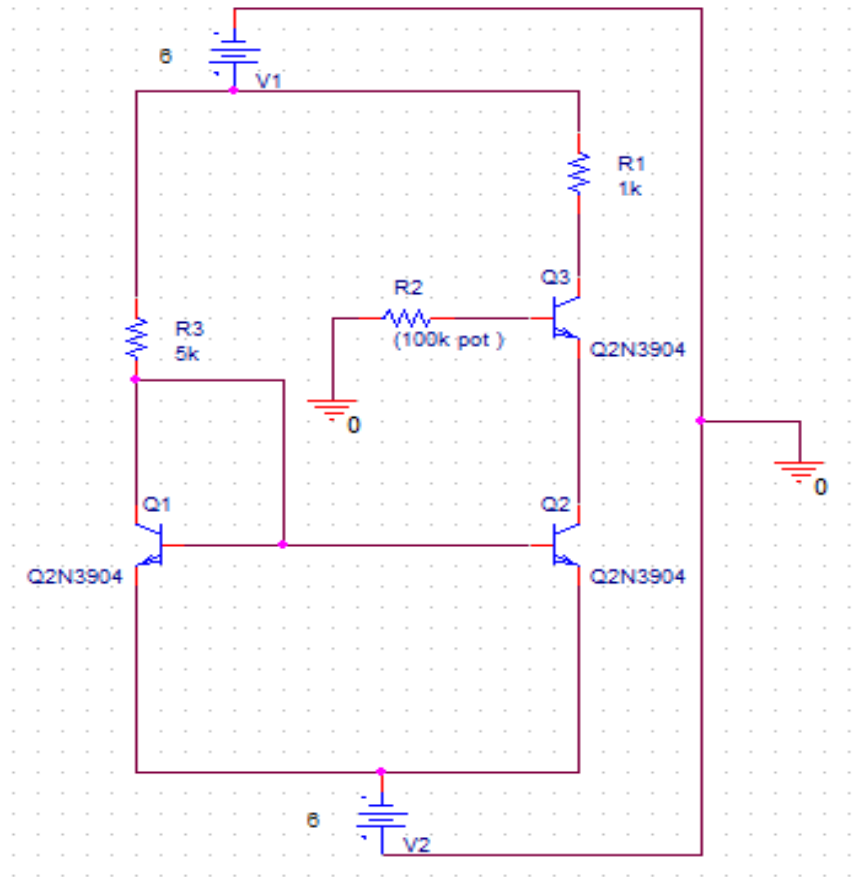


FIGURE 3

Procedure:

- Implement the circuit given in figure 3.
- Vary the potentiometer and observe changes in I_{ref} and I_o

Observations:

S. No	I_{ref}	I_o
1		
2		
3		
4		
5		
6		
7		
8		

Calculations:

Make calculation of I_o for the observed value of I_{ref} . Also calculate the percentage error.

Result:

LAB SESSION 09

To illustrate the operation of current source implemented using BJT, with Base-Current Compensation.

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 09

Objective:

To illustrate the operation of current source implemented using BJT, with Base-Current Compensation.

Equipment Required:

- Protoboard
- Q2N3904 BJT npn transistors
- Resistors, Capacitors
- Digital Multimeter
- Function Generator
- Oscilloscope
- Connecting wires

THEORY:

Figure shows a bipolar current mirror with a current transfer ratio that is much less dependent on β than that of simple current mirror. The reduced dependence is achieved by using transistor Q3

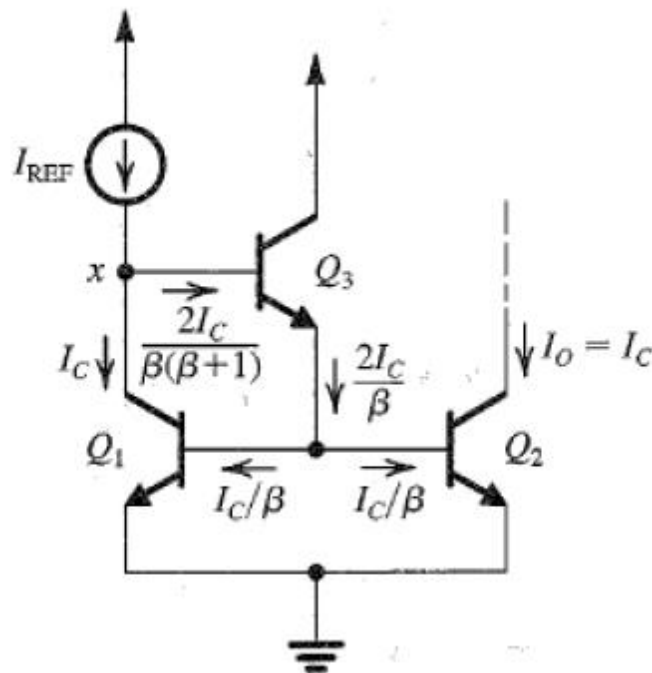


FIGURE 1

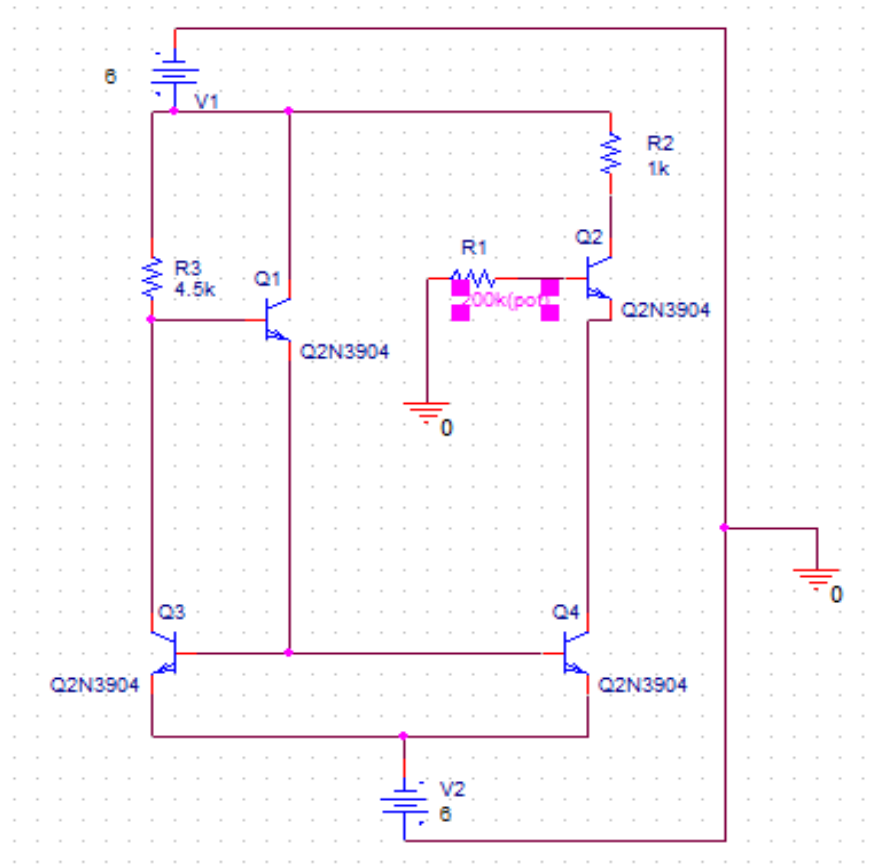


FIGURE 2

Procedure:

- Implement the circuit in figure 2 .
- Vary potentiometer & observe readings for I_{ref} & I_o

Observations:

S. No	I_{ref}	I_o
1		
2		
3		
4		
5		
6		
7		
8		

Calculations:

Make calculation of I_o for the observed value of I_{ref} . Also calculate the percentage error.

Result:

LAB SESSION 10

To illustrate the operation of BJT Differential Pair

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Skill Sets	Psychomotor Domain Assessment Rubric-Level P3				
	Extent of Achievement				
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Equipment Identification Sensual ability to identify equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 10

Objective:

To illustrate the operation of BJT Differential Pair

Equipment Required:

- Protoboard
- Q2N2222 BJT npn transistors
- Resistors, Capacitors
- Digital Multimeter
- Function Generator
- Oscilloscope
- Connecting wires

Theory:

It consists of two matched transistors, Q1 & Q2, whose emitters are joined together and biased by constant current source I. It is essential that, collector circuits be such that Q1 & Q2 never enter saturation.

Circuit Diagram

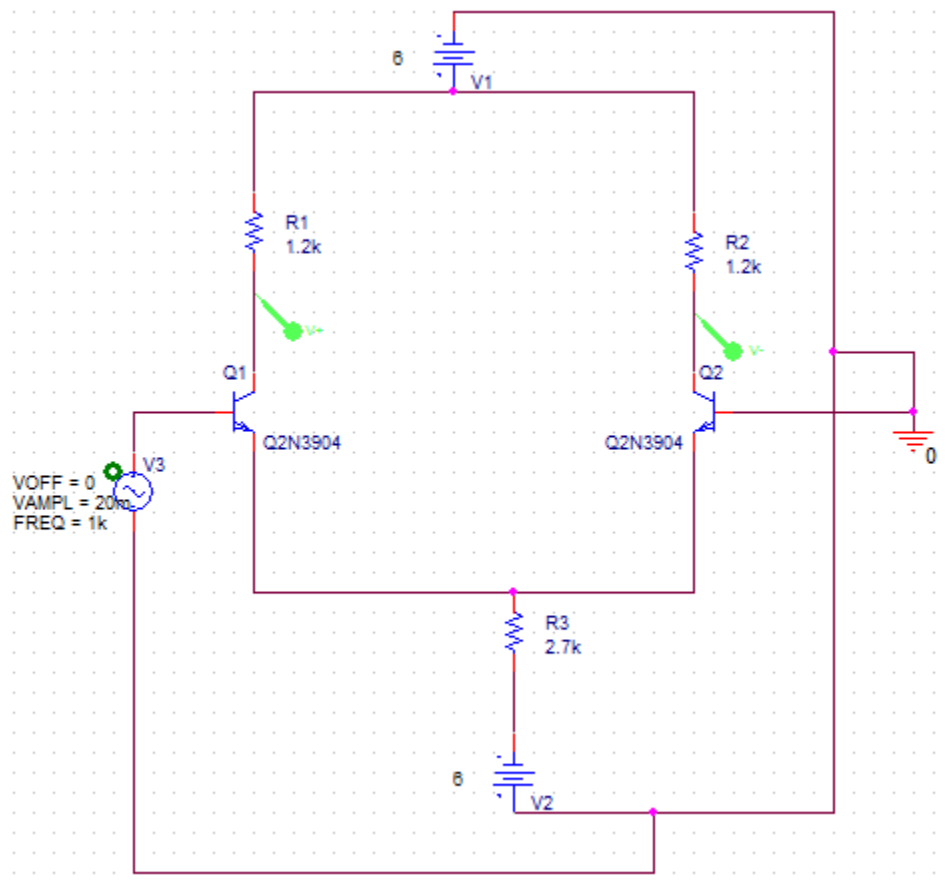


Figure 1

Observations:

S.No	V _{B1}	V _{B2}	V _{B1} -V _{B2}	V _{C1}	V _{C2}	V _{C1} -V _{C2}

3.Draw generalized output voltage waveform:

Calculations:**Result :**

V_{c1} is: _____

V_{c2} is: _____

V_{out} is: _____

LAB SESSION 11

To investigate the characteristics curves for Field Effect Transistor.

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____
 Laboratory Session No. _____ Date: _____

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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 11

Objective:

To investigate the characteristics curves for Field Effect Transistor.

Equipment Required:

- D.C power supply
- Oscilloscope
- Multimeter
- MOSFET 2N7000
- Resistors

Basic Theory

The acronym 'FET' stands for field effect transistor. It is a three-terminal unipolar solid state device in which current is controlled by an electric field as is done in vacuum tubes.

Broadly speaking, there are two types of FETs:

- (a) Junction field effect transistor (JFET)
- (b) metal-oxide semiconductor FET (MOSFET)

It is also called insulated-gate FET (IGFET). It may be further subdivided into:

- (i) depletion-enhancement MOSFET i.e. DEMOSFET
- (ii) enhancement-only MOSFET i.e. E-only MOSFET

Figure1 , shows the physical structure of the n-channel enhancement-type MOSFET. The meaning of the name s "enhancement " and "channel " will become apparent shortly. The transistor is fabricated on a p-type substrate, which is a single-crystal silicon wafer that provides physical support for the device (and for the entire circuit in the case of an integrated circuit). Two heavily doped n-type regions, indicated in the figure as the n^+ source 1 and the n^+ drain regions, are created in the substrate. A thin layer of silicon dioxide (SiO_2) of thickness t_{ox} (typically 2-50 nm), which is an excellent electrical insulator, is grown on the surface of the substrate, covering the area between the source and drain regions. Metal is deposited on top of the oxide layer to form the gate electrode of the device. Metal contacts are also made to the source region, the drain region, and the substrate, also known as the body. Thus four terminals are brought out: the gate terminal (G), the source terminal (S), the drain terminal (D), and the substrate or body terminal (B).

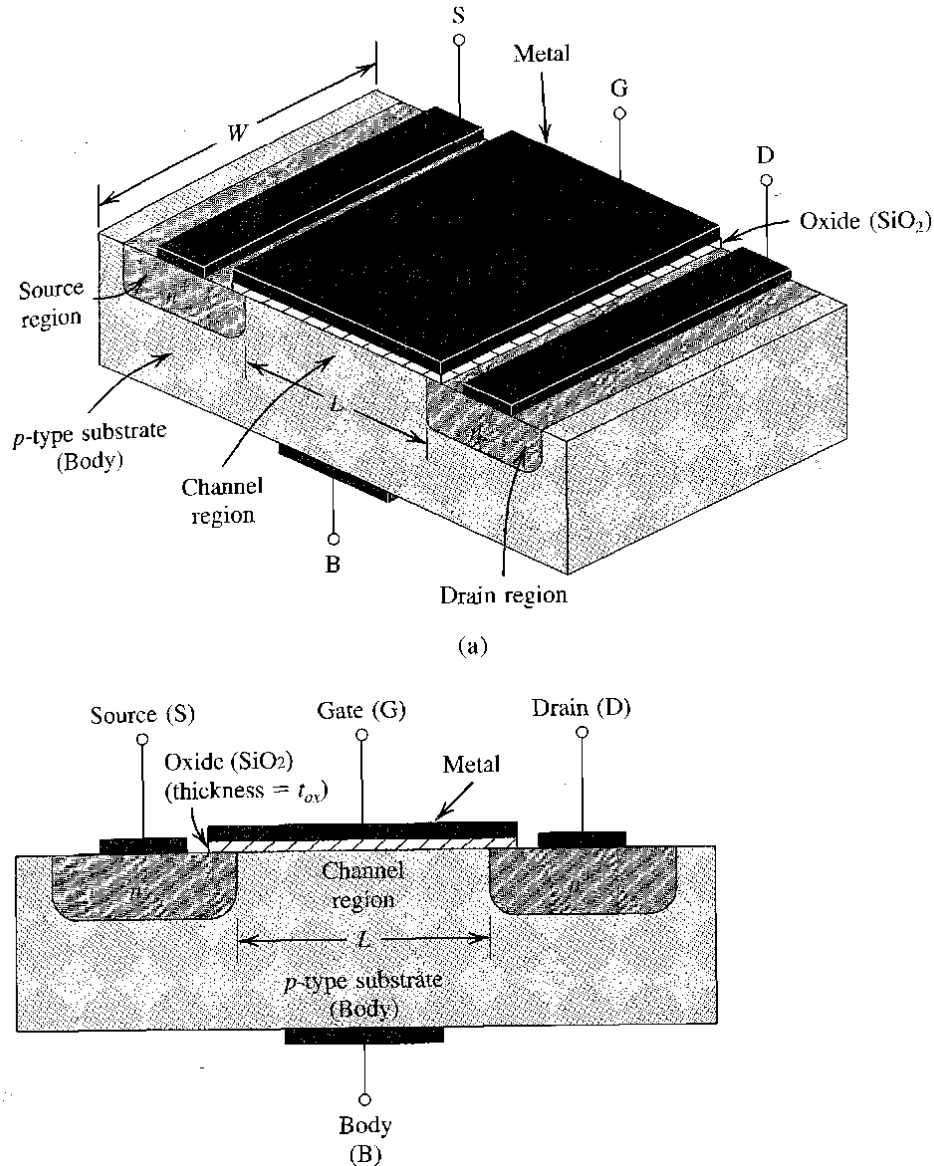


Fig.1

MOSFET with $V_{GS}=0$ and $V_{DS}=0$

With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source. One diode is formed by the pn junction between the n^+ drain region and the p-type substrate, and the other diode is formed by the pn junction between the p-type substrate and the n^+ source region. These back-to-back diodes prevent current conduction from drain to source when a voltage v_{DS} is applied. In fact, the path between drain and source has a very high resistance (of the order of $10^{12} \Omega$).

MOSFET with small V_{GS} and $V_{DS}=0$

Consider next the situation depicted in Fig. 4.2. Here we have grounded the source and the drain and applied a positive voltage to the gate. Since the source is grounded, the gate voltage appears in effect between gate and source and thus is denoted v_{GS} . The positive voltage on the gate causes, in

the first instance, the free holes (which are positively charged) to be repelled from the region of the substrate under the gate (the channel region). These holes are pushed downward into the substrate, leaving behind a carrier-depletion region. The depletion region is populated by the bound negative charge associated with the acceptor atoms. These charges are "uncovered" because the neutralizing holes have been pushed downward into the substrate. As well, the positive gate voltage attracts electrons from the n^+ source and drain regions (where they are in abundance) into the channel region. When a sufficient number of electrons accumulate near the surface of the substrate under the gate, an n region is in effect created, connecting the source and drain regions. Now if a voltage is applied between drain and source, current flows through this induced n region, carried by the mobile electrons. The induced n region thus forms a channel for current flow from drain to source and is aptly called so. Correspondingly, the MOSFET is called an n -channel MOSFET or, alternatively, an NMOS transistor. Note that an n -channel MOSFET is formed on a p -type substrate: The channel is created by inverting the substrate surface from p type to n type. Hence the induced channel is also called an inversion. The value of V_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the **threshold voltage** and is denoted V_t . Obviously, for an n -channel FET is positive. The value of V_t is controlled during device fabrication and typically lies in the range of 0.5 V to 1.0 V.

MOSFET with small V_{GS} and small V_{DS} :

Having induced a channel, we now apply a positive voltage V_{DS} between drain and source. We first consider the case where V_{DS} is small (i.e., 50 mV or so). The voltage V_{DS} causes a current i_D to flow through the induced n channel. Current is carried by free electrons traveling from source to drain (hence the names source and drain). By convention, the direction of current flow is opposite to that of the flow of negative charge. Thus the current in the channel, i_D , will be from drain to source. The magnitude of i_D depends on the density of electrons in the channel, which in turn depends on the magnitude of V_{DS} . Specifically, for $V_{GS} = V_t$, the channel is just induced and the current conducted is still negligibly small. As V_{GS} exceeds V_t , more electrons are attracted into the channel. We may visualize the increase in charge carriers in the channel as an increase in the channel depth. The result is a channel of increased conductance or, equivalently, reduced resistance. In fact, the conductance of the channel is proportional to the **excess gate voltage** ($V_{GS} - V_t$), also known as the **effective voltage** or the **overdrive voltage**. It follows that the current i_D will be proportional to $V_{GS} - V_t$, and, of course, to the voltage V_{DS} that causes i_D to flow.

MOSFET with small V_{GS} and large V_{DS} :

We next consider the situation as V_{DS} is increased. For this purpose let V_{GS} be held constant at a value greater than V_t . V_{DS} appears as a voltage drop across the length of the channel. That is, as we travel along the channel from source to drain, the voltage (measured relative to the source) increases from 0 to V_{DS} . Thus the voltage between the gate and points along the channel decreases from V_{GS} at the source end to $V_{GS} - V_{DS}$ at the drain end. Since the channel depth depends on this voltage, we find that the channel is no longer of uniform depth; rather, the channel will take the tapered form being deepest at the source end and shallowest at the drain end. As V_{DS} is increased, the channel becomes more tapered and its resistance increases correspondingly. Thus the i_D - V_{DS} curve does not continue as a straight line but bends

Eventually, when V_{DS} is increased to the value that reduces the voltage between gate and channel at the drain end to V_t —that is, $V_{GD} = V_t$ or $V_{GS} - V_{DS} = V_t$ or $V_{DS} = V_{GS} - V_t$ —the channel depth at the drain end decreases to almost zero, and the channel is said to be **pinched off**. Increasing V_{DS} beyond this value has little effect (theoretically, no effect) on the channel shape, and the current through the channel remains constant at the value reached for $V_{DS} = V_{GS} - V_t$. The drain current thus **saturates** at this value, and the MOSFET is said to have

entered the **saturation region** of operation. The voltage V_{DS} at which saturation occurs is denoted by V_{DSsat}

$$V_{DSsat} = V_{GS} - V_t$$

Obviously, for every value of $V_{GS} > V_t$, there is a corresponding value of V_{DSsat} . The device operates in the saturation region if $V_{DS} \geq V_{DSsat}$. The region of the i_D - V_{DS} characteristic obtained for $V_{DS} < V_{DSsat}$ is called the **triode region**, a carryover from the days of vacuum-tube devices whose operation a FET resembles.

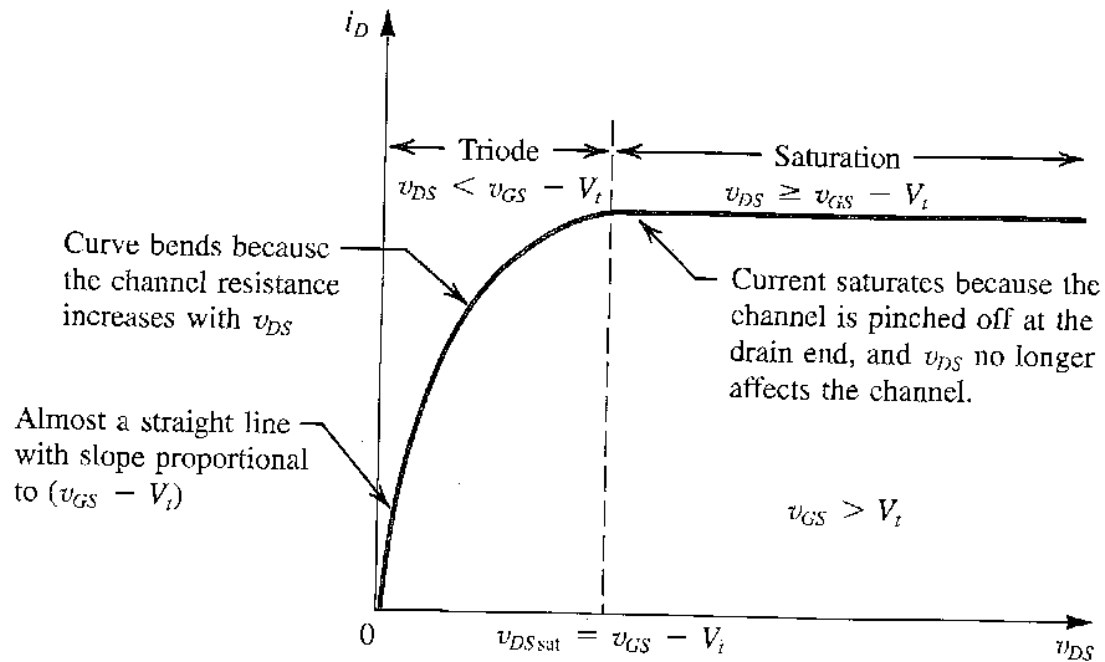


Fig.2

Procedure

1. Connect the circuit as shown in fig 3.
2. Let $V_{DS} = (0, 0.5, 1, 1.5, 2, 2.5, 3, 4, 5, 5.5, 6, 6.5, 7)$ V measure I_D .
3. Repeat step 2 for $V_{GS} = (0.5, 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7)$ V.

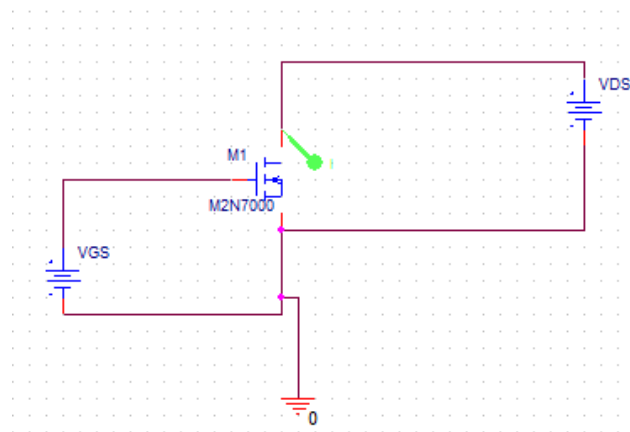


Fig. 3

Observations & Calculations

A. Draw I_D Vs V_{GS}

a) For $V_{DS}=3V$

[illegible]

B. Draw (drain characteristics) between I_D & V_{DS} for different values of V_{GS} .

a. For $V_{GS}=0.5V$

[illegible]

b. For $V_{GS}=1.5V$

[illegible]

c. For $V_{GS}=2V$

[illegible]

LAB SESSION 12

To analyze Common Source Amplifier circuit and also determine phase shift between input and output

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester: _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Skill Sets	Psychomotor Domain Assessment Rubric-Level P3				
	Extent of Achievement				
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Observation's Use Displays skills to perform related mathematical calculations using the observations from lab work	Unable to use lab work observations for mathematical calculations	Able to slightly use lab work observations for mathematical calculations	Able to somewhat use lab work Observations for mathematical calculations	Able to moderately use lab work Observations for mathematical calculations	Fully use lab work observations for mathematical calculations
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Equipment Handling equipment care during the use	Doesn't handle Equipment with required care	Rarely handles equipment with required care	Occasionally handles Equipment with required care	Often handles Equipment with required care	Handles equipment with required care
Ability to troubleshoot errors and try to resolve with/without the supervision or guidance	Unable to troubleshoot experimentation errors and resolve them	Able to troubleshoot experimentation errors but cannot resolve them	Able to troubleshoot experimentation errors and resolve them under supervision	Able to troubleshoot experimentation errors independently but need guidance in resolving them	Able to troubleshoot experimentation errors and resolve them without supervision or guidance

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 12

Objective:

To illustrate the operation of Common Source Amplifier and also determine phase shift between input and output

Equipment Required:

- Protoboard
- Function Generator
- Digital Multimeter
- Power Supply
- Resistors
- Transistors: 1 x 2N7000
- Capacitors

Theory:

Common source FET amplifier circuit is one of the most commonly used providing current and voltage gain along with a satisfactory input and output impedance.

Common source FET configuration is probably the most widely used of all the FET circuit configurations for many applications, providing a high level of all round performance.

The common source circuit provides a medium input and output impedance levels. Both current and voltage gain can be described as medium, but the output is the inverse of the input, i.e. 180° phase change. This provides a good overall performance and as such it is often thought of as the most widely used configuration.

Common Source Amplifier:

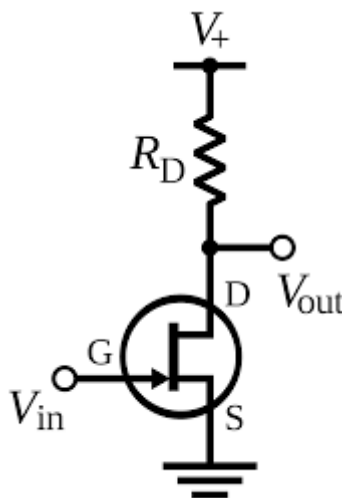


Fig 5: Common Source Amplifier

Hence Common Source amplifiers have:

- ☐ Inverting output
- ☐ High input resistance
- ☐ Moderately high voltage gain
- ☐ Large output resistance

Procedure:

Implement a common-source amplifier, as shown in Figure 6 . Note the 100 μ F AC coupling capacitor at the input, and the 100 μ F bypass capacitor on the gate; the latter makes the gate an AC ground, appropriate to the common-gate configuration.

- ☐ Construct the circuit in circuit Figure 6. Be sure to use the correct polarity for the coupling capacitors, or the circuit may not function properly.
- ☐ With the power supply on, the function generator connected to the input port, and the oscilloscope set to observe the input voltage V_{in} , adjust the amplitude of the function generator such that V_{in} is a 10mV sinusoid at 1kHz. Then measure and record the AC voltage gain V_{out} / V_{in}

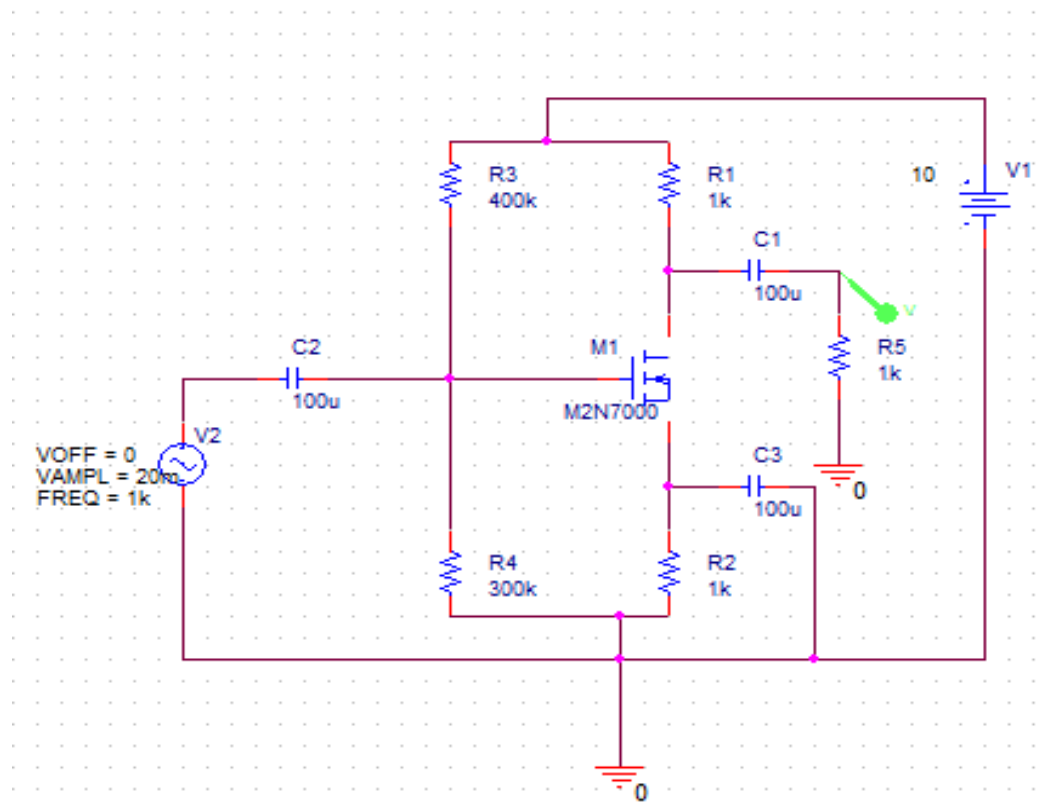


Fig 2: common source amplifier (practical circuit)

Analysis:

Determine the gate , drain and source voltage . perform all necessary calculations .Let $V_t = 1\text{ V}$.
justify that the circuit can be used as an amplifier

Observations:

1. DC analysis

Parameters	Measured value	Expected value
V_G		
V_S		
V_D		

2. AC Analysis (Apply 20mV peak to peak sinusoidal input from function generator, measure output voltage)

$V_{out}(\text{with load resistor})$	$V_{out}(\text{without load resistor})$

3. Determine voltage gain

4. Draw input and output voltage waveform

Results:

The gain of the common source amplifier with load is: _____

The gain of the common source amplifier without load is: _____

The phase shift between input and output signal of common source amplifier is _____.

LAB SESSION 13

To illustrate the operation of Common Gate Amplifier and also determine phase shift between input and output

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Skill Sets	Psychomotor Domain Assessment Rubric-Level P3				
	Extent of Achievement				
	0	1	2	3	4
Equipment Identification Sensual ability to identify equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
Procedural Skills Displays skills to act upon sequence of steps in lab work	Unable to either learn or perform lab work procedure	Able to slightly understand lab work procedure and perform lab work	Able to somewhat understand lab work procedure and perform lab work	Able to moderately understand lab work procedure and perform lab work	Fully understands lab work procedure and perform lab work
Response Capability to imitate the lab work on his/her own	Unable to imitate the lab work	Able to slightly imitate the lab work	Able to somewhat imitate the lab work	Able to moderately imitate the lab work	Fully imitates lab work
Observation's Use Displays skills to perform related mathematical calculations using the observations from lab work	Unable to use lab work observations for mathematical calculations	Able to slightly use lab work observations for mathematical calculations	Able to somewhat use lab work Observations for mathematical calculations	Able to moderately use lab work Observations for mathematical calculations	Fully use lab work observations for mathematical calculations
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Ability to troubleshoot errors and try to resolve with/without the supervision or guidance	Unable to troubleshoot experimentation errors and resolve them	Able to troubleshoot experimentation errors but cannot resolve them	Able to troubleshoot experimentation errors and resolve them under supervision	Able to troubleshoot experimentation errors independently but need guidance in resolving them	Able to troubleshoot experimentation errors and resolve them without supervision or guidance

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 13

Objective:

To illustrate the operation of Common Gate Amplifier and also determine phase shift between input and output

Equipment Required:

- Protoboard
- Function Generator
- Digital Multimeter
- Power Supply
- Resistors
- Transistors: 1 x 2N7000
- Capacitors

Theory:

MOS transistor is a voltage controlled device, where gate voltage modulates the channel resistance and voltage between drain and source determines current flow between the drain and source terminals. Like BJT, MOS transistor can perform as amplifier and as electronic switch. MOS comes in two different flavors, as NMOS and as PMOS.

Small-Signal Amplifier Design and Biasing

If a small time-varying signal is superimposed on the DC bias at the input (gate or base terminal), then under the right circumstances the transistor circuit can act as a linear amplifier. Figure 1 illustrates the situation appropriate to a MOSFET common-source amplifier. The transistor is first biased at a certain DC gate bias to establish a desired drain current, shown as the “Q”-point (quiescent point) Figure 1a. A small AC signal of amplitude ΔV_{gs} is then superimposed on the gate bias, causing the drain current to fluctuate synchronously. If ΔV_{gs} is small enough, then we can approximate the I_d vs. V_{gs} curve by a straight line with a slope given by

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \quad (1)$$

and then the drain current amplitude is $\Delta I_d = g_m \Delta V_{gs}$. With a drain resistor R_d as shown, the drain current is related to the output voltage by $V_{ds} = V_{dd} - I_d R_d$, so the AC output signal will be given by

$$\Delta V_{ds} = -\Delta I_d R_d = -g_m R_d \Delta V_{gs} \quad (2)$$

The voltage gain is therefore $A_v = -g_m R_d$. This can be appreciated graphically using a load-line approach as in Figure 1b.

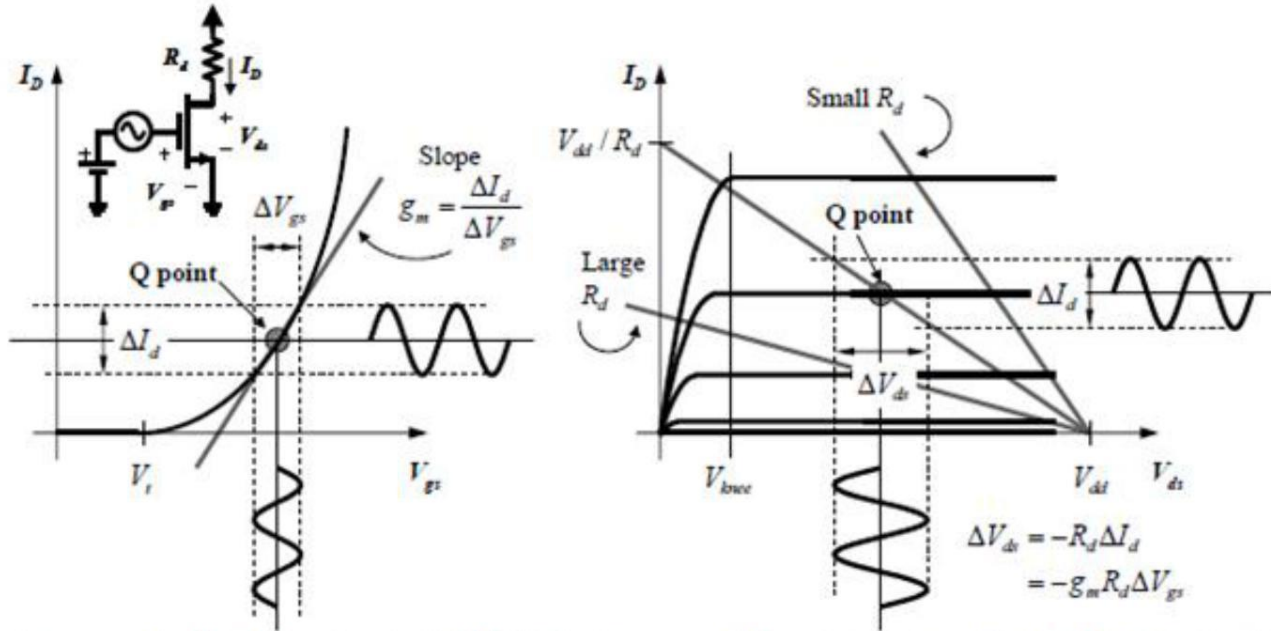


Figure 1 – Amplification in a MOSFET common-source configuration. (a) A small AC signal is superimposed on the DC gate bias, creating an AC drain current. (b) Same situation with a load-line superimposed on the output characteristic, showing how the AC drain current leads to an AC drain voltage and gain of $-g_m R_d$.

Figure 1 also illustrates the importance of the bias point selection in the operation of transistor amplifiers. Figure 1a shows that the transconductance (and hence the gain) will depend on the gate bias; this can be quantified using the I_d vs. V_{gs} characteristic

$$I_m = K_n (V_{gs} - V_t)^2 \quad (3)$$

Substituting (3) into (1) gives

$$g_m = 2K_n (V_{gs} - V_t) = 2\sqrt{K_n I_d} = \frac{2I_d}{(V_{gs} - V_t)} \quad (4)$$

To establish a large transconductance we must bias the device well above threshold. This is also important to insure that the transistor stays in saturation over the full AC cycle. However, there is a limit on gate bias and drain current imposed by the output characteristic and load resistor as shown in Figure 1b. To allow for maximum output voltage swing the Q-point should lie approximately halfway between V_{dd} and the edge of the ohmic region, shown in the figure as V_{knee} . If the drain current or load resistor is too large, the device will swing into the ohmic region during operation leading to significant waveform distortion.

Another important consideration is the DC power dissipation in the device given by $P = V_{ds} I_d$. This power is dissipated as heat within the device so there is always a thermal limit on the dissipated power for every device and package. The datasheet will specify the maximum DC power P_{max} , maximum DC current I_{dmax} , and maximum DC voltage V_{dsmax} , to avoid

destroying the device. These limits are superimposed on the output characteristic in Figure 2. The Q-point must be selected to lie below the shaded region in the figure.

Although the focus has been on MOSFETs in this discussion, it is important to recognize that the key conclusions above are largely independent of the choice of device. All transistors can be described by an output-current versus input-voltage characteristic like that in Figure 2-1a, and hence by a bias-dependent transconductance. Only the details of the voltage dependence will be different. For example, BJTs follow a diode-like exponential model; state-of-the-art short-channel MOSFETs have a nearly linear I_d vs. V_{gs} characteristic and hence a constant g_m .

Lastly, note that the supply voltage is also an important variable. Generally a larger supply voltage is desirable for maximum voltage gain and maximum output voltage swing. This can be seen as follows: for a given drain current I_d , the drain resistor that is required for a drain bias of $V_{ds} \approx V_{dd} / 2$ is

$$R_d = \frac{V_{dd} - V_{ds}}{I_d} \approx \frac{V_{dd}}{2I_d} \quad (5)$$

and thus the gain is given by

$$|A_v| = g_m R_d \approx \frac{g_m V_{dd}}{2I_d} = V_{dd} \sqrt{\frac{K_n}{I_d}} \quad (6)$$

The maximum gain scales with supply voltage for a specified device and current level.

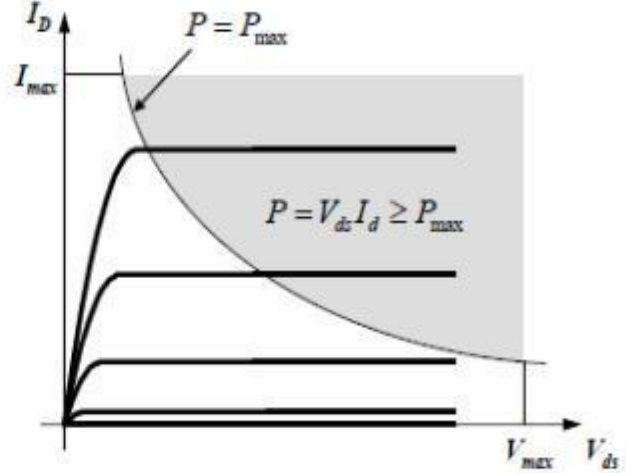


Figure 2 – Limitations on biasing imposed by maximum power considerations.

MOSFET Design Parameters and Subthreshold Currents

For amplifier designs using any transistor (MOSFETs or BJTs) we need to know the transconductance g_m . For MOSFETs, a knowledge of the threshold voltage V_t and the current parameter K_n can be used to estimate g_m using (4), *assuming the square-law device model (3) holds*. A common method to estimate these parameters is to measure and plot the square-root of I_d versus V_{gs} , which theoretically should yield a linear dependence,

$$\sqrt{I_d} = \sqrt{K_n} (V_{gs} - V_t) \quad (7)$$

Thus the x-intercept if such a plot should yield the threshold voltage, and the slope should yield the current parameter.

The 2N7000, also in your parts kit, is at the other extreme: it is intended for larger currents and has an inherently larger transconductance. Consequently we need to operate this device closer to threshold in order to keep the DC currents low, an imperative from a DC power-dissipation standpoint. The data sheet specifies a maximum DC power dissipation of 400mW; for drain voltages in the range of 2.5-5V (appropriate to supply voltages in the range of 5-10V) we would need to keep the currents below ~100mA.

Figure 3 shows a measured plot of I_d vs. V_{gs} for a 2N7000 for currents in this range; on this scale we can see a significant departure from the square-law characteristic. This device has gate lengths of around 2.5 μ m.

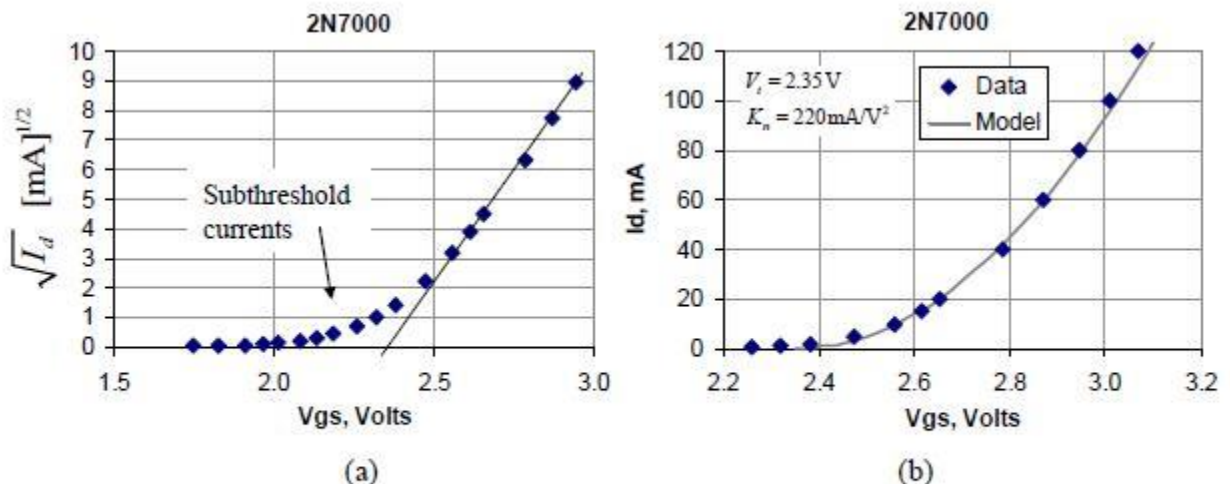


Figure 3 – (a) Data for a 2N7000 device plotted as $\sqrt{I_d}$ vs. V_{gs} , showing sub-threshold currents. (b) Same data set plotted as I_d vs. V_{gs} , with comparison to the ideal model using given parameters (dashed line)

Is this a problem? No, it just means that we can't expect (3) to work well below currents of around 10mA. Above 10mA, the model seems to work reasonably well, and for the particular device shown in Figure 3 we find $V_t \approx 2.35\text{ V}$ and $K_n \approx 220\text{ mA/V}^2$.

Remember, these parameters vary from device to device, and also may vary considerably from manufacturer to manufacturer. Figure 4 shows a comparison of characteristic from four different 2N7000 devices, two from one manufacturer, and two from another manufacturer, selected randomly. Not only does the threshold voltage vary, but it is apparent that the current parameter K_n also varies between manufacturers.

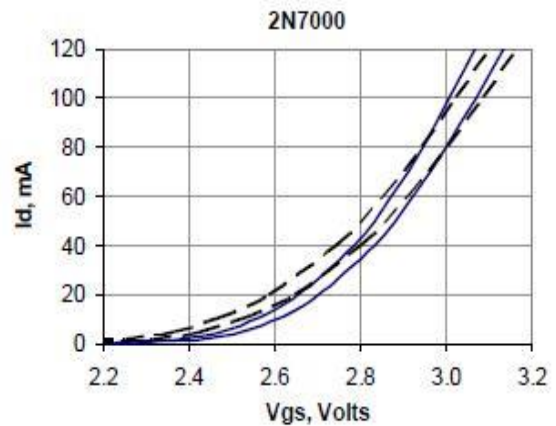


Figure 4 – Comparison of four different 2N7000 devices. Dashed lines and solid lines represent different manufacturers.

Frankly the 2N7000 isn't a great choice for small-signal linear amplifier designs, it is really intended for use in power switching circuits. You might wonder why we chose the 2N7000 for this experiment. The simple answer: it is cheap and ubiquitous, a common theme for components used in AIC labs!

The simple answer: it is cheap and ubiquitous, a common theme for components used in AIC labs!

Common Gate Amplifier:

As shown in figure 5 the common gate amplifier has a grounded gate terminal, a signal input at the source terminal and the output taken at the drain.

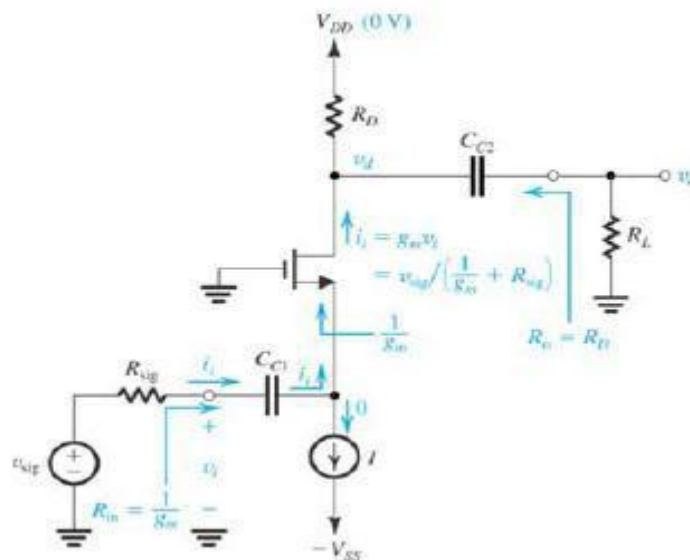


Fig 5: Common Gate Amplifier

Hence Common Gate amplifiers have

- Non-Inverting output
- Moderate input resistance
- Moderately large small signal voltage gain but smaller than common source amplifier.
- Small signal current gain less than one.
- Potentially large output resistance (Dependent on R_D)

Procedure:

- Implement a common-source amplifier, as shown in Figure 6 . Note the 100 μ F AC coupling capacitor at the input, and the 100 μ F bypass capacitor on the gate; the latter makes the gate an AC ground, appropriate to the common-gate configuration.
- Construct the circuit in circuit Figure 6. Be sure to use the correct polarity for the coupling capacitors, or the circuit may not function properly.
- With the power supply on, the function generator connected to the input port, and the oscilloscope set to observe the input voltage V_{in} , adjust the amplitude of the function generator such that V_{in} is a 10mV sinusoid at 1kHz. Then measure and record the AC voltage gain V_{out} / V_{in}

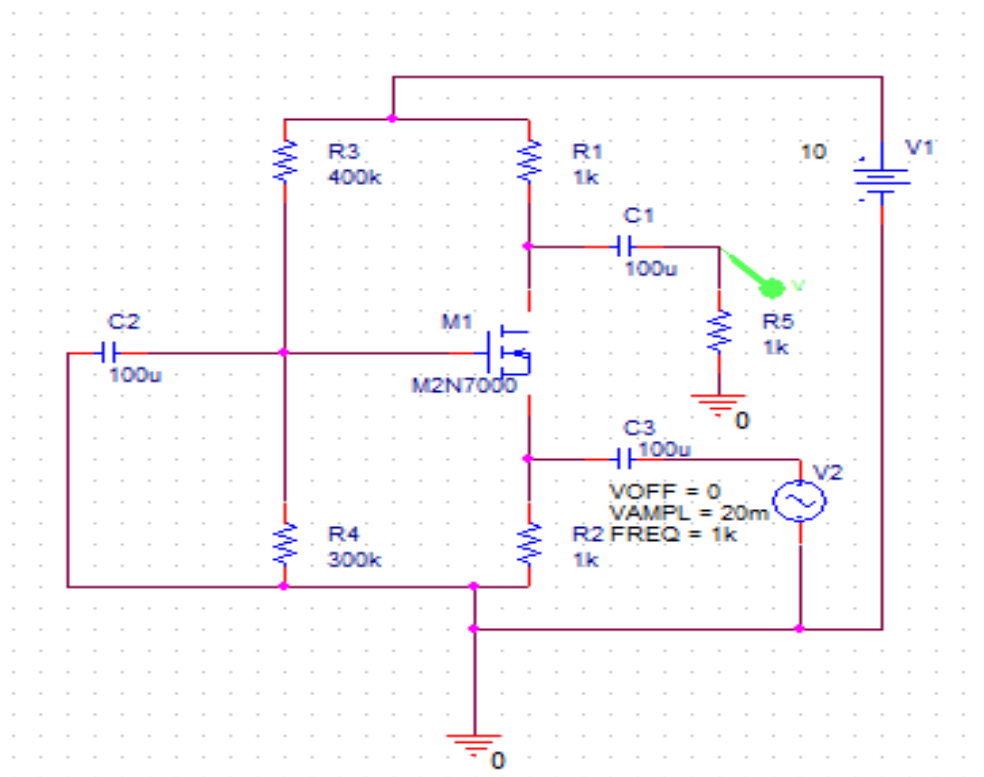


Fig 6: common gate amplifier (practical circuit)

Analysis:

Determine the gate , drain and source voltage . perform all necessary calculations .Let $V_t = 1\text{ V}$.
justify that the circuit can be used as an amplifier

Observations:

1. DC analysis

Parameters	Measured value	Expected value
V_G		
V_S		
V_D		

2. AC Analysis (Apply 20mV peak to peak sinusoidal input from function generator, measure output voltage)

$V_{out}(\text{with load resistor})$	$V_{out}(\text{without load resistor})$

3. Determine voltage gain

4. Draw input and output voltage waveform

Results:

The gain of the common gate amplifier with load is: _____

The gain of the common gate amplifier without load is: _____

The phase shift between input and output signal of common gate amplifier is _____.

LAB SESSION 14

To illustrate the operation of Simple MOS Mirror

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____
 Laboratory Session No. _____ Date: _____

Skill Sets	Psychomotor Domain Assessment Rubric-Level P3				
	Extent of Achievement				
	0	1	2	3	4
Equipment Identification Sensual ability to identify equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
Procedural Skills Displays skills to act upon sequence of steps in lab work	Unable to either learn or perform lab work procedure	Able to slightly understand lab work procedure and perform lab work	Able to somewhat understand lab work procedure and perform lab work	Able to moderately understand lab work procedure and perform lab work	Fully understands lab work procedure and perform lab work
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 14

Objective:

To illustrate the operation of Simple MOS Mirror

Equipment Required:

- Protoboard
- Function Generator
- Digital Multimeter
- Power Supply
- Resistors
- Transistors: 1 x 2N7000
- Capacitors

Theory:

Focus initially on N-MOS transistor Q1 which is connected in the so-called “diode connection.” That is, the drain and gate are shorted together so that the drain node is at the same potential as the gate. Hence, the drain-to-source voltage is equal to the gate-to-source voltage (i.e., $V_{DS} = V_{GS}$). From the theory of the MOSFET, we know that V_{GS} must exceed the threshold voltage V_t of the FET for drain current to flow. The characteristic curve for the “diode connection” is shown below. [Reference: Figure 5.14 on page 268 of Sedra & Smith.]

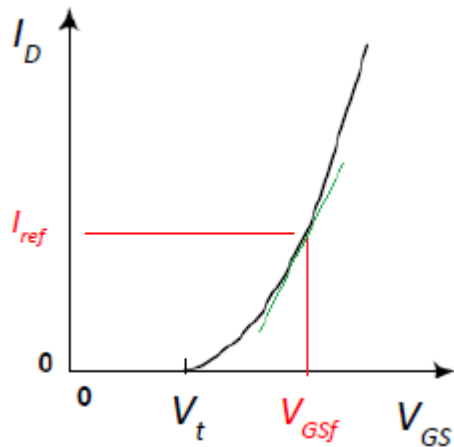


Fig 1. I_D Vs V_{GS} curve

The goal for a current mirror is to establish a stable I_{ref} value and then to mirror (or replicate) current I_{ref} in other branches of the circuit. In other words, we want I_O to equal I_{ref} regardless of the applied value of V_{DS} of the mirroring transistor. This assumes identical transistor geometries of course. What causes a

current mirror to deviate from $I_{ref} = I_0$? An error or deviation can result from (1) the mirroring transistor's finite output drain-to-source resistance r_0 , (2) a parametric mismatch between transistors Q1 and Q2, and (3) a temperature difference between transistors Q1 and Q2. In integrated circuits the transistors are physically close together for thermal matching and they are fabricated simultaneously on the same wafer. So, they should be well matched and thermally coupled as well as physically possible.

Let us analyze how a finite output resistance causes I_0 to deviate from I_{ref} . To do this we write the equations for the drain currents of transistors Q1 & Q2. These equations are

$$I_{ref} = \frac{1}{2} \mu_n \left(\frac{W}{L} \right)_1 (V_{GS} - V_t)^2 \times (1 + \lambda V_{DS1}); \text{ where } V_{DS1} = V_{GS} \text{ in } Q_1$$

$$I_0 = \frac{1}{2} \mu_n \left(\frac{W}{L} \right)_2 (V_{GS} - V_t)^2 \times (1 + \lambda V_{DS2})$$

$$\frac{I_0}{I_{ref}} = \frac{(W/L)_2 \times (1 + \lambda V_{DS2})}{(W/L)_1 \times (1 + \lambda V_{GS})}$$

Select Value of Resistor R_{ref} :

To set the value of resistor R_{ref} requires knowing the reference current I_{ref} — for our experiment we choose 3 mA. Thus, R_{ref} can be determined from 3 mA ($R_{ref} = V_{DD} - V_{GS}$). Let $V_{GS} = 2V$. Thus, you will want to compensate for this in adjusting the reference current to 3mA (assume we want to set it to better than a 2% error from the 3 mA target value).

For the range of load resistances provided measure the new I_0 in each case.

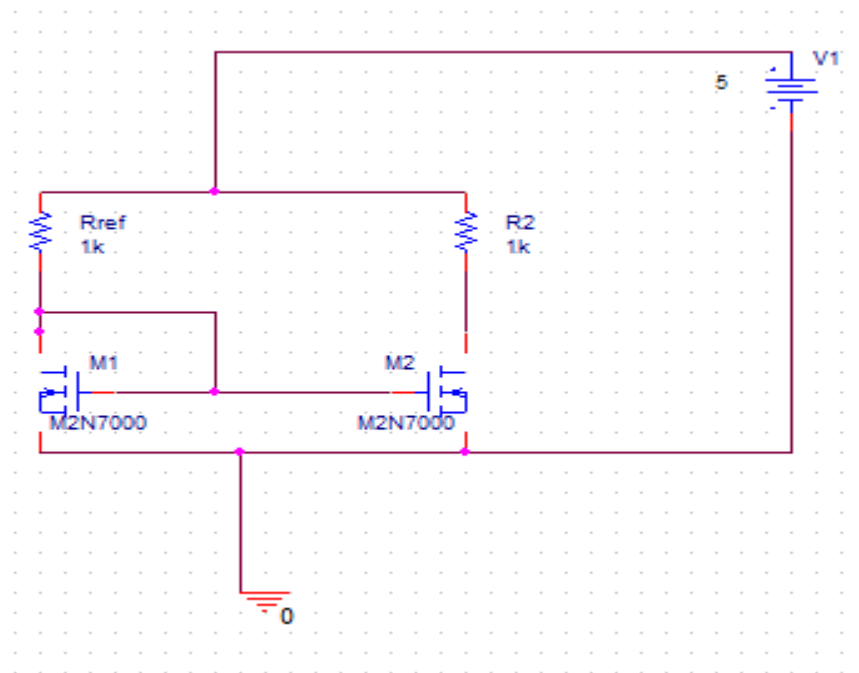


Fig.2 Simple MOS Mirror

Procedure:

- Implement the circuit in figure 2 for Simple MOS Mirror.
- Vary R_2 & observe readings for I_{ref} & I_o .

S. No	I_{ref}	I_o
1		
2		
3		
4		
5		
6		

Calculations:

Make calculation of I_o for the observed value of I_{ref} . Also calculate the percentage error.

Result:

OPEN-ENDED LAB

You are required to design an active loaded Wilson BJT current source having a current of 5mA. You are required to change the base resistance of the active load from the roll numbers of your group ranging from ohm to kohm. Incase you have less than 5 group members you use any large variant resistance to complete the count of 5 base resistances. Use +6 and -6 Volts supply.

Student Name: _____

Roll no.: _____ **Batch:** _____

Semester : _____ **Year:** _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ **Date:** _____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Skill Sets	Psychomotor Domain Assessment Rubric-Level P3				
	Extent of Achievement				
	0	1	2	3	4
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

OPEN-ENDED LAB

Objective:

You are required to design an active loaded Wilson BJT current source having a current of 5mA. You are required to change the base resistance of the active load from the roll numbers of your group ranging from ohm to kohm. In case you have less than 5 group members you use any large variant resistance to complete the count of 5 base resistances. Use +6 and -6 Volts supply.