PRACTICAL WORK BOOK

For Academic Session 2014

ELECTRONIC DEVICES & CIRCUITS
(EL-231) For S.E(EL)

Name: _____

Roll Number: _____

Class: _____

Batch: _____

Department : _____

Department of Electronic Engineering

NED University of Engineering & Technology, Karachi

LABORATORY WORK BOOK

FOR THE COURSE

EL -231 Electronic Devices & Circuits

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Lab Session 01

OBJECTIVES

To investigate the Inverting Amplifier i.e.

To determine the phase shift between the input and output signals.

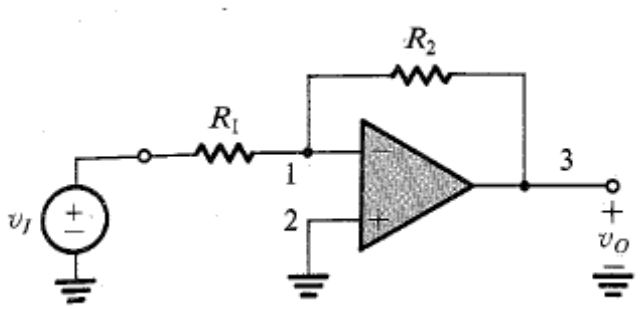
To measure the frequency response of an op amp and demonstrate the effect of negative feedback

EQUIPMENT REQUIRED:

Protoboard
741 Opamps
Resistors
Digital Multimeter
Function Generator
Oscilloscope

Theory:

Figure shows the inverting configuration. It consists of one opamp & two resistors R1 & R2. R2 is connected frpm output terminal back to inverting or inverting input terminal. If R2/R1 =10, & we apply the sine wave input of 1V pk-pk, output will be a sine wave of 10V pk-pk, & phase shifted 180^o



Observations:

S.No	Frequency	Input (p-p)	Output (p-p)	Gain
1 1k				
2				
3				
4				
5 10k				
6				
7				
8				
9 100k				
10				
11				
12				

Calculations:

Calculated Gain:

$$G=Vo/Vi=-(R2/R1)$$

Lab Session 02

OBJECTIVES

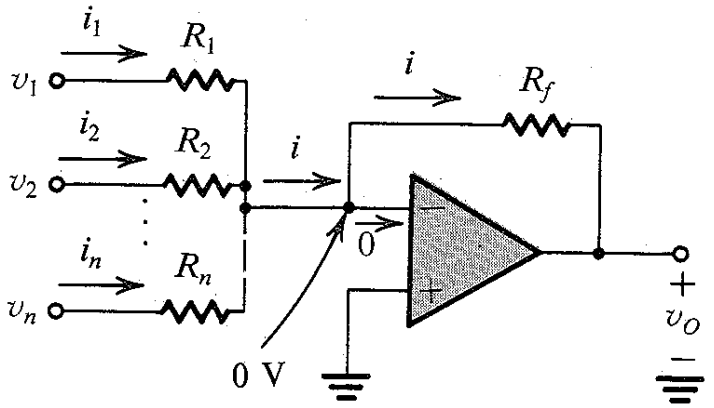
To investigate the Weighted Summer Operation

EQUIPMENT REQUIRED:

Protoboard
741 Opamps
Resistors
Digital Multimeter
Function Generator
Oscilloscope

THEORY:

Figure shows that there are number of input signals, V1, V2 ……. Vn each applied to a corresponding resistor R1, R2, …….Rn, which are connected to inverting terminal of Opamp
Output is the weighted sum of the input signals V1, V2……. Vn. Each summing coefficient may be independently adjusted using R1, R2…….Rn



$$v_O = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \cdots + \frac{R_f}{R_n}v_n\right)$$

OBSERVATIONS:

S. No	INPUT SIGNALS		OUTPUT	Gain
	V1 (p-p)	V2 (p-p)	p-p	
1				
2				
3				
4				
5				

CALCULATIONS:

Calculated Gain:

Lab Session 03

OBJECTIVES

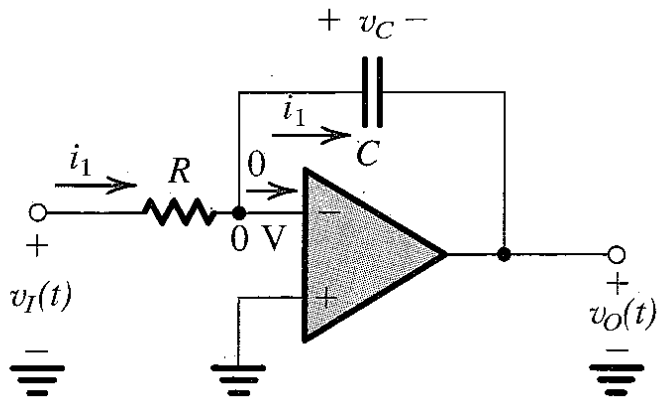
To investigate the Operation of Inverting Integrator

EQUIPMENT REQUIRED:

Protoboard
741 Opamps
Resistors, Capacitors
Digital Multimeter
Function Generator
Oscilloscope

THEORY:

By placing the capacitor in the feedback path, and resistor at the input realizes the mathematical operation of integration.



OBSERVATIONS:

S. No	Frequency	Input (p-p)	Output (p-p)	Gain
1 1k				
2				
3				
4				
5 10k				
6				
7				
8				
9 100k				
10				
11				
12				

CALCULATIONS:

The integrating frequency according to the values of C & R is:

Lab Session 04

OBJECTIVES

To investigate the Operation of BJT Current Mirror.

EQUIPMENT REQUIRED:

Protoboard
Q2N2222 BJT npn transistors
Resistors, Capacitors
Digital Multimeter
Function Generator
Oscilloscope
Connecting wires

THEORY:

The basic BJT Current Mirror is shown in figure. Neglecting base current, the reference current Iref is passes through the diode connected transistor Q1, & thus produces corresponding voltage Vbe, which in turn is applied between base & emitter of Q2. If Q2 is matched to Q1, then the collector current of Q1 is equal to that of Q1

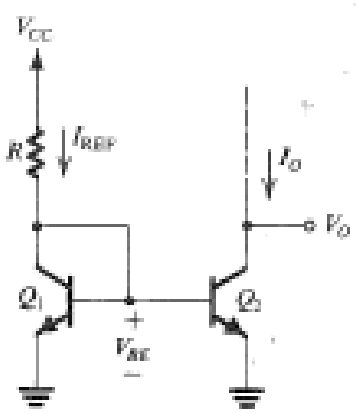


FIGURE 1

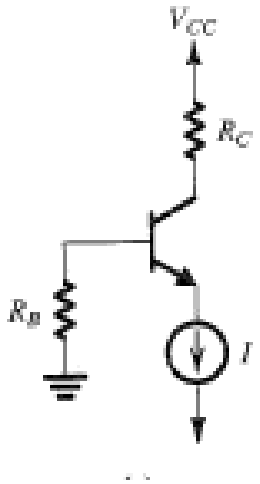


FIGURE 2

PROCEDURE:

- Implement the circuit given in figure 2, using current source in figure 1.
- Vary the potentiometer and observe changes in Iref and Io

OBSERVATIONS:

S. No	Iref	Io
1		
2		
3		
4		
5		
6		
7		
8		

CALCULATIONS:

Lab Session 05

OBJECTIVES

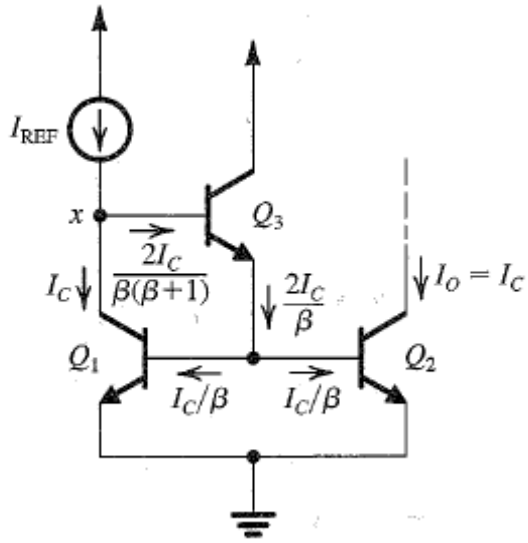
To illustrate the operation of current source implemented using BJT, with Base-Current Compensation.

EQUIPMENT REQUIRED:

Protoboard
Q2N2222 BJT npn transistors
Resistors, Capacitors
Digital Multimeter
Function Generator
Oscilloscope
Connecting wires

THEORY:

Figure shows a bipolar current mirror with a current transfer ratio that is much less dependent on β than that of simple current mirror. The reduced dependence is achieved by using transistor Q3



PROCEDURE:

- Implement the circuit in figure 2 of previous lab session using above current source, using potentiometer in place of Iref
- Vary potentiometer & observe readings for Iref & Io

OBSERVATIONS:

S. No	Iref	Io
1		
2		
3		
4		
5		
6		
7		
8		

CALCULATIONS:

Lab Session 06

OBJECTIVES

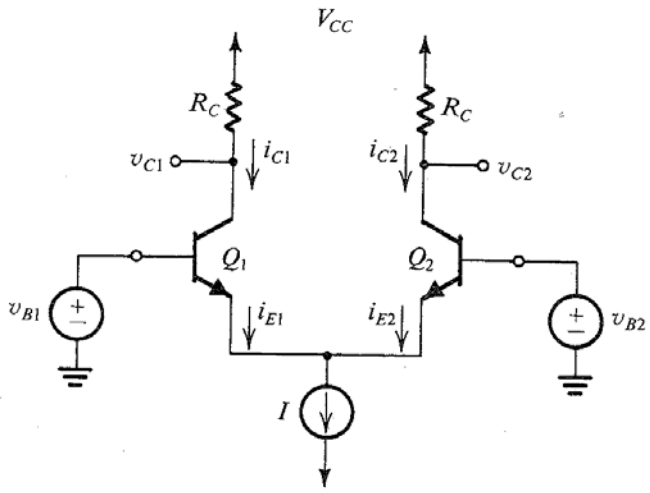
To illustrate the operation of BJT Differential Pair
As a Swith
As an Amplifier

EQUIPMENT REQUIRED:

Protoboard
Q2N2222 BJT npn transistors
Resistors, Capacitors
Digital Multimeter
Function Generator
Oscilloscope
Connecting wires

THEORY:

It consists of two matched transistors, Q1 & Q2, whose emitters are joined together and biased by constant current source I. It is essential that, collector circuits be such that Q1 & Q2 never enter saturation.



OBSERVATIONS:

S.NO V B1	VB2 VB1-VB2 Vc1	Vc2 Vc1-Vc2			
1					
2					
3					
4					
5					
6					
7					
8					

RESULTS:

Lab Session 07

OBJECTIVES

To illustrate the operation of Wilson MOS Mirror

EQUIPMENT REQUIRED:

Protoboard
MOSFET
Resistors, Capacitors
Digital Multimeter
Function Generator
Oscilloscope
Connecting wires

THEORY:

Figure 1 shows the Wilson MOS Mirror. Advantage of MOS Wilson lies in its enhanced output resistance. To balance the two branches of the mirror, and to avoid systematic current error resulting from the difference between Q1 & Q2, other two transistors Q3 & Q4 connected.

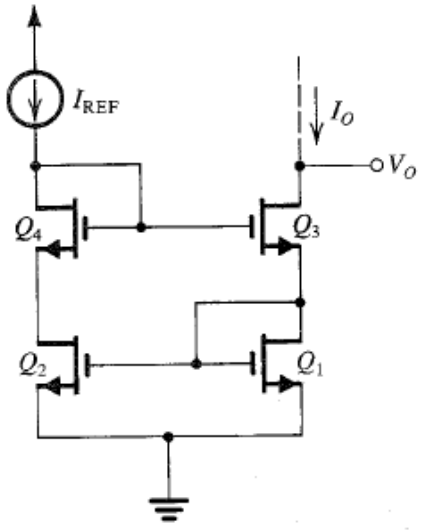
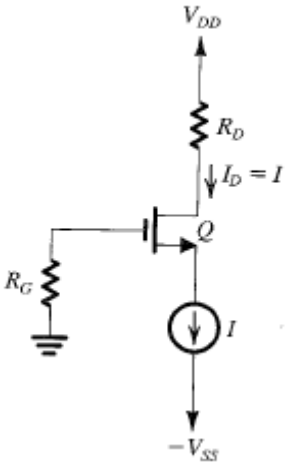


FIGURE 1



PROCEDURE:

- Implement the circuit in figure 2 using MOS Wilson current Mirror as that in figure 1, using potentiometer in place of Iref
- Vary potentiometer & observe readings for Iref & Io

OBSERVATIONS:

S. No	Iref	Io
1		
2		
3		
4		
5		
6		
7		
8		

CALCULATIONS:

Lab Session 08

OBJECTIVES

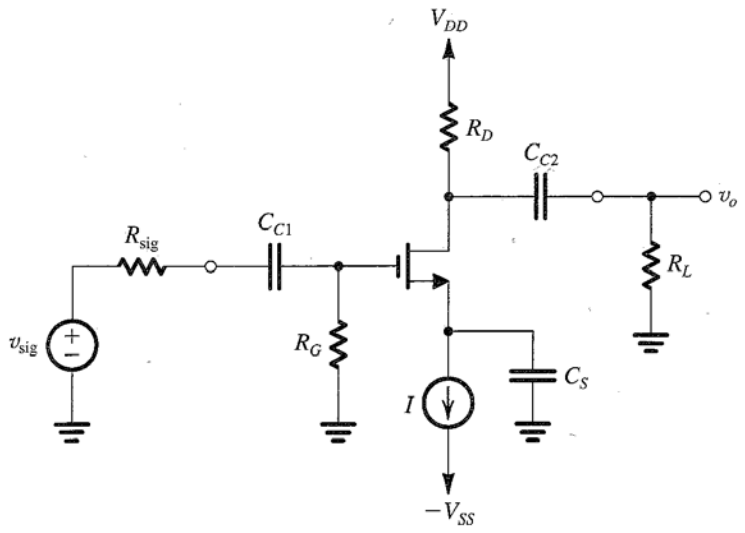
To illustrate the operation of Common Source Amplifier and also determine phase shift between input and ouput.

EQUIPMENT REQUIRED:

Protoboard
Q2N2222 BJT npn transistors
Resistors, Capacitors
Digital Multimeter
Function Generator
Oscilloscope
Connecting wires

THEORY:

A Common Source Amplifier or Grounded Source Configuration is shown in figure. To establish a signal ground, or ac ground, a large capacitor is connected between source & ground. The signal current bypasses the output resistance of the current source & is called a bypass Capacitor. Cc1 is known as Coupling Capacitor, & acts as a perfect short circuit at all signal frequencies of interest.



OBSERVATIONS:

S.No	Frequency	Input (p-p)	Output (p-p)	Gain
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				

CALCULATIONS:

Calculated Gain:

Lab Session 09

OBJECTIVES

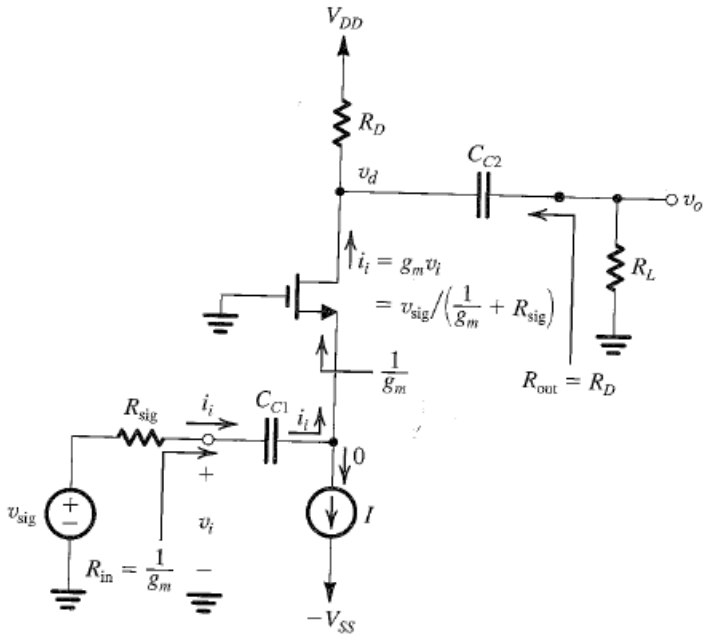
To illustrate the operation of Common Gate Amplifier.

EQUIPMENT REQUIRED:

Protoboard
MOSFET
Resistors, Capacitors
Digital Multimeter
Function Generator
Oscilloscope
Connecting wires

THEORY:

By establishing a signal ground on the MOSFET gate terminal, a circuit configuration called Common Gate is obtained. The input is applied to the source and output is taken at the drain terminal, with gate being the common terminal between input & output ports.



OBSERVATIONS:

S.No	Frequency	Input (p-p)	Output (p-p)	Gain
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				

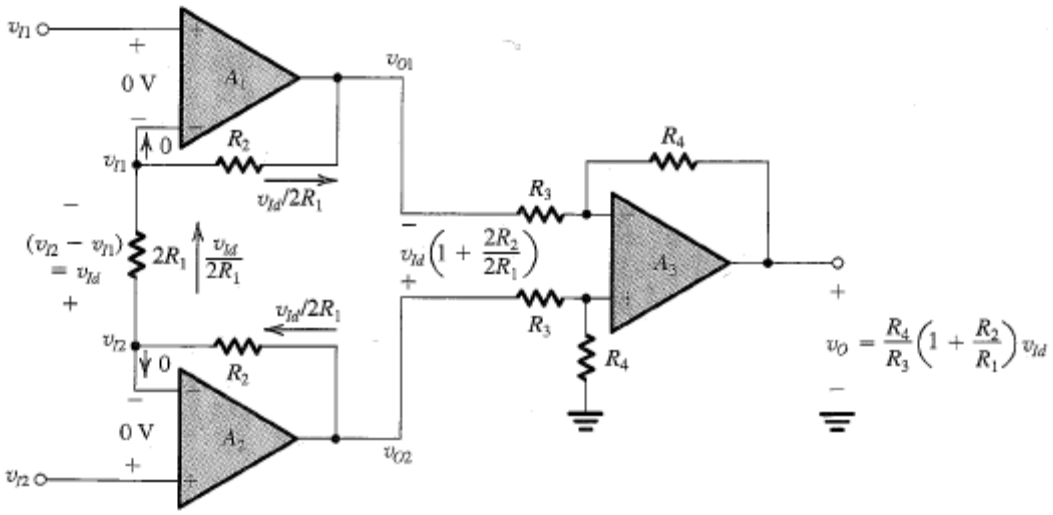
CALCULATIONS:

Calculated Gain:

Lab Session 10

PROJECT # 1

To illustrate the operation of Instrumentation Amplifier

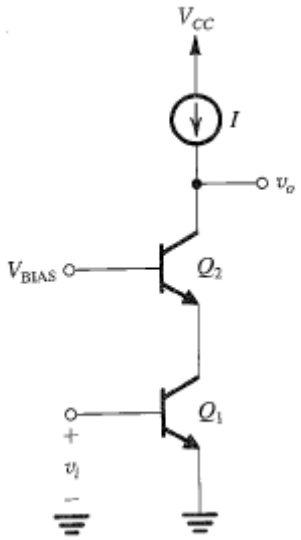


Lab Session 11

PROJECT # 2

To illustrate the operation of BJT Cascode Configuration and thus find:

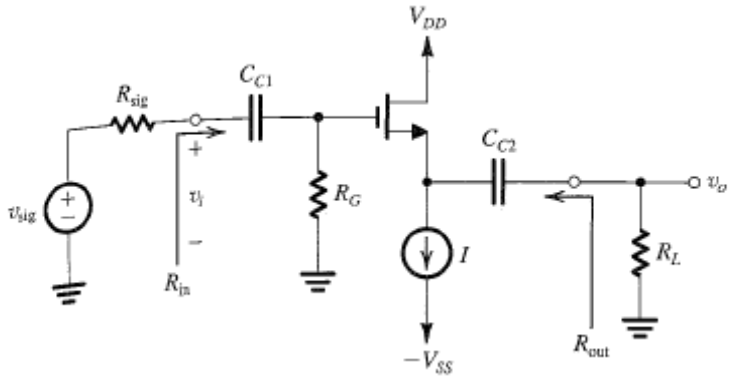
1. Gain
2. Frequency Response



Lab Session 12

PROJECT # 3

To illustrate the operation of Common Drain Amplifier



Lab Session 13

OBJECTIVES:

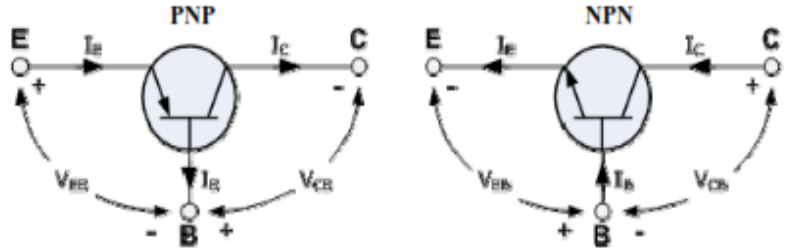
(i) To study the input and output characteristics of a PNP transistor in Common Base mode and determine transistor parameters.
(ii) To study the input and output characteristics of an NPN transistor in Common Emitter mode and determine transistor parameters.

EQUIPMENT REQUIRED:

(i)Transistors (2 Nos: 1 PNP (CK 100 or equivalent) and 1 NPN (BC 107 or equivalent)),(ii)Resistors (4 Nos.) (iii) Multimeters (3 Nos.), (iv) D.C. power supply, (v) Connecting wires and (vi) Breadboard.

BASIC THEORY:

A **Bipolar Junction Transistor** or **BJT** is a three terminal device having two PN- junctions connected together in series. Each terminal is given a name to identify it and these are known as the Emitter (E), Base (B) and Collector (C). There are two basic types of bipolar transistor construction, NPN and PNP, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. Bipolar Transistors are "CURRENT" Amplifying or current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing current applied to their base terminal. The principle of operation of the two transistors types NPN and PNP, is exactly the same the only difference being in the biasing (base current) and the polarity of the power supply for each type.



The symbols for both the NPN and PNP bipolar transistor are shown above along with the direction of conventional current flow. The direction of the arrow in the symbol shows current flow between the base and emitter terminal, pointing from the positive P-type region to the negative N-type region, exactly the same as for the standard diode symbol. For normal operation, the emitter-base junction is forward-biased and the collector-base junction is reverse-biased.

Transistor Configurations:

There are three possible configurations possible when a transistor is connected in a circuit: (a) Common base, (b) Common emitter (c) Common collector. We will be focusing on the first two configurations in this experiment. The behavior of a transistor can be represented by d.c. current-voltage (I-V) curves, called the static characteristic curves of the device. The three important characteristics of a transistor are: (i) Input characteristics, (ii) Output characteristics and (iii) Transfer Characteristics. These characteristics give information about various transistor parameters, e.g. input and out dynamic resistance, current amplification factors, etc.

Common Base Transistor Characteristics

In common base configuration, the base is made common to both input and output as shown in its circuit diagram.

(1) Input Characteristics: The input characteristics is obtained by plotting a curve between I_E and V_{EB} keeping voltage V_{CB} *constant*. This is very similar to that of a forward-biased diode and the slope of the plot at a given operating point gives information about its input dynamic resistance.

Input Dynamic Resistance (ri): This is defined as the ratio of change in base emitter voltage (ΔV_{EB}) to the resulting change in base current (ΔI_E) at constant collector-emitter voltage (V_{CB}). This is dynamic as its value varies with the operating current in the transistor.

$$r_i = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB}}$$

(2) Output Characteristics: The output characteristic curves are plotted between I_C and V_{CB}, keeping I_E constant. The output characteristics are controlled by the input characteristics. Since I_C changes with I_E, there will be different output characteristics corresponding to different values of I_E. These curves are almost horizontal. This shows that the output dynamic resistance, defined below, is very high.

Output Dynamic Resistance (r o): This is defined as the ratio of change in collector-emitter voltage (ΔV_{CB}) to the change in collector current (ΔI_C) at a constant base current I_E.

$$r_o = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E}$$

(3) Transfer Characteristics: The transfer characteristics are plotted between the input and output currents (I_E versus I_C).

Current amplification factor (α): This is defined as the ratio of the change in collector current to the change in emitter current at a constant collector-base voltage (V_{CB}) when the transistor is in active state.

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}}$$

This is also known as small signal current gain and its value is very large. The ratio of I_C and I_E is called α_{dc} of the transistor. Hence,

$$\alpha_{dc} = \left.\frac{I_C}{I_E}\right|_{V_{CB}}$$

Since I_C increases with I_E almost linearly, the values of both α_{dc} and α_{ac} are nearly equal.

Common Emitter Transistor Characteristics

In a common emitter configuration, emitter is common to both input and output as shown in its circuit diagram.

(1) Input Characteristics: The variation of the base current I_B with the base-emitter voltage V_{BE} keeping the collector-emitter voltage V_{CE} fixed, gives the input characteristic in CE mode.

Input Dynamic Resistance (ri): This is defined as the ratio of change in base emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). This is dynamic and it can be seen from the input characteristic, its value varies with the operating current in the transistor:

$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}}$$

The value of r_i can be anything from a few hundreds to a few thousand ohms.

(2) Output Characteristics: The variation of the collector current I_C with the collector emitter voltage V_{CE} is called the output characteristic. The plot of I_C versus V_{CE} for different fixed values of I_B gives one output characteristic. Since the collector current changes with the base current, there will be different output characteristics corresponding to different values of I_B.

Output Dynamic Resistance (r o): This is defined as the ratio of change in collector emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at a constant base current I_B.

$$r_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B}$$

The high magnitude of the output resistance (of the order of 100 kW) is due to the reverse-biased state of this diode.

(3) Transfer Characteristics: The transfer characteristics are plotted between the input and output currents (I_B versus I_C). Both I_B and I_C increase proportionately.

Current amplification factor (ß): This is defined as the ratio of the change in collector current to the change in base current at a constant collector-emitter voltage (V_{CE}) when the transistor is in active state.

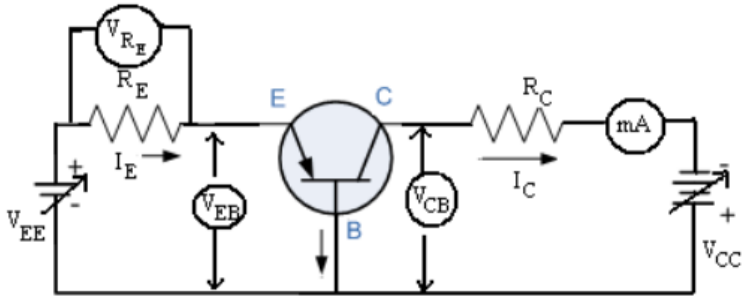
$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}}$$

This is also known as small signal current gain and its value is very large. The ratio of I_C and I_B we get what is called $ß_{dc}$ of the transistor. Hence,

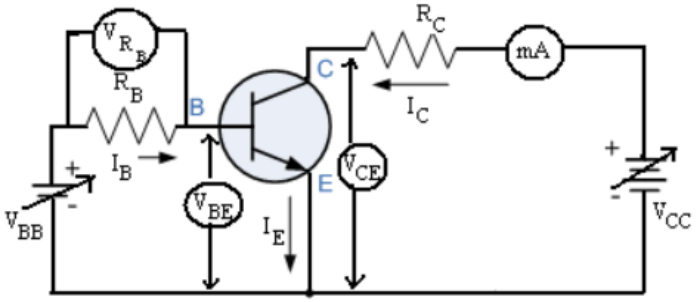
$$\beta_{dc} = \left.\frac{I_C}{I_B}\right|_{V_{CE}}$$

Since I_C increases with I_B almost linearly, the values of both $ß_{dc}$ and $ß_{ac}$ are nearly equal.

Circuit Diagrams:



PNP transistor in CB configuration



NPN transistor in CE configuration

PROCEDURE:

1. Note down the type number of both the transistors.
2. Identify different terminals (E, B and C) and the type (PNP/NPN) of the transistors. For any specific information refer the datasheet of the transistors.

(I) PNP Common Base (CB) characteristics

1. Configure CB circuit using the PNP transistor as per the circuit diagram. Use R_E=R_C= 150 Ω.
2. For input characteristics, first fix the voltage V_{CB} by adjusting V_{CC} to the minimum possible position. Now vary the voltage V_{EB} slowly (say, in steps of 0.05V) by varying V_{EE}. Measure V_{EB} using a multimeter. If V_{CB} varies during measurement bring it back to the initial set value. To determine I_E, measure V_{RE} across the resistor and use the relation $I_E = V_{RE}/R_E$.
3. Repeat the above step for another value of V_{CB} say, 2V.
4. Take out the multimeter measuring V_{EB} and connect in series with the output circuit to measure I_C. For output characteristics, first fix I_E= 0, i.e. V_{RE}= 0. By adjusting V_{CC}, vary the collector voltage V_{CB} in steps of say 1V and measure V_{CB} and the corresponding I_C using multimeters. After acquiring sufficient readings, bring back V_{CB} to 0 and reduce it further to get negative values. Vary V_{CB} in negative direction and measure both V_{CB} and I_C, till you get 0 current.
5. Repeat the above step for at least 5 different values of I_E by adjusting V_{EE}. You may need to adjust V_{EE} continuously during measurement in order to maintain a constant I_E.

6. Plot the input and output characteristics by using the readings taken above and determine the input and output dynamic resistance.
7. To plot transfer characteristics, select a suitable voltage V_{CB} well within the active region of the output characteristics, which you have tabulated already. Plot a graph between I_C and the corresponding I_E at the chosen voltage V_{CB}. Determine α_{ac} from the slope of this graph.

(II) NPN Common Emitter (CE) characteristics

1. Now configure CE circuit using the NPN transistor as per the circuit diagram. Use R_B= 100kΩ and R_C= 1 kΩ.
2. For input characteristics, first fix the voltage V_{CE} by adjusting V_{CC} to the minimum possible position. Now vary the voltage V_{BE} slowly (say, in steps of 0.05V) by varying V_{BB}. Measure V_{BE} using a multimeter. If V_{CE} varies during measurement bring it back to the set value. To determine I_B, measure V_{RB} across the resistor R_B and use the relation $I_B = V_{RB}/R_B$.
3. Repeat the above step for another value of V_{CE} say, 2V.
4. For output characteristics, first fix I_B= 0, i.e. V_{RB}= 0. By adjusting V_{CC}, vary the collector voltage V_{CE} in steps of say 1V and measure V_{CE} and the corresponding I_C using multimeters. If needed vary V_{CE} in negative direction as described for CB configuration and measure both V_{CE} and I_C, till you get 0 current.
5. Repeat the above step for at least 5 different values of I_B by adjusting V_{BB}. You mayneed to adjust V_{BB} continuously during measurement in order to maintain a constant I_B.
6. Plot the input and output characteristics by using the readings taken above and determine the input and output dynamic resistance.
7. Plot the transfer characteristics between I_C and I_B as described for CB configuration for a suitable voltage of V_{CE} on the output characteristics. Determine $ß_{ac}$ from the slope of this graph.

OBSERVATIONS AND CALCULATIONS:

CB configuration:

Transistor code: _____,
Transistor type: _____ (PNP/NPN)
R_E = _____,
R_C = _____.

Table (1): Input Characteristics

Sl. No.	V_{CB} = V			V_{CB} = V		
	V_{EB} (V)	V_{RE} (V)	I_E (mA)	V_{EB} (V)	V_{RE} (V)	I_E (mA)
1						
2						
..						
..						
10						

Table (2): Output Characteristics

Sl. No.	$I_{E1} = 0$		$I_{E2} =$		$I_{E3} =$		$I_{E4} =$		$I_{E5} =$	
	V_{CB} (V)	I_C (mA)	V_{CB} (V)	I_C (mA)	V_{CB} (V)	I_C (mA)	V_{CB} (V)	I_C (mA)	V_{CB} (V)	I_C (mA)
1										
2										
..										
..										
10										

Table (3): Transfer Characteristics V_{CB} = _____ V

Sl. No.	I_E (mA)	I_C (mA)
1		
2		
3		
4		
5		

CE configuration:

Transistor code: _____,
Transistor type: _____ (PNP/NPN)
R_B = _____,
R_C = _____.

Table (4): Input Characteristics

Sl. No.	V_{CE} = V			V_{CE} = V		
	V_{BE} (V)	V_{RB} (V)	I_B (µA)	V_{BE} (V)	V_{RB} (V)	I_B (µA)
1						
2						
..						
..						
10						

Table (5): Output Characteristics

Sl. No.	$I_{B1} = 0$		$I_{B2} =$		$I_{B3} =$		$I_{B4} =$		$I_{B5} =$	
	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)
1										
2										
..										
..										
10										

Table (6): Transfer Characteristics $V_{CE} =$ _____ V

Sl. No.	I_B (μA)	I_C (mA)
1		
2		
3		
4		
5		

Graphs:

Plot the input, output and transfer characteristics for each configuration.

CB configuration:

(1) Input characteristics: Plot $V_{EB} \sim I_E$, for different V_{CB} and determine the input dynamic resistance in each case at suitable operating points.
(2) Output characteristics: Plot $V_{CB} \sim I_C$, for different I_E and determine the output dynamic resistance in each case at suitable operating points in the active region.
(3) Transfer characteristics: Plot $I_E \sim I_C$, for a fixed V_{CB} and determine α_{ac}.

CE configuration:

(1) Input characteristics: Plot $V_{BE} \sim I_B$, for different V_{CE} and determine the input dynamic resistance in each case at suitable operating points.
(2) Output characteristics: Plot $V_{CE} \sim I_C$, for different I_B and determine the output dynamic resistance in each case at suitable operating points in the active region.
(3) Transfer characteristics: Plot $I_B \sim I_C$, for a fixed V_{CE} and determine β_{ac}.

Lab Session 14

OBJECTIVES

To investigate the characteristics curves for Field Effect Transistor.

EQUIPMENT REQUIRED

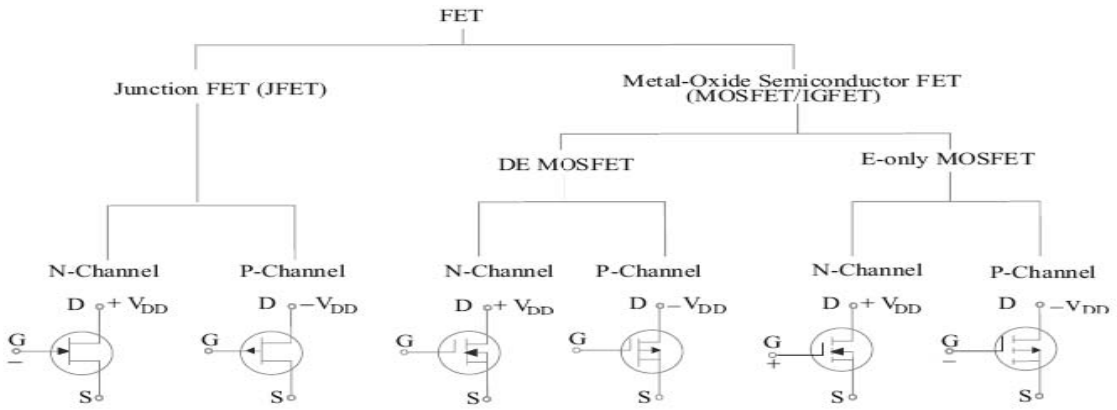
D.C power supply.
Oscilloscope ,A.V.Ometer .
FET, Resistors 1kΩ and 200kΩ.

BASIC THEORY

The acronym 'FET' stands for **field effect transistor**. It is a three-terminal unipolar solid state device in which current is controlled ***by an electric field*** as is done in vacuum tubes.
Broadly speaking, there are two types of FETs:
(*a*) junction field effect transistor (JFET)
(*b*) metal-oxide semiconductor FET (MOSFET)

It is also called insulated-gate FET (IGFET). It may be further subdivided into:
(*i*) depletion-enhancement MOSFET *i.e.* DEMOSFET
(*ii*) enhancement-only MOSFET *i.e.* E-only MOSFET

Both of these can be either *P*-channel or *N*-channel devices.
The FET family tree is shown below:



As shown in Fig.1, it can be fabricated with either an N-channel or P-channel though N-channel is generally preferred. For fabricating an N-channel JFET, first a narrow bar of N-type semiconductor material is taken and then two P-type junctions are diffused on opposite sides of its middle part [Fig.1 (a)].

These junctions form two P-N diodes or gates and the area between these gates is called channel. The two P-regions are internally connected and a single lead is brought out which is called gate terminal. Ohmic

contacts (direct electrical connections) are made at the two ends of the bar-one lead is called source terminal S and the other drain terminal D. When potential difference is established between drain and source, current flows along the length of the 'bar' through the channel located between the two P-regions. The current consists of only majority carriers which, in the present case, are electrons. P-channel JFET is similar in construction except that it uses P-type bar and two N-type junctions. The majority carriers are holes which flow through the channel located between the two N-regions or gates. Following FET notation is worth remembering:

1. **Source.** It is the terminal through which majority carriers enter the bar. Since carriers come from it, it is called the source.
2. **Drain.** It is the terminal through which majority carriers leave the bar i.e. they are drained out from this terminal. The drain to source voltage V_{DS} drives the drain current I_D.
3. **Gate.** These are two internally-connected heavily-doped impurity regions which form two P-N junctions. The gate-source voltage V_{GS} reverse biases the gates.
4. **Channel.** It is the space between two gates through which majority carriers pass from

Source-to-drain when V_{DS} is applied. Schematic symbols for N-channel and P-channel JFET are shown in Fig.1 (c). It must be kept in mind that gate arrow always points to N-type material.

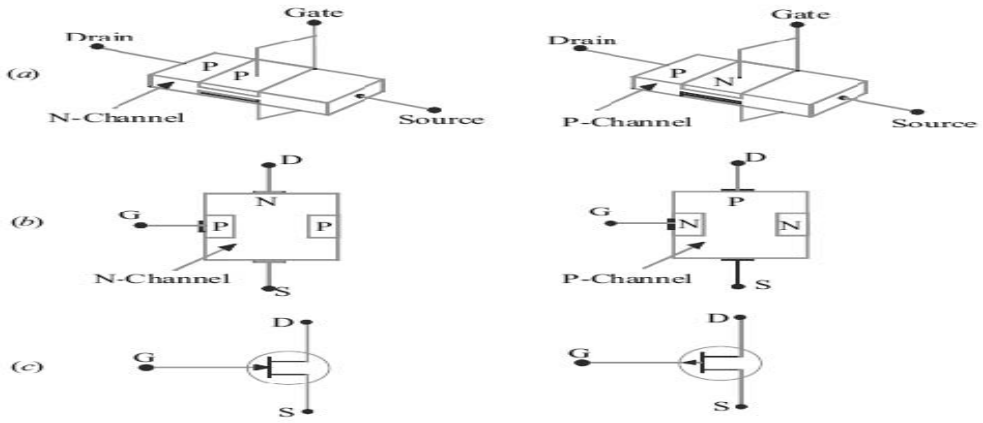


Fig. 1 FET construction

Static Characteristics of a JFET

We will consider the following two characteristics:

a) **Drain characteristic:** It gives relation between I_D and V_{DS} for different values of V_{GS} (which is called running variable).
b) **Transfer characteristic:** It gives relation between I_D and V_{GS} for different values of V_{DS}. We will analyse these characteristics for an N-channel JFET connected in the common-source mode as shown in Fig. 2. We will first consider the drain characteristic when $V_{GS}= 0$ and then when V_{GS} has any negative value upto V_{GS}(off).

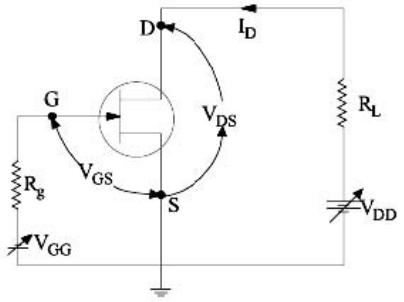


Fig. 2

JFET Drain Characteristic With $V_{GS} = 0$

Such a characteristic is shown in Fig. 3.

It can be subdivided into following four regions :

1) Ohmic Region OA: This part of the characteristic is linear indicating that for low values of V_{DS}, current varies directly with voltage following Ohm's Law. It means that JFET behaves like an ordinary resistor till point A (called knee) is reached.
2) Curve AB In this region, I_D increases at reverse square-law rate upto point B which is called pinch-off point. This progressive decrease in the rate of increase of I_D is caused by the square law increase in the depletion region at each gate upto point B where the two regions are closest without touching each other.

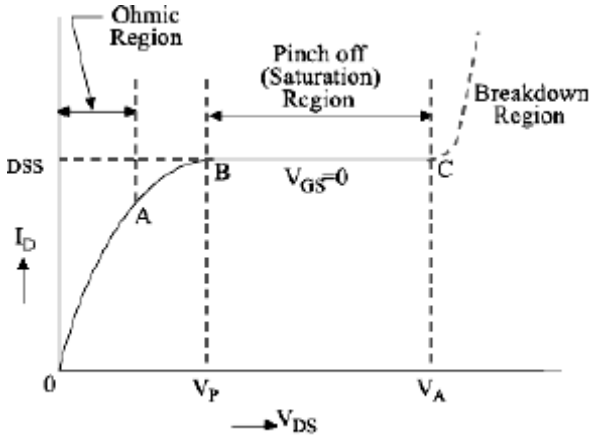


Fig. 3

3) Pinch-off Region BC: It is also known as saturation region or 'amplified' region. Here, JFET operates as a constant-current device because I_D is relatively independent of V_{DS}. It is due to the fact that as V_{DS} increases channel resistance also increases proportionally thereby keeping I_D practically constant at I_{DSS}. It should also be noted that the reverse bias required by the gate-channel junction is supplied entirely by the voltage drop across the channel resistance due to flow of I_{DSS} and none by external bias because $V_{GS} = 0$.
4) Breakdown Region: If V_{DS} is increased beyond its value corresponding to point C (called avalanche breakdown voltage), JFET enters the breakdown region where I_D increases to an excessive value. This happens because the reverse-biased gate-channel P-N junction undergoes avalanche breakdown when small changes in V_{DS} produce very large changes in I_D. It is interesting to note that increasing values of V_{DS} make a JFET behave first as a resistor (ohmic region), then as a constant-current source (pinch-off region) and finally, as a constant-voltage source (breakdown region).

PROCEDURE

1. Connect the circuit as shown in fig 4.
2. Let V_{DS} =(0,0.5,1,1.5,2,2.5,3,4,5)v measure I_D.
3. Repeat step 3 for V_{GS} =(0.5,1,1.5,2,2.5,3,3.5,4,4.5) V.

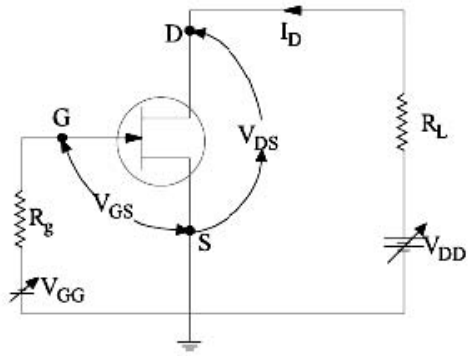


Fig. 4

OBSERVATIONS AND CALCULATIONS

1. Draw (drain characteristics) between I_D & V_{DS} for different values of V_{GS}.
2. Draw I_D with V_{GS}
3. Find g_m