PRACTICAL WORKBOOK

FOR ACADEMIC SESSION 2014

DIGITAL INTEGRATED CIRCUITS (EL-303)
THIRD YEAR ELECTRONICS

Name:

Roll Number:

Class:

Batch:

Department :

Department of Electronic Engineering
NED University of Engineering and Technology, Karachi

LABORATORY WORKBOOK

FOR THE COURSE

EL-303 DIGITAL INTEGRATED CIRCUITS

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THE BOARD OF STUDIES OF DEPARTMENT OF ELECTRONIC ENGINEERING

DIGITAL INTEGRATED CIRCUITS LABORATORY

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Lab No.1

PURPOSE:

Introduction to Digital Integrated Circuits and Orcad PSpice.

INTRODUCTION:

Analog and digital signals are used to transmit information, usually through electric signals. In both these technologies, the information, such as any audio or video, is transformed into electric signals. The difference between analog and digital technologies is that in analog technology, information is translated into electric pulses of varying amplitude. In digital technology, translation of information is into binary format (zero or one) where each bit is representative of two distinct amplitudes.

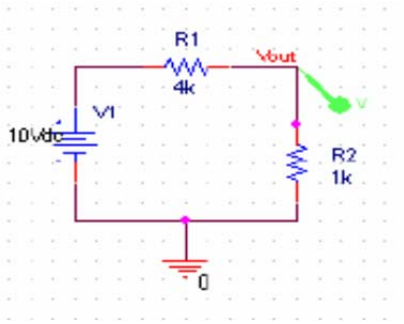
COMPARISON CHART:

	Analog	Digital
Signal:	Analog signal is a continuous signal which represents physical measurements.	Digital signals are discrete time signals generated by digital modulation.
Waves:	Denoted by sine waves	Denoted by square waves
Representation:	Uses continuous range of values to represent information	Uses discrete or discontinuous values to represent information
Example:	Human voice in air, analog electronic devices.	Computers, CDs, DVDs, and other digital electronic devices.
Technology:	Analog technology records waveforms as they are.	Samples analog waveforms into a limited set of numbers and records them.
Data transmissions:	Subjected to deterioration by noise during transmission and write/read cycle.	Can be noise-immune without deterioration during transmission and write/read

	Analog	Digital
		cycle.
Response to Noise:	More likely to get affected reducing accuracy	Less affected since noise response are analog in nature
Flexibility:	Analog hardware is not flexible.	Digital hardware is flexible in implementation.
Uses:	Can be used in analog devices only. Best suited for audio and video transmission.	Best suited for Computing and digital electronics
Applications:	Thermometer	PCs, PDAs
Bandwidth:	Analog signal processing can be done in real time and consumes less bandwidth.	There is no guarantee that digital signal processing can be done in real time and consumes more bandwidth to carry out the same information.
Memory:	Stored in the form of wave signal	Stored in the form of binary bit
power:	analog instrument draw large power	digital instrument draw only negligible power
cost:	low cost and portable	cost is high and easily not portable
impedance:	Low	high order of 100mega ohm
errors:	analog instruments usually have a scale which is cramped at lower end and give considerable observational errors	digital instruments are free from observational errors like parallax and approximation errors

ORCAD-PSPICE:

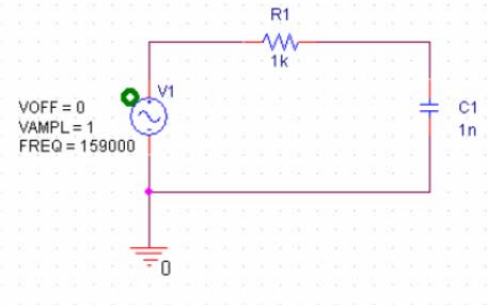
- From Program open Orcad10.0 Capture CIS.
- Go to File → New→ Project.
- Name the project as **example**, click on the tab Analog or Mixed A/D and save it the default Location.
- In **create PSpice Project** Window click on the tab **Create based upon an existing project** and then click OK.
- In **Studio Suite** Selection select **PSpiceAD** and then click Ok.
- In **Design Resources** click on Schematic 1 and then double click on Page1, a page will open.
- Click the **place part** button (which is in the vertical toolbar on the right side) and then go to add library, select all the p-spice libraries and then open them.
- From library select R/ANALOG and place it on the Schematic Page. Place 2 resistors.
- From library select VDC/SOURCE
- To connect the items in the circuit, select the **Place Wire** tool by clicking on the third button from the top on the vertical toolbar on the right side. Drag the mouse between the terminals of your placed parts to connect them.
- In order for PSpice to simulate your circuit, it must have a "zero" node for a ground. To add this ground, select the **Place Ground** tool by clicking on the 9th button from the top on the vertical toolbar on the right side.
- To change the value for an item, double click the value you want to change and enter the value you want on the dialog box that appears. Double click on the **1k** value of the horizontally placed resistor and change the **Value** to **4k**.
- It is important to name the nodes you want to plot in PSpice so you can find them easily. To name a node, select the **Place Net Alias** tool then change the **Alias** to **Vout** and click **OK**.
- Then place the alias on the desired node for Vout (i.e. the junction of the 2 resistors).
- The circuit should look like this



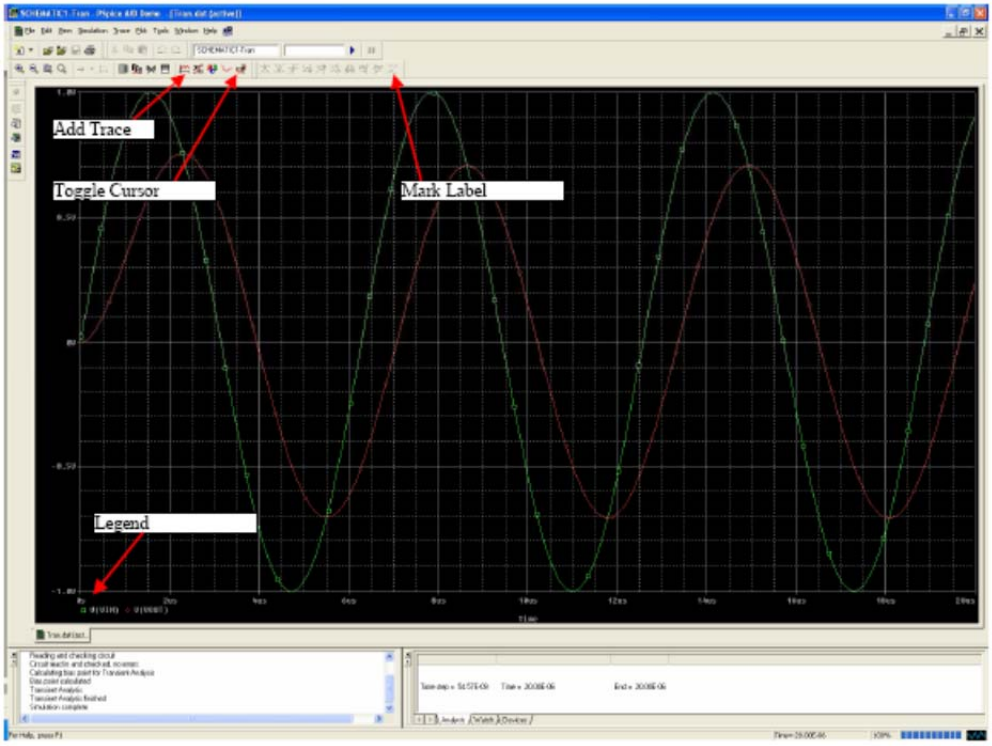
- Next, configure the simulation by clicking the **New Simulation Profile** button on the top toolbar. Enter the **Name** lab1.
- Click **Create**.

TRANSIENT ANALYSIS:

- For this circuit, select and wire these components:
  Capacitor (Place Part C in ANALOG library), Resistor (Place Part R in ANALOG library), Sinusoidal Source (Place Part VSIN in SOURCE library), and Ground (Place Ground 0 SOURCE library).
- Double click on the VOFF attribute of the VSIN component.Change the value from <VOFF> to 0. Click OK. Similarly, set the VAMPL attribute to 1 and the FREQ attribute to 159000. (1/(2*PI*R*C)). This circuit is shown below:



- Next, configure the simulation by clicking the **New Simulation Profile** button on the top toolbar. Enter the **Name** Tran and the following dialog box will appear. Set Analysis type: **Time Domain (transient)**, **Run To Time:** 20us, and **Maximum Step Size** to 100ns. Click **OK**.
- Click on the **Voltage/Level Marker** button and place a marker at the junction of the **R** and **C** and at the junction between the **Source** and the **R**.
- Click the **Run PSpice** button and the PSpice Analysis results will appear as shown below.



- Click the **toggle cursor** button to determine values of Vin and Vout at different points.

Lab No.2

PURPOSE:

To produce an astable multivibrator with:

Symmetrical square wave output

EQUIPMENT REQUIRED:

- Bread Board
- Resistors (1/4 Watt), Capacitor
- Digital multimeter
- Function generator
- Oscilloscope

THEORY:

With an astable multivibrator, the op amp operates only in the non-linear region. So its output has only two voltage levels, Vmin and Vmax. The astable continually switches from one state to the other, staying in each state for a fixed length of time. The circuit of an astable multivibrator is shown in figure f7.01. Note that this circuit does not need an input signal. To find out the relations governing the operation of the astable, we start with the usual hypothesis that the operational amplifier has an ideal behavior. Suppose the output is in the state Vo = Vmax. When Vo takes this value the voltage V_{Al} of the non inverting input is:

$$V_{Al} = Vmax .R\,1/ (R1 + R2)$$

The capacitor C starts charging through resistor R towards the value Vmax. This charging continues until the voltage V_B of the inverting input reaches the value V_{Al}. At this point, as the inverting input voltage is more than the non-inverting input, the output switches low, to Vmin. The voltage V_{A2} is now given by:

$$V_{A2} = Vmin .R1 / (R1 + R2)$$

At this point, the capacitor C starts discharging through R towards the voltage Vmin until it reaches the value V_{A2}, at which point the output switches to Vmax .The cycle then starts again.

We have seen that the voltage across the capacitor C can vary from V_{Al} to V_{A2}, so in the

period of time when the output is low, at Vmin, the voltage on the capacitor is given by:

$$V_B(t)=Vmin - (Vmin-Vmax*R1/(R1 + R2))*e^{-t/R*C}$$

While in the period of time when the output is at *Vmax,* the capacitor voltage is:

$$V_B(t)=Vmax - (Vmax-Vmin*R1/(R1 + R2))*e^{-t/R*C}$$

The period T1 for which the output voltage is at *Vmax* can be found by calculating the time the capacitor voltage takes to equal V_{Al}. So:

$$Vmax/(R1+R2) = (Vmin/(R1+R2)-Vmax)*e^{-T1/R*C} + Vmax$$

From which:

$$T1=R*C*\ln \frac{Vmax-R1/(R1+R2)*Vmin}{Vmax-R1/(R1+R2)*Vmax}$$

Similarly we can find the period T2 for which the output stays at *Vmin:*

$$T2=R*C*\ln \frac{Vmax*R1/(R1+R2)-Vmin}{Vmin*R1/ (R1+R2)-Vmin}$$

Supposing that *Vmin* = -*Vmax* we obtain:

$$T1=T2=2R*C*\ln \frac{1+R1/ (R1+R2)}{1-R1/ (R1+R2)}$$

The total period *T* of the square-wave is given by the sum of *T* 1 and *T2.* We can see that the square-wave period and so the frequency can be varied by varying the values of R1, R2, R and C. To obtain an asymmetrical square-wave (duty cycle not 50%) we can make the capacitor charge and discharge through resistors of different values.

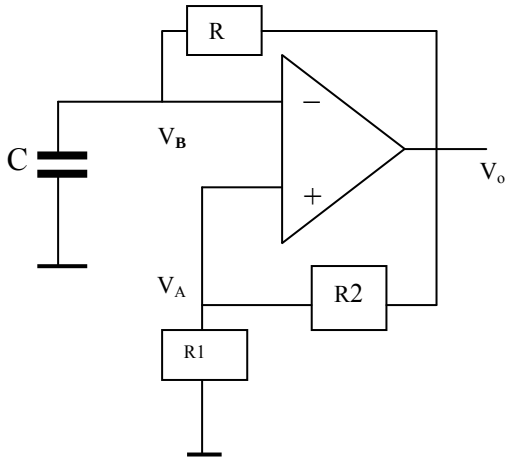
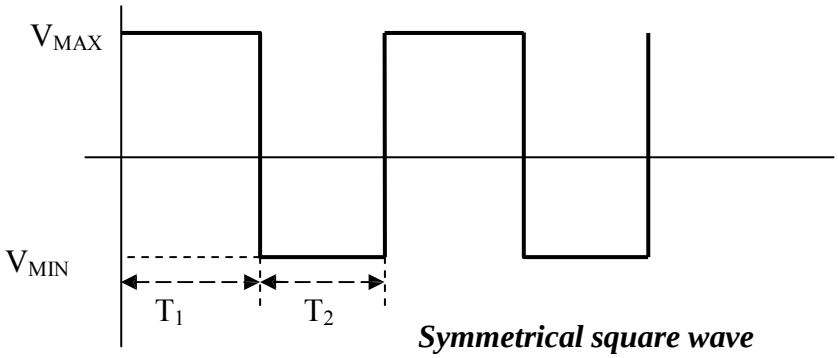


Fig2.1

$$\mathbf{T} = T_1 + T_2$$



Symmetrical square wave

Fig 2.2

PRELAB ASSIGNMENT:

Use the computer software tool Orcad PSPICE to simulate the circuit .Make sure to bring the PSPICE results to the laboratory. In addition to being an aid in immediately verifying measured results, **they will be the basis of your Pre-lab grade for this lab.**

- Transient response (time-domain). Also mark label to the maximum output voltage (using PSpice.

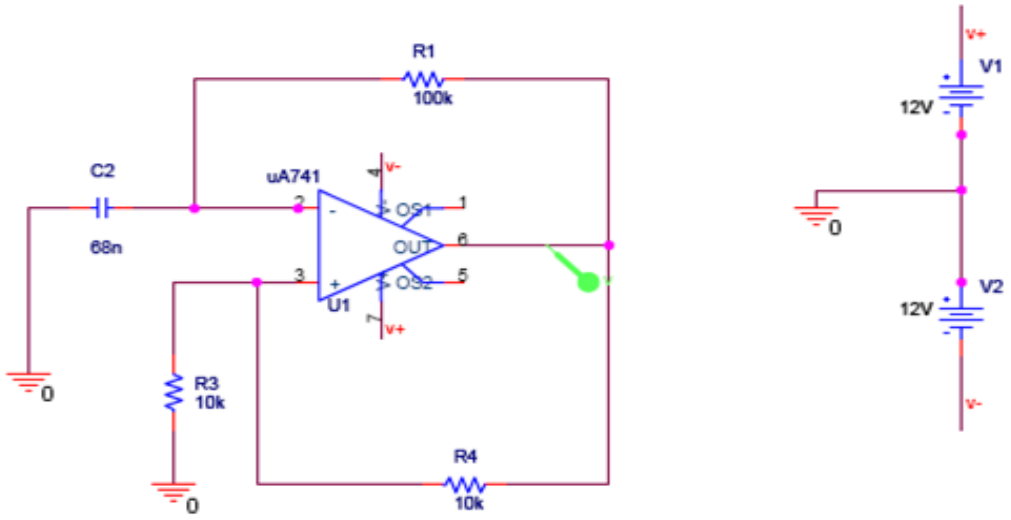


Fig2.3

PROCEDURE:

- Implement the circuit of Fig 2.3.
- Calculate the output frequency with the formulae.
- Connect the first probe of the oscilloscope to the output V_o of the amplifier and the second probe to the inverting input V_B
- Measure the frequency with the oscilloscope, and compare it with the theoretical result
- Calculate the capacitor voltages at which output switching occurs, according to the formulae
- Measure the capacitor voltages at which output switching occurs and compare the results with those calculated from theory.

Calculate the values of T1 and T2 as given by the formulae.
Measure the values of T1 and T2 with the oscilloscope.

OBSERVATION (SYMMETRICAL SQUARE WAVE):

S.NO.	Quantity	Observed Value	Calculated Value
1	$V_{B\ (P-P)}$		
2	$V_{O(P-P)}$		
3	Frequency		
4	Vmax		
5	Vmin		
6	Capacitor charging time		
7	Capacitor discharging time		

OUTCOME:

- The approximate frequency of the oscillation of the astable multivibrator (Symmetrical square wave), when R1=R2=10k and R=100K, C = 68nf an d Vmin = -Vmax comes out to be: $1 / T_1+T_2 =$

PROJECT

Assigned Task:

Design a circuit using 741 op-amp to generate an asymmetrical square wave keeping in view Lab 2

Attach the working of the circuit, Calculations and all the observations as done in Lab No.2

Lab No.3

PURPOSE:
To determine the frequency and output amplitude of a triangular wave generator.

EQUIPMENT REQUIRED:

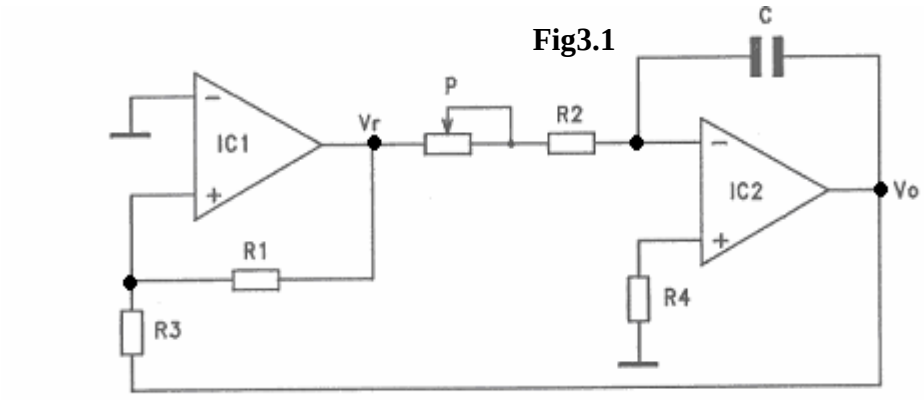
- Bread Board
- Resistors (1/4 Watt), Capacitor
- Digital multimeter
- Function generator
- Oscilloscope

THEORY:
Among the waveforms that can be generated with op amps, the most common are the triangular, the ramp and the square-wave. A triangular wave can be generated with the circuit of figure F8.01.in which two operational amplifiers are used. The first operates as a comparator, while the second as an integrator. V_O is the output voltage of the integrator, Vr the output voltage of the comparator. The saturation voltages Vmax and Vmin are equal in amplitude, and so can be called +Vr and –Vr respectively. Suppose the output of the comparator is +Vr. The voltage V_O will be a negative ramp which will continue to grow until the voltage of the non-inverting input of the comparator rises above zero. The minimum value of the output voltage V_O, applying the superposition principle, will be given by:

$$0=\frac{Vr*R3 + V_O*R1}{R1+R3}$$

From which we get: $V_O = -Vr*R3/R1$

Fig3.1



The same principles apply for the maximum voltage the output reaches, with the only difference that the ramp is raising and the voltage Vr is negative: defining this voltage as $V_{O'}$
we have:
Vo' = Vr *R3 / Rl
To calculate the time T taken to rise from V_O to $V_{O'}$ remember that the capacitor C charges with a constant current given by:

$$I = Vr / (P+R2)$$

So, from:

$$I = - C*dVo / dt$$

We find that:

$$\frac{Vr}{P+R2} = -\frac{C* (Vo' -Vo)}{T}$$

From which:

$$V o' -Vo = - \frac{Vr*T}{C*(P+R2)}$$

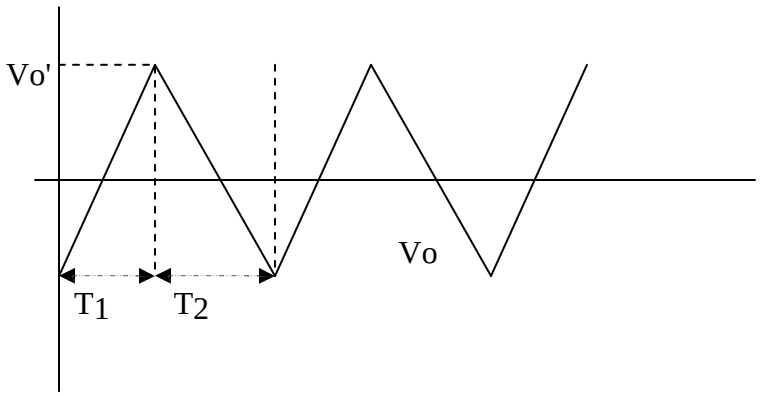
As: $Vo' -Vo = 2*Vr*R3 / Rl$

we have:

$$T = 2*R3*(P + R2)*C / Rl$$

The time T is equal to half period, so the output frequency F will be the inverse of twice T:

$$F = R1/ [4*R3*(R2+P)*C]$$



Triangular wave

PRELAB ASSIGNMENT:

Use the computer software tool Orcad PSPICE to simulate the circuit. Plot the output waveform of both the op-amps. Make sure to bring the PSPICE results to the laboratory. In addition to being an aid in immediately verifying measured results, **they will be the basis of your Pre-lab grade for this lab.**

- Transient response (time-domain). Also mark label to the maximum output voltage (using PSpice).

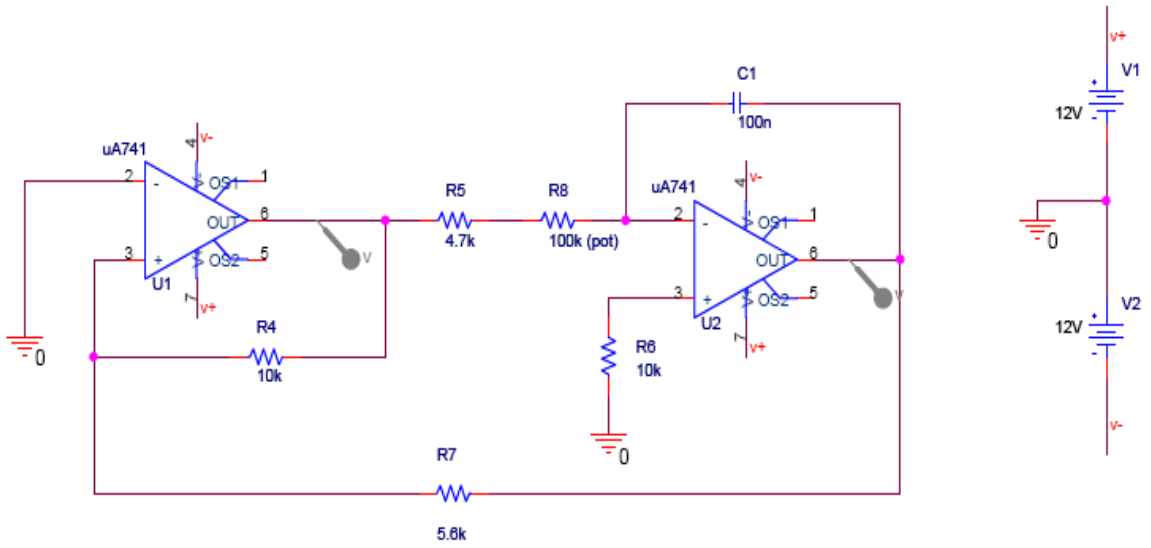


Fig 3.2

PROCEDURE:

Adjust 100kΩ potentiometer completely CCW to obtain zero resistance and measure the output voltage value of the comparator (1st op-amp) using oscilloscope.
Adjust the potentiometer to half value.
Calculate the amplitude of the output voltage (2nd op-amp).
Measure the amplitude of the output voltage with the oscilloscope.
Calculate the output voltage frequency according to the formulae.
Measure the output frequency with the oscilloscope.
Check the presence of a square wave at the output of the comparator (1st op-amp).

OBSERVATION:

S.NO.	Quantity	Observed Value	Calculated value
1	V_O(triangular)		
2	Frequency (triangular)		

OUTCOME:

The approximate frequency of the oscillation of the astable multivibrator comes out to be:
The output voltage of the oscillation of the astable multivibrator comes out to be:

PROJECT

Assigned Task:

Design a circuit using 741 op-amp to generate a ramp wave keeping in view Lab 3

Attach the working of the circuit, Calculations and all the observations as done in Lab No. 3

Lab No. 4

PURPOSE:

Implementation of Bistable Multivibrator using 555 timer.

EQUIPMENT REQUIRED:

- Digital multimeter
- Oscilloscope
- Bread Board
- LM555 Timer IC
- Capacitor 10 nF, 1uF
- Resistance sheet (1/4 watt)
- LEDs -2
- Push button Switch

THEORY:

Multivibrators and CMOS Oscillators can be easily constructed from discrete components to produce relaxation oscillators for generating basic square wave output waveforms. But there are also dedicated IC's especially designed to accurately produce the required output waveform with the addition of just a few extra timing components. One such device that has been around since the early days of IC's and has itself become something of an industry "standard" is the **555 Timer Oscillator** which is more commonly called the **"555 Timer"**.

The **555 Timer** which gets its name from the three 5kΩ resistors it uses to generate the two comparators reference voltage, is a very cheap, popular and useful precision timing device that can act as either a simple timer to generate single pulses or long time delays, or as a relaxation oscillator producing stabilized waveforms of varying duty cycles from 50 to 100%.

The 555 timer chip is extremely robust and stable 8-pin device that can be operated either as a very accurate ***Monostable***, ***Bistable*** or ***Astable*** Multivibrator to produce a variety of applications such as one-shot or delay timers, pulse generation, LED and lamp flashers, alarms and tone generation, logic clocks, frequency division, power supplies and converters etc, in fact any circuit that requires some form of time control as the list is endless.

The single 555 Timer chip in its basic form is a Bipolar 8-pin mini Dual-in-line Package (DIP) device consisting of some 25 transistors, 2 diodes and about 16 resistors arranged to form two comparators, a flip-flop and a high current output stage as shown below. As well as the 555 Timer there is also available the NE556 Timer Oscillator which combines TWO individual 555's

within a single 14-pin DIP package and low power CMOS versions of the single 555 timer such as the 7555 and LMC555 which use MOSFET transistors instead.

A simplified "block diagram" representing the internal circuitry of the **555 timer** is given below with a brief explanation of each of its connecting pins to help provide a clearer understanding of how it works.

555 Timer Block Diagram

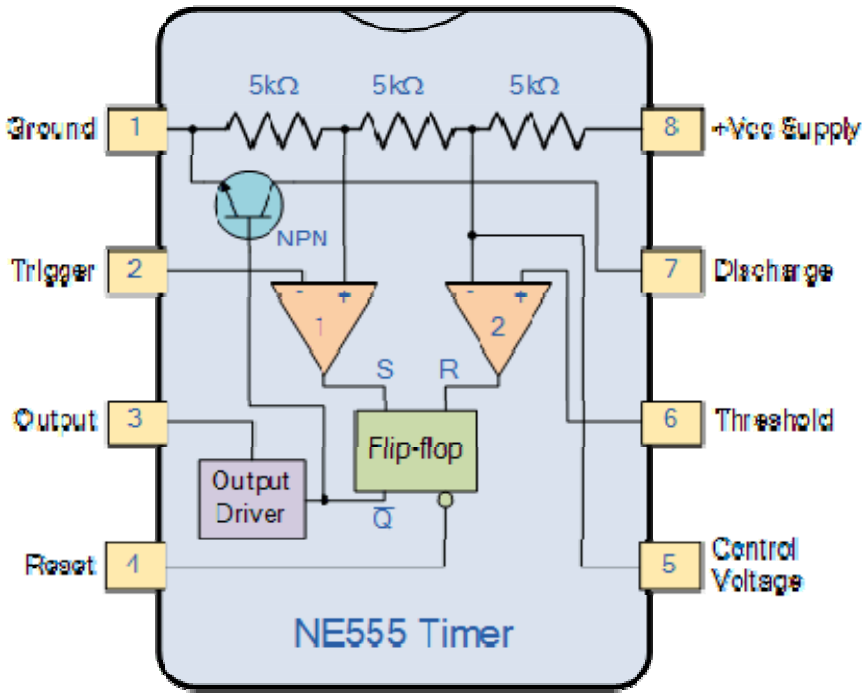


Fig 4.1

- Pin 1. − **Ground**, The ground pin connects the 555 timer to the negative (0v) supply rail.

- Pin 2. − **Trigger**, The negative input to comparator No 1. A negative pulse on this pin "sets" the internal Flip-flop when the voltage drops below 1/3Vcc causing the output to switch from a "LOW" to a "HIGH" state.

- Pin 3. − **Output**, The output pin can drive any TTL circuit and is capable of sourcing or sinking up to 200mA of current at an output voltage equal to approximately Vcc - 1.5V so small speakers, LEDs or motors can be connected directly to the output.

- Pin 4. − **Reset**, This pin is used to "reset" the internal Flip-flop controlling the state of the output, pin 3. This is an active-low input and is generally connected to a logic "1" level when not used to prevent any unwanted resetting of the output.

- Pin 5. − **Control Voltage**, This pin controls the timing of the by overriding the 2/3Vcc level of the voltage divider network. By applying a voltage to this pin the width of the output signal can be varied independently of the RC timing network. When not used it is connected to ground via a 10nF capacitor to eliminate any noise.

- Pin 6. − **Threshold**, The positive input to comparator No 2. This pin is used to reset the Flip-flop when the voltage applied to it exceeds 2/3Vcc causing the output to switch from "HIGH" to "LOW" state. This pin connects directly to the RC timing circuit.

- Pin 7. − **Discharge**, The discharge pin is connected directly to the Collector of an internal NPN transistor which is used to "discharge" the timing capacitor to ground when the output at pin 3 switches "LOW".

- Pin 8. − **Supply +Vcc**, This is the power supply pin and for general purpose TTL 555 timers is between 4.5V and 15V.

The **555 Timers** name comes from the fact that there are three 5kΩ resistors connected together internally producing a voltage divider network between the supply voltage at pin 8 and ground at pin 1. The voltage across this series resistive network holds the positive input of comparator two at 2/3Vcc and the positive input to comparator one at 1/3Vcc.

The two comparators produce an output voltage dependent upon the voltage difference at their inputs which is determined by the charging and discharging action of the externally connected RC network. The outputs from both comparators are connected to the two inputs of the flip-flop which in turn produces either a "HIGH" or "LOW" level output at Q based on the states of its inputs. The output from the flip-flop is used to control a high current output switching stage to drive the connected load producing either a "HIGH" or "LOW" voltage level at the output pin.

The most common use of the 555 timer oscillator is as a simple astable oscillator by connecting two resistors and a capacitor across its terminals to generate a fixed pulse train with a time period determined by the time constant of the RC network. But the 555 timer oscillator chip can also be

connected in a variety of different ways to produce Monostable or Bistable multivibrators as well as the more common Astable Multivibrator.

Bistable 555 Timer

The **555 Bistable** is one of the simplest circuits we can build using the 555 timer oscillator chip. This bistable configuration does not use any RC timing network to produce an output waveform so no equations are required to calculate the time period of the circuit. Consider the Bistable 555 Timer circuit below.

Bistable 555 Timer (flip-flop)

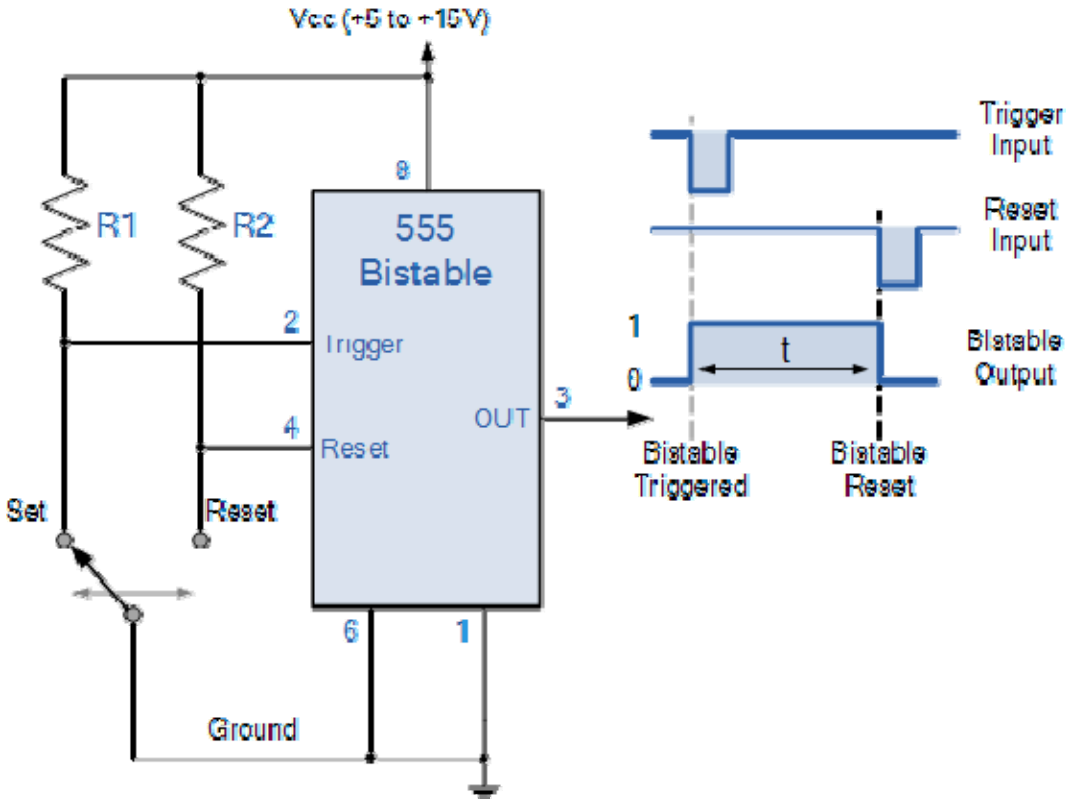


Fig 4.2

555 Timer Output

. The output (pin 3) of the standard 555 timer or the 556 timer, has the ability to either "Sink" or "Source" a load current of up to a maximum of 200mA, which is sufficient to directly drive output transducers such as relays, filament lamps, LED's motors, or speakers etc with the aid of series resistors or diode protection.

This ability of the 555 timer to both "Sink" (absorb) and "Source" (supply) current means that the output device can be connected between the output terminal of the 555 timer and the supply to sink the load current or between the output terminal and ground to source the load current. For example.

Sinking and Sourcing the 555 Timer

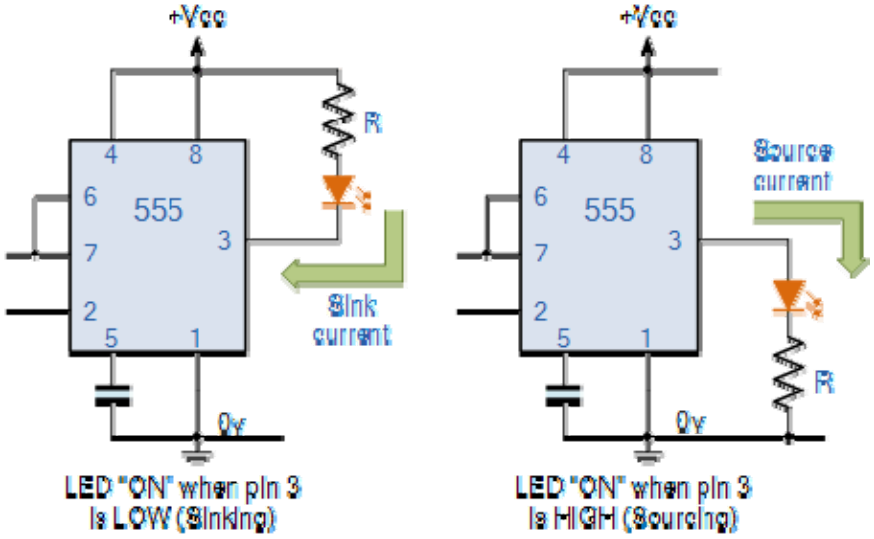


Fig 4.3

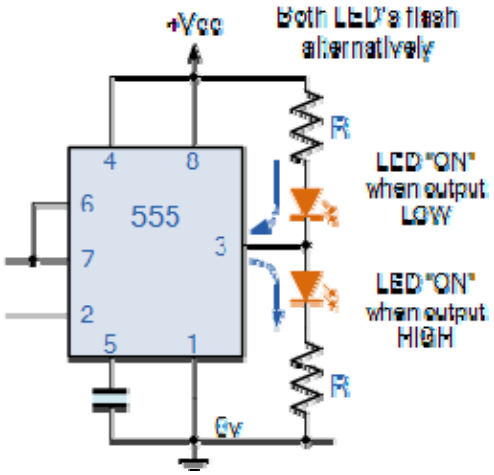


Fig 4.4

In the first circuit above, the LED is connected between the positive supply rail (+Vcc) and the output pin 3. This means that the current will "Sink" (absorb) or flow into the 555 timer output terminal and the LED will be "ON" when the output is "LOW".

The second circuit above shows that the LED is connected between the output pin 3 and ground (0 V). This means that the current will "Source" (supply) or flow out of the 555 timers output terminal and the LED will be "ON" when the output is "HIGH".

The ability of the 555 timer to both sink and source its output load current means that both LED's can be connected to the output terminal at the same time but only one will be switched "ON" depending whether the output state is "HIGH" or "LOW". The circuit to the left shows an example of this. the two LED's will be alternatively switched "ON" and "OFF" depending upon the output. Resistor, R is used to limit the LED current to below 20mA.

It was said earlier that the maximum output current to either sink or source the load current via pin 3 is about 200mA and this value is more than enough to drive or switch other logic IC's, LED's or small lamps etc. But what if one wants to switch or control higher power devices such as motors, electromagnets, relays or loudspeakers. Then we would need to use a ***Transistor*** to amplify the 555 timers output in order to provide a sufficiently high enough current to drive the load.

APPLICATION:

This type of circuit is ideal for use in an automated model railway system where the train is required to run back and forth over the same piece of track. A push button (or reed switch with a magnet on the underside of the train) would be placed at each end of the track so that when one is hit by the train, it will either trigger or reset the bi-stable multivibrator. The output of the 555 would control a DPDT relay which would be wired as a reversing switch to reverse the direction of current to the track, thereby reversing the direction of the train.

PRELAB ASSIGNMENT:

Use the computer software tool Multisim to simulate the circuit. Plot the output waveform of by changing the switch position each time. Make sure to bring the simulated results to the laboratory. In addition to being an aid in immediately verifying measured results, **they will be the basis of your Pre-lab grade for this lab.**

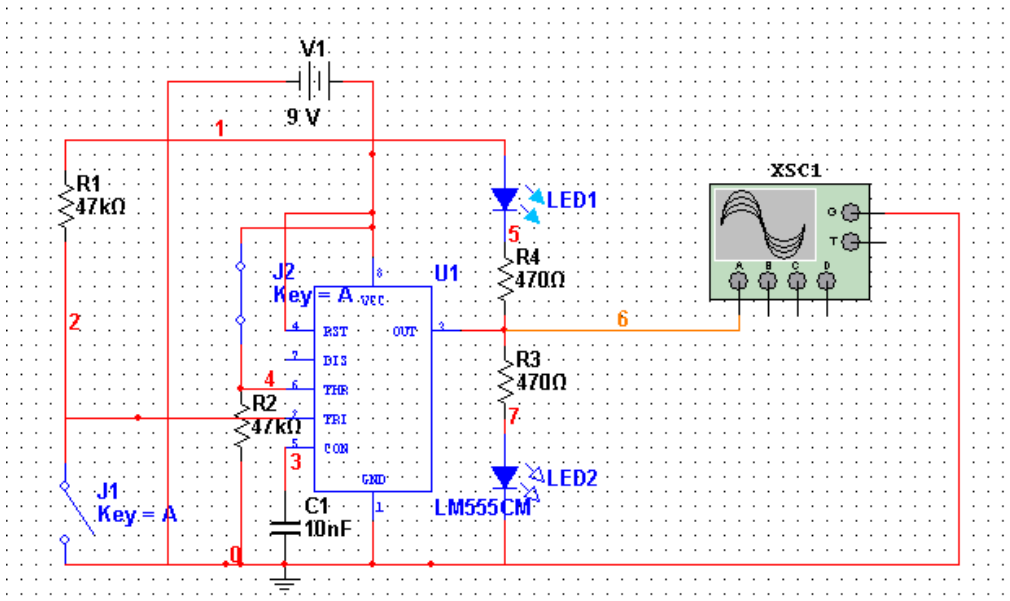


Fig 4.5

PROCEDURE:

- Implement the circuit in Fig 4.5 and change the switch position each time to observe the working of bistable multivibrator on oscilloscope.
- Note down the maximum output voltage.
- Compare the results with the simulated one.

Result :

The output turns high when _____ is closed and turns low when _____is closed.

Lab No.5

PURPOSE:

To illustrate the operation and characteristics of the analog switches.

EQUIPMENT REQUIRED:

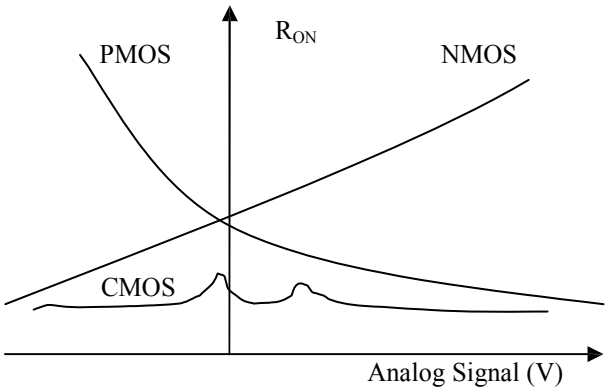
- Base unit for the IPES system
- Experiment module G33/EV
- Digital multimeter

BASIC THEORY:

CMOS Switches

MOSFETs are easily integrated into driver circuits on a single chip, and are therefore suitable for use as analog signal switches. The main disadvantage in switches featuring PMOS and NMOS transistors is there sensitivity to ON resistance at the analog signal voltage.

This problem can almost entirely eliminated by the use of CMOS switch consists of two parallel switches one featuring a channel-p MOSFET, the other with a channel-n MOSFET this parallel combination gives a relatively flat ON resistance/ analog signal voltage curve .



DESCRIPTION OF THE MODULE

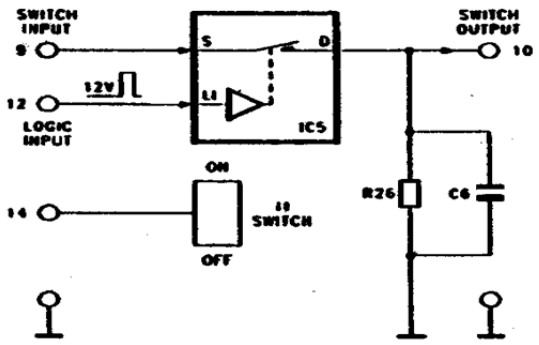
ANALOG SWITCH

The section of the circuit denominated" ANALOG SWITCH" consists of the integrated analog switch ICs (DG 200 CJ).

The data sheet shows that this is a two-channel single-pole single-throw (SPST) analog switch which employs CMOS technology to ensure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in both directions with no offset voltage in the ON condition and block voltages up to 30 Vp-p in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With logic "0" at the input to the driver, the switch will be ON; logic "1" will turn the switch OFF. A voltage of between 0 and 0.8V is required for logic "0", while logic "1" is given by a voltage of between 2.4 and 15V. The input can therefore be directly interfaced with TTL, DTL, RTL and CMOS circuits.

The switch action is break-before-make, in order to prevent any shorting in the input signal. For the sake of convenience in the execution of the exercises, and as the switch is bidirectional, the two terminals of the analog switch are indicated on the trainer panel as SWITCH IN and SWITCH OUT. The driver logic input may be manual (ON/OFF operation via special switch) or external. This is selected by fitting a jumper between jack 12 and jack 14.

Fig5.1



PROCEDURE:

Measuring r_{DS} (ON) without current

Purpose of the exercise

The purpose of this exercise is to measure the drain-source resistance present in the analog switch without current.

Connect the ±12V and ground jacks on the panel to a corrected power supply.
Connect jack 12 to jack 14.
Connect the digital multimeter (set to measure ohms) between jacks 9 and 10.
Set switch I_1 to ON; read the value of r_{DS} (ON) indicated on the digital multimeter.

Measuring r_{DS} (ON) with current

PURPOSE of the exercise

The purpose of this exercise is to measure the drain-source resistance present in the analog switch in the ON state as the current increases.

PROCEDURE

Connect the ±12V and ground jacks on the panel to a corrected power supply.
Connect jacks 12 and 14.
Connect a variable 0 => + 12V DC power supply between jack 9 and ground.
Set switch I_1 to ON.
Increase the input voltage gradually until voltage can be measured at the terminals of R_{26}, as shown in column 1 of table 9.1. For each R_{26} voltage, measure the voltage between jacks 9 and 10 and list these voltages in column
Care should be taken to avoid exceeding 12V, as this might damage the unit.
Given R_{26} equivalent to 1.2KΩ.
Calculate the current circulating between drain and source.
From V_{DS} and I_{DS}, calculate the value of R_{DS} and list in column 4.
Plot the drain source current values (I_{DS} - mA) on the x-axis and the drain source resistance values (R_{DS} - Ω) on the y-axis.

S.N.	V_{R26}(volts)	$I_{DS(mA)}$	$V_{DS\ (mV)}$	$R_{DS\ (\Omega)}$
1				
2				
3				
4				
5				
6				

OUTCOME:

The R_{DS} (ON) without current comes out to be: _____
The R_{DS} (ON) with current 2 mA comes out to be: _____

Lab No.6

PURPOSE:

To illustrate the switching times and switching threshold of the analog switches.

EQUIPMENT REQUIRED:

- Base unit for the IPES system
- Experiment module G33/EV
- Digital multimeter
- Function generator
- Oscilloscope

BASIC THEORY:

One of the main specifications regarding the application of analog switches is the TURN ON TIME and the TURN OFF TIME. When a switch is commanded to change from ON to OFF, and vice-versa, a propagation delay occurs in the circuit driver. The T_{ON} and T_{OFF} times may be used to determine when a switch begins operation and whether multiple switches connected in a multiplexer configuration will be "make-before-break"
or "break-before-make", i.e. whether the switches are triggered and then pause, or whether the pause precedes their action. The propagation delay should not be confused with the settling time, which is also effected by the load impedance. Two transitions will therefore apply:

$$\text{OFF to ON } t_{settling} = t_{ON} + t_l \uparrow \text{ where } t_l \uparrow = f(R_{ON}, R_{LOAD}, C_D, C_{LOAD})$$

$$\text{ON to OFF } t_{settling} = t_{OFF} + t_l \downarrow \text{ where } t_l \downarrow . = f(R_{LOAD}, C_{LOAD}, C_D)$$

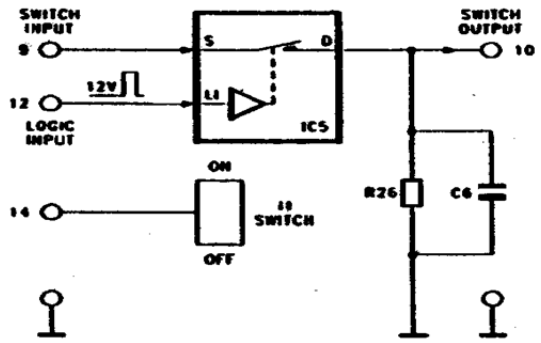


Fig.6.1

Measurement of the switching time

Purpose of the exercise

The purpose of this exercise is to determine the time required by the analog switch to open and close.

Procedure

Connect the ±12V and ground jacks on the panel to a corrected power supply.
Connect a + 10V DC power supply between jack 9 and ground.
Send a rectangular signal from the function generator between jack 12 and ground (amplitude 5V positive, frequency 50 KHz).
Connect one of the probes of the oscilloscope to the generator signal and the other to the output signal present between jack 10 and ground.
Measure the switching times between the output signal and the control signal; i.e. the rise time which corresponds to the closing of the analog switch and the fall time which corresponds to its opening.

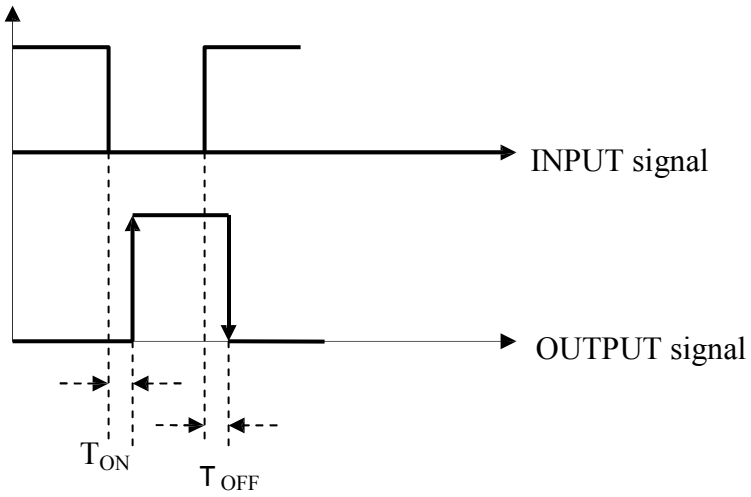


Fig 6.2

Measurement of the switching threshold

Purpose of the exercise

The purpose of this exercise is to measure the voltages at which the analog switch opens and closes.

Procedure

Connect the ±12V and ground jacks on the panel to a corrected power supply.
Connect a +5V DC power supply between jack 9 and ground.
Send a triangular signal from the function generator between the 12 jack and ground (amplitude 5V positive, frequency 1 KHz).
Connect one of the probes of the oscilloscope to the generator signal and the other to the output signal present between jack 10 and ground.
Measure the switching threshold by comparing the output signal with the control signal, i.e. the amplitude of the control signal at which the analog switch opens (V_1) and the amplitude at which it closes (V_2).

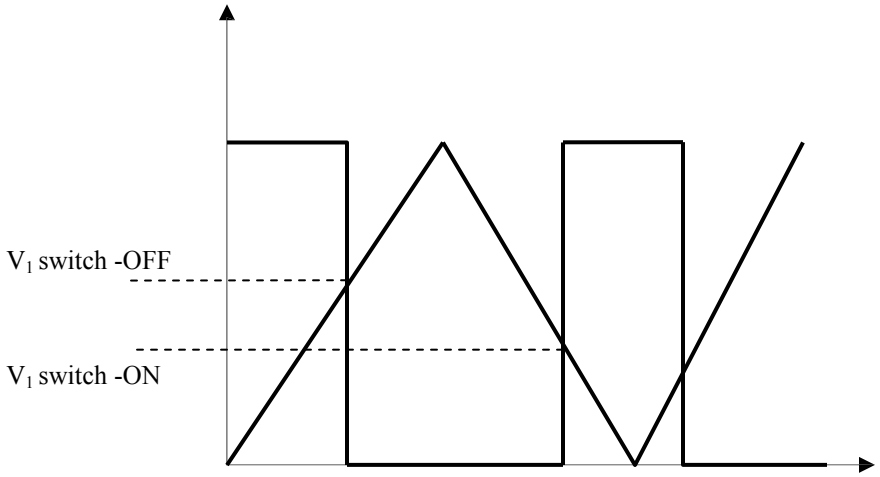


Fig 6.3

OUTCOME:

The t_{ON} (Turn ON time) of the analog switch comes out to be: _____
The t_{OFF} (Turn OFF time) of the analog switch comes out to be: _____
The voltages at which the analog switch opens comes out to be: _____
The voltages at which the analog switch closes comes out to be: _____

Lab No.7

PURPOSE:

To illustrate the operation and characteristics of the sample and hold circuit

EQUIPMENT REQUIRED:

Base unit for the IPES system
Experiment module G33/EV
Function generator
Oscilloscope

THEORY:

INTRODUCTION

The most simple sample and hold circuit consists of a switch and a capacitance. Two important specifications may be easily illustrated using the basic circuit. These are the aperture time and the acquisition time. The aperture time is the delay (reaction time) between the moment in which the control logic instructs the switch to open and the moment in which the aperture actually occurs. When extremely long aperture times (in the order of milliseconds) are tolerated, a relay may be used for the switch. For aperture times of less than 100 μs, FETs or BJTs are used as switches.
In variable-time systems, the input signal to the sample and hold circuit changes; the sample and hold circuit holds the last signal measured. The acquisition time is the time required by the sample and hold circuit to acquire the input signal value (within a predetermined degree of accuracy) when the control logic passes from hold to sample. Clearly, the most onerous condition is that in which the output must alter over its entire range (e.g. from + 10V to -10V and vice-versa).

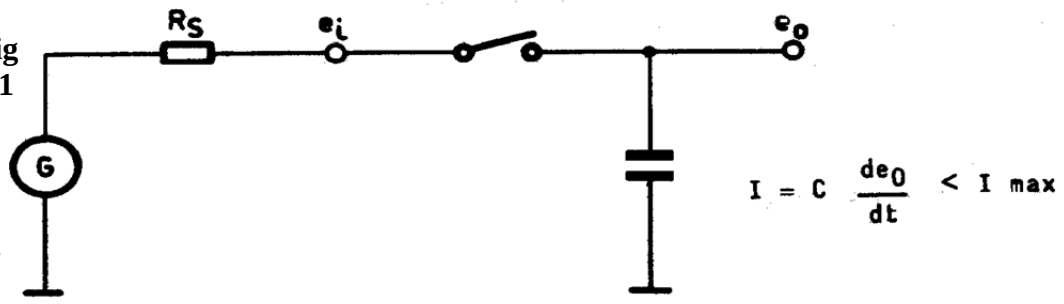


Fig 7.1

Module Description

Sample and hold device featuring operational amplifiers and analog switches
This circuit represents a non-inverting sample and hold with four operational amplifiers and four analog switches.
Operational amplifiers IC_8 and IC_{10}, together with analog switches IC9a and IC9c, make up the classic sample and hold circuit.

As the two analog switches must operate in opposing modes:

HOLD phase:	IC9a = closed	IC9c = open
SAMPLE phase:	IC9a = open	IC9c = close

And as there is only one command, switch IC9b is used to carry out an inversion.
Capacitor C_9 is the HOLD capacitor, and is also referred to as the "data storage capacitor".
Input amplifier IC_8, configured as non-inverting, has a high input resistance and features a potentiometer for calibration of the offset voltage.
Operational IC_{10} is of the FET type, and therefore has a very high input resistance (being connected in a non-inve rting configuration). This means that the di scharge of capacitor C_9 in the HOLD phase is minimal.
The circuit consisting of IC_{9d} and IC_{11} is added in order to minimize the errors introduced by analog switch IC_{9c} and operational amplifier IC_{10}. The errors introduced by these two parts of the circuit are identical (also considering that R_{42} corresponds approximately to the output resistance of operational amplifier IC_8) and are therefore cancelled when applied to the two diffe rential inputs of a mplifier IC_{12} It is important that capacitors IC_9 and IC_{10} are almost identical.
By connecting jack 17 to jack 19, the SAMPL E/HOLD status may be controlled via the SAMPLE/HOLD switch. If jack 17 is conn ected to jack 18, the SAMP LFJHOLD status is controlled by the signal from the GENERATOR

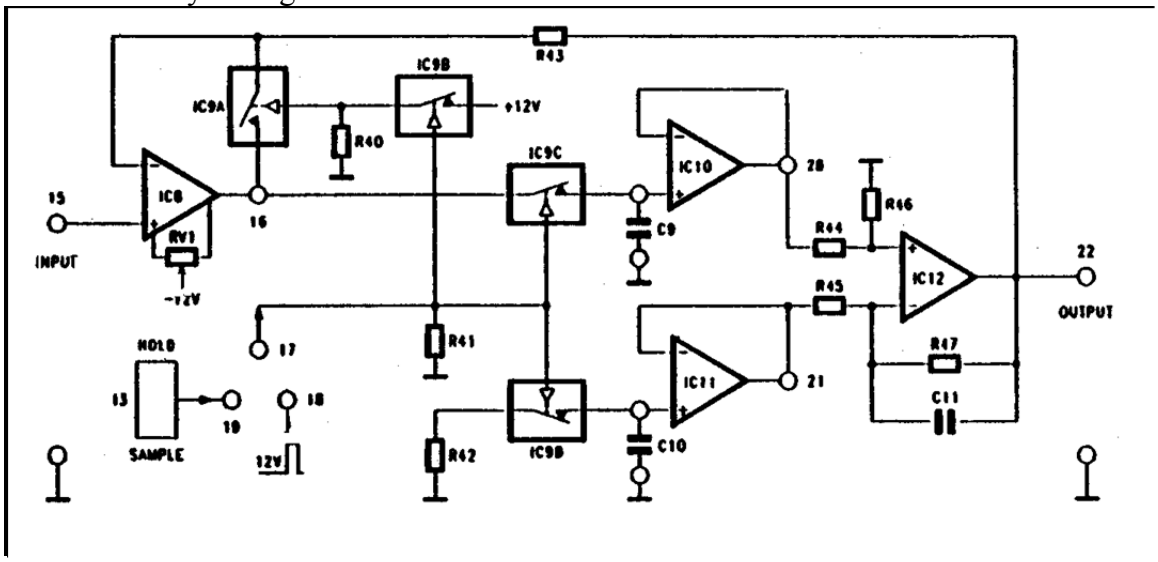


Fig 7.2

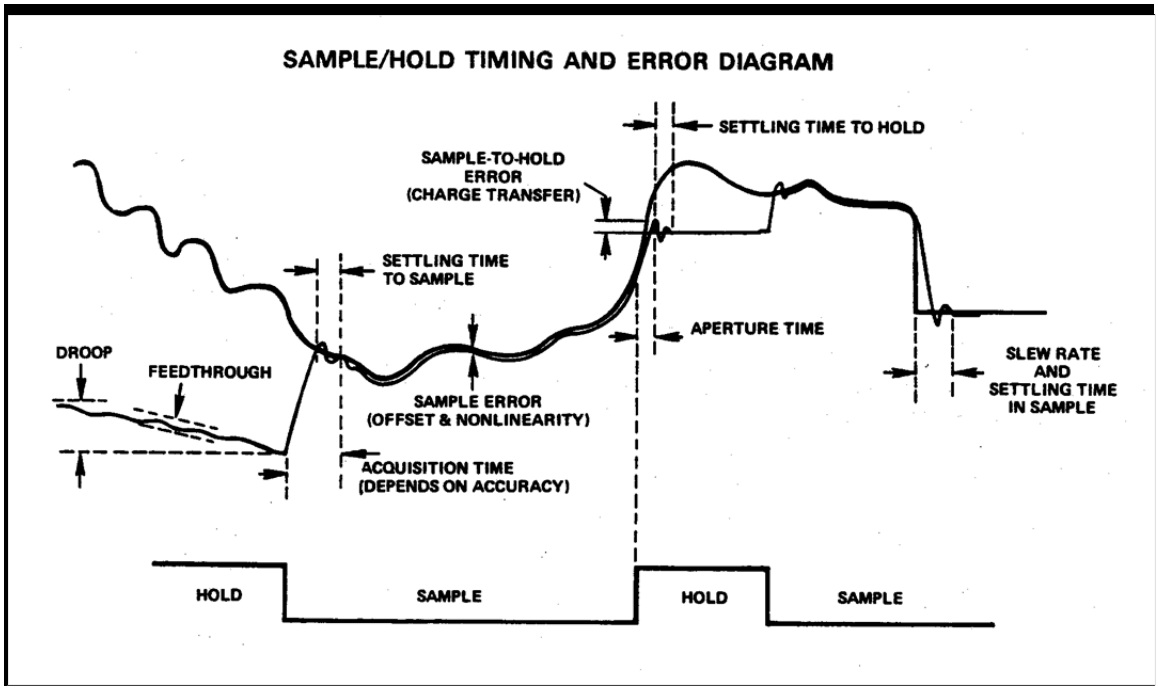


Fig. 7.3

PROCEDURE:

Measuring the acquisition time

Purpose of the exercise

The purpose of this exercise is to measure the time required for transformation of the input signal into an output signal (starting from the beginning of the sampling phase).

Procedure

Connect the ±12V and ground jacks of the panel to a corrected power supply.
Connect jack 17 to jack 18.
Connect jack 7 to jack 5.
Set switch I_2 to 10 KHz.
Adjust the duty-cycle of the potentiometer so that the sample time is 60 µsec and the hold time 10 µsec (turn the knob completely counterclockwise).
Connect jack 3 to jack 15.
Connect one of the probes of the oscilloscope to the output signal between jack 22 and ground. The second probe should be connected first to the sample and hold signal and then to the input signal.
Fig. 7.4 shows the behavior in time of the three signals.

Note the existence of a delay (acquisition time) is approximately 10 to 15µsec between the "start sampling" command signal and the settling of the output signal.

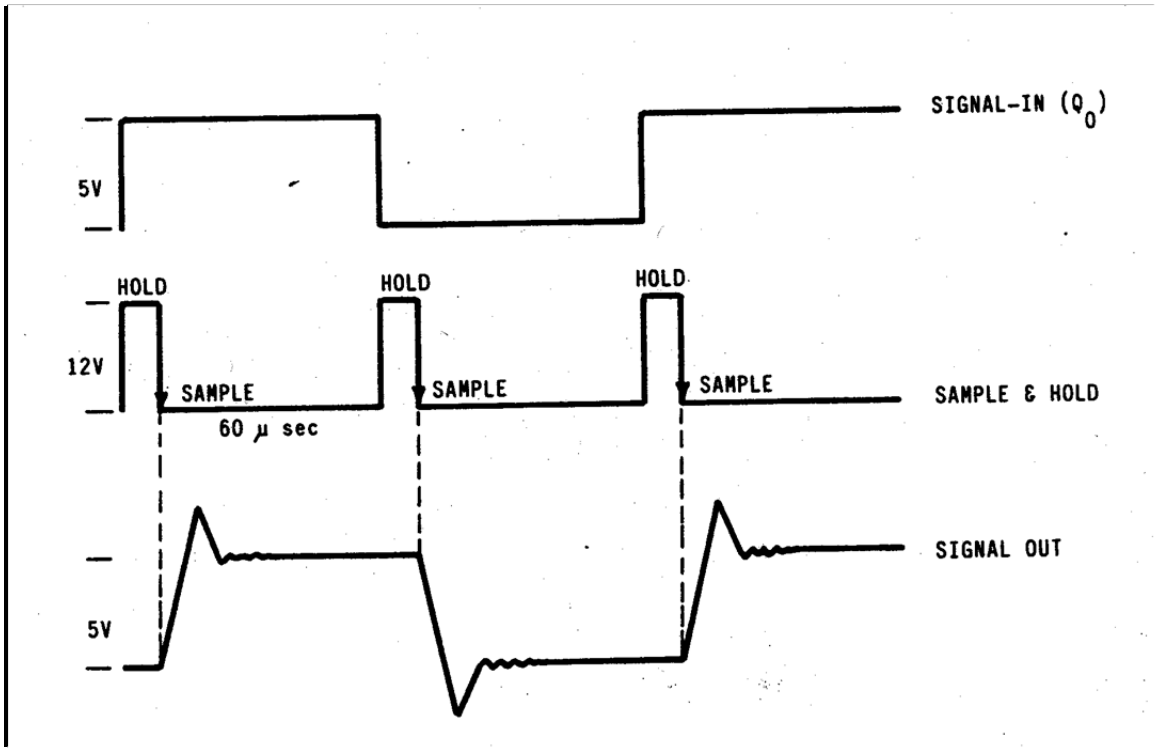


Fig 7.4

Vary the duty cycle of controlling signal (connected to jack 17), and take observations.
Vary the duty cycle and take observations.
Connect the jack 15 and ground to function generator (sine wave of 5V positive with 5 KHz).
Vary the duty cycle of controlling signal (connected to jack 17).
Observe the acquisition times for different duty cycles of sample and hold signal.
Repeat the procedure with triangular wave input

OUTCOME:

The time required for transformation of the square wave input signal into an output signal comes out to be as follows:

APERTURE TIMES:

Rise Time =
Fall Time =

ACQUISITION TIMES:

Rise Time =
Fall Time =

Lab No.8

PURPOSE:

General considerations on the Digital-to-Analog and Analog-to-Digital Conversion and observation of its different parameters.

EQUIPMENT REQUIRED:

- Base unit for the IPES system
- Experiment module F03A
- Digital multimeter.

BASIC THEORY:

An analog-to-digital (A/D) conversion means quantizing the amplitude of a physical quantity (e.g. a voltage) into a discrete levels class. Thus obtaining a series of digits, forming a number of a proper code. Generally the binary code and, consequently, binary numbers are used. Analog data can be obtained again through digital-to-analog (D/A) conversion.

Due to the quantization, each value V of the analog signal included within the interval V_i to V_{i+1} is always quantized at the same level N_i.

The interval: V_{i+1} to $V_1 = Q$, is defined as "quantum level".

Another important parameter of A/D converters is the conversion time since it defines the capacity of the converter to operate the conversion of a variable signal; in fact, remember that the sequence of the quantized levels must allow the regeneration of the original analog signal.

A time-variable signal can be converted into a discrete values class carrying out the sampling and holding operations. The sampling and holding operations are carried out through proper circuits called "Sample and Hold".

Resolution

It defines the smallest standard incremental change in. the output voltage of a DAC or the amount of input voltage change required to increment the output of an

ADC between a code change and the next adjacent code change. A converter with "n" switches can divide the input in 2^n parts: the least significant increment is then 2^{-n}, or one least significant bit (LSB). On the contrary the Most Significant Bit carries a weight of 2-1. Resolution is applied to DACs and ADCs and may be expressed in percent of full scale or in binary bits.

Quantization error

The "ideal" quantization error obtained from the ideal characteristic of the A/D converter. It is the maximum deviation of a straight line of a perfect ADC, from a transfer function. As, by its very nature, an ADC quantizes the analog input into a finite number of output codes, only an infinite resolution would exhibit zero quantizing error. The quantizing error cannot strictly be applied to a DAC; in fact, the equivalent effect is more precisely a resolution error.

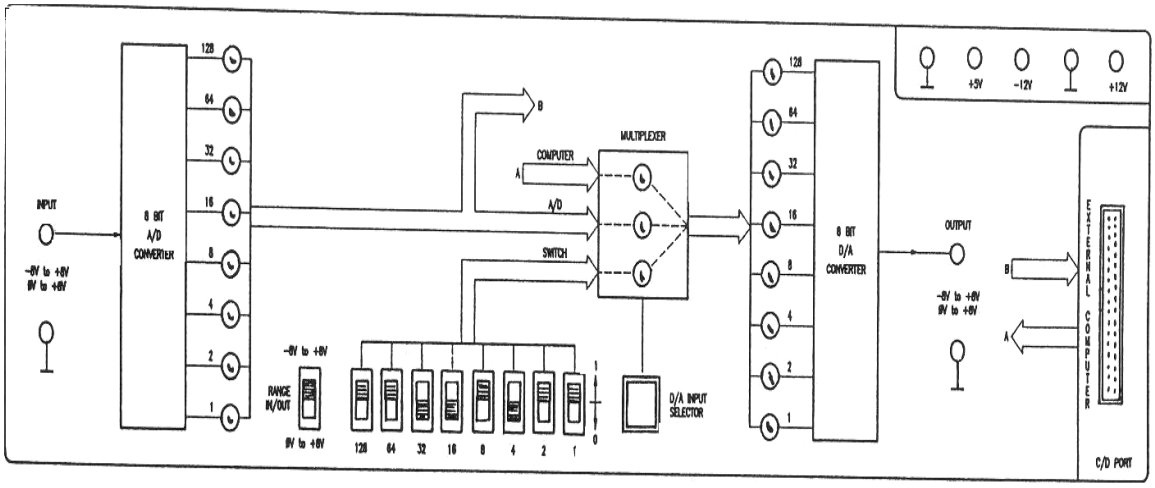
DESCRIPTION OF THE MODULE F03A

This module carries out an educational system of analog-to-digital and digital-to-analog conversion. This system consists of two 8-bit converters of large diffusion. A signal adapter is inserted before the A/D converter. This device permits the conversion of signals coming from conditioners with output range not coinciding with the converter output. The input range is chosen by acting on the IN/OUT selector and can be from 0 to

+8V with the selector down and from -8 to +8V with the selector up. The input of the digital-to-analog converter can come from the analog-to-digital converter, from the computer or from a series of switches installed on the panel. The input connection is chosen through the pushbutton (D/A INPUT SELECTOR) and displayed on the LEDS of

the multiplexer. The equipment must be power supplied with regulated D.C. voltages of +12,-12V and +5V.

Fig 8.1



A/D converter

The A/D converter (ADCO804LCN) operates with an input range included from 0V to +5 V, that is, an input voltage of 0 V generates a digital output signal consisting of a sequence of all 0s , whereas an input voltage of +5volts generates a digital signal of all

1s. Therefore the input signal must be adapted so that the minimum value of its

range can generate an output signal of all 0 and the maximum value of the range generates a digital signal of all 1.

D/A Converter

The digital signal (8 bits) which must be sent to the input of the D/A converter (DACO800) can come from the A/D converter, from the computer or from a set of the 8 switches.
The operational amplifier IC_{1A} has a gain of 0.5 and carries out a shift range of the input signal if the range -8 to +8 is selected, the operational amplifier IC_{1B} makes the extreme range values coincide with 0v and 5v.

Range:

The range of module can be selected through *Range IN/OUT* switch. The range can be 0v to +8v, i.e.

OV = 00000000
+8V = 11111111

or -8v to +8v, i.e.

-8V = 00000000
+8V = 11111111

PROCEDURE:

Set switch *Range IN/OUT* to 0V to 8V.

Resolution measurement:

- Connect the ±12V, +5V and ground jacks of the panel to a corrected power supply.
- Select *SWITCH* option through *D/A input selector*.
- Set the switches (S_{128} to S_1) to any position and note the analog voltage output through multimeter.
- Change the position of switch S_1 (LSB), and note the analog voltage output through multimeter.
- The change in voltages is equal to one resolution.

Binary codes for different voltage levels:

- Connect the ±12V, +5V and ground jacks of the panel to a corrected power supply.
- Select *A/D* option through *D/A input selector*.
- Apply different voltage values to the analog input.
- Read the corresponding binary values on LEDs.
- Note the analog output values of the D/A converter corresponding to the different digital values and compare with the analog input value.

Quantization error:

- Apply some voltage to ADC input.
- Increase the input voltage to maximum value so that the output of ADC does not change.
- Apply maximum change in input voltage for which output shows same value as previous. The change is Quantization error, normally equal to half of the resolution.

Now set the switch *Range IN/OUT* to -8 V to +8 V, and repeat the procedure.

OBSERVATION:

Input Voltage	**Binary Code(0 V to +8 V)**	**Output voltage**
Input Voltage	**Binary Code(-8 V to +8 V)**	**Output voltage**

OUTCOME:

- The resolution of the ADC and DAC, for the switch *Range IN/OUT* position 0 V to 8 V, is….
- The quantization error of the ADC and DAC, for the switch *Range IN/OUT* position 0 V to 8 V, is….
- The resolution of the ADC and DAC, for the switch *Range IN/OUT* position -8 V to +8 V, is….
- The quantization error of the ADC and DAC, for the switch *Range IN/OUT* position -8 V to +8 V, is….

Lab No.9

PURPOSE:

Frequency analysis of the Digital-to-Analog and Analog-to-Digital Conversion, and observation of its different parameters:

EQUIPMENT REQUIRED:

- Base unit for the IPES system
- Experiment module F03A
- Digital multimeter.
- Function generator
- Oscilloscope

BASIC THEORY:

A time-variable signal can be converted into a discrete values class carrying out the following operations:

Sampling operations: This is conversion of continuous time into discrete time, through which the instantaneous values of the analog signal are separated. The frequency of the sampling signal must guarantee the complete regeneration of the original signal. At this point, consider the sampling theorem stating that, if B is the bandwidth of the analog signal, the minimum sampling frequency must be equal to 2 B.

Therefore $F \geq 2\ B$

Sampling frequency: Analog signal is sampled at sampling frequency. The relation between analog and digital frequencies is:

Digital frequency = analog frequency / sampling frequency

$$f = F/Fs$$

Periodic sampling of continuous-time signal implies a mapping of the infinite frequency range for the variable F (or Ω) into a finite frequency range for the variable *f(*or ω*)*. Since the highest frequency in a discrete time signal is $\omega = \pi$ or $f = ½$, it follows that, with a sampling rate F_s, the corresponding highest values of F and Ω are

$$Fmax = Fs/2 = 1/2T$$
$$\Omega max = \pi * Fs = \pi/T$$

Quantization operation: This is conversion of discrete time continuous valued into a discrete time discrete valued (digital) signal. it holds a constant value during the whole conversion time of the A/D converter. Actually the sampled value is held until the next sampling.

Coding: In the coding process, each discrete value is represented by a binary sequence.

PROCEDURE:

- Connect the ±12V, +5V and ground jacks of the panel to a corrected power supply.
- Select *A/D* option through *D/A input selector*.
- Apply different voltage values to the analog input.
- Read the corresponding binary values on LEDs.
- Note the analog output values of the D/A converter corresponding to the different digital values and compare with the analog input value.

Response to a square, triangular, sine wave:

Set the selector of IN/OUT RANGE to "-8 to +8 V".

- Select *A/D* option through *D/A input selector*.
- Apply a sine wave with frequency of 1 kHz and amplitude not exceeding, ±8 V, to the input.
- Display the signal after the double conversion on oscilloscope.
- Compare its wave shape, amplitude, and phase shift with those of the input signal.
- Repeat the test with a triangular wave and with a square one.

Frequency response:

- Repeat the last test and increase the frequency of the input signal.
- Note the frequency up to which the signal reconstruction is correct.

Set the selector of IN/OUT RANGE to "0 to +8 V".
Check the response to a sine, triangular, and square wave, with different frequencies.

OUTCOME:

The maximum frequency of the sine wave input up to which output can be reconstructed comes out to be: _____.
The most effected wave type by increasing frequency is: _____.
The least effected wave type by increasing frequency is: _____.

Lab No.10

PURPOSE:

Implementation of Full Adder
Description of the module E18/EV
Illustration of gate delay of a TTL Inverter

EQUIPMENT REQUIRED:

- Base unit for the IPES system
- Experiment module E18/EV
- Digital multimeter
- Function generator
- Oscilloscope
- Bread Board
- 7408 (AND)
- 7432 (OR)
- 7486 (XOR)
- 7486 (XOR)

BASIC THEORY:

DESCRIPTION OF THE MODULE

The educational module E18 consists in a printed circuit on which digital logic circuits (TTL and CMOS) are mounted performing the following functions:

No. of circuits	Name of circuit	IC
-6	Inverters	74LS04
-4	2- input AND ports	74LS08
-4	2-input NAND ports	74LSOO
-4	2- input OR ports	74LS32
-4	2-input NOR ports	74LS02
-4	2-input EX-OR ports	74LS86
-2	TTL-CMOS and CMOS-TTL interfaces	MM74C906
-4	J-K Flip-Flops	74LS76
-1	4-bit full Adder	74LS83
-1	4-bit Shift-register	74LS95
-1	Synchronous BCD counter	74LS160

-1	BCD decoder and display driver	74LS247
-1	7-segment display	HDSP5301
-1	Sync up/down counter	74LS192
-1	9-bit parity generator	74LS280
-1	Monostable	74LS221
-1	Multiplexer	74LS153
-1	Demultiplexer	74LS155
-1	BCD to decimal decoder	74LS42
-1	Encoder	74LS147
-1	Three state buffer	74LS125
-1	Latch	74LS75
-1	4-bit comparator	74LS85
-1	4-bit preselector	PICO-D-137-AK-1
-1	Clock generator (1 Hz, 10 kHz)	74LS14
-2	Push- buttons	4/6417
-8	Switches	4/7201
-10	LEDs	TIL210
-4	NAND ports with two CMOS inputs	CD4011
-2	20-pin terminals	

The components are mounted to carry out the experiments more quickly especially more complex circuits.
The connections between terminals of the devi ces are carri ed out b y means of electri cal cables and proper tubes present on the module and, electrically connected to the terminals of the integrated circuits. Each integrated circuit shows the silk screen printed logical diagram. The functions related to the IC are shown and terminals (In-Out) are indicated.

Implementation of the full-adder circuit, using the module E18/EV:

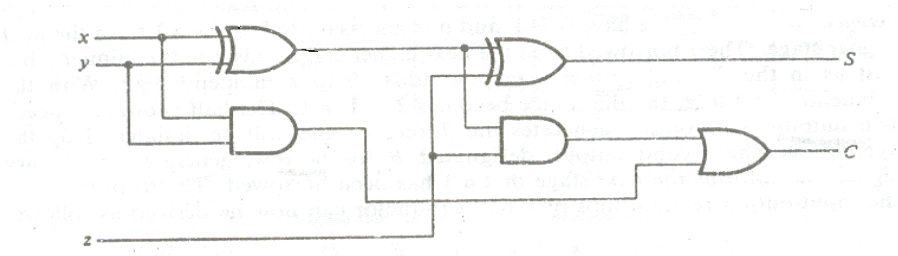
Full- Adder

A full-adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two of the input variables, denoted by *x* and *y*, represent two significant bits to be added. The third input *z*, represents the carry from the previous lower significant position. Two outputs are necessary because the arithmetic sum of three binary digits ranges in value from 0 to3 and binary 2or 3 needs two digits. The binary variable *S* indicates the sum and *C* the carry. The binary variable *S* gives the value if the least significant bit of the sum. The binary variable *C* gives the output carry.

PROCEDURE:

- Implement the circuit of full adder on bread board.
- Supply the required power (5V) to ICs AND OR and XOR
- Check the output using logic probe. And fill in the truth table.

Fig.10.1



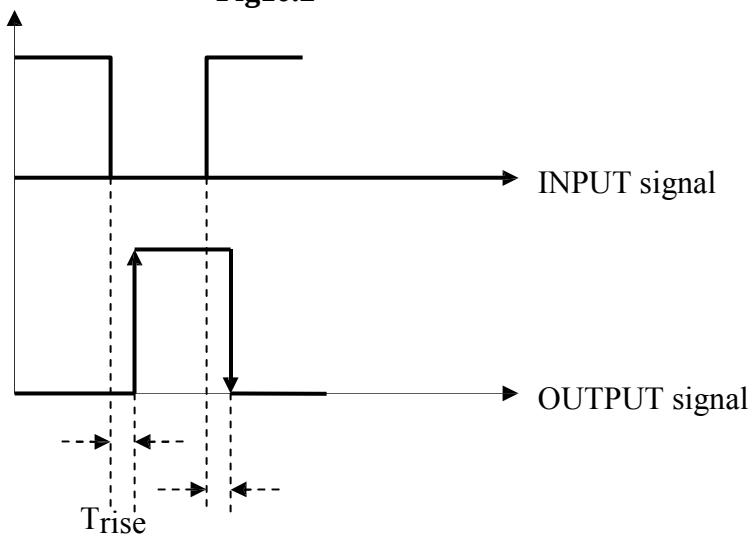
Measurement of gate delay of a TTL inverter:

Gate delay: Gate delay is the time taken by an IC to respond the change in input.

PROCEDURE:

Connect the +12V, +5V and ground jacks on the module to a corrected power supply.
Connect +5V and ground of the HEX INVERTER to a corrected power supply.
Send a rectangular signal from the function generator to input of HEX INVERTER (amplitude 5V positive, frequency 50 KHz).
Connect one of the probes of the oscilloscope to the generator signal and the other to the corresponding output signal of the HEX INVERTER.
Measure the gate delay between the output signal and the input signal.

Fig10.2



OUTCOME:

The gate delay of a TTL Inverter comes out to be: _____

The resulting truth table of the adder circuit is as follows:

x	*y*	*z*	*C*	*S*
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Lab No.11

PURPOSE:

To study the Basic Characteristics of Flip-Flops

EQUIPMENT REQUIRED:

- Base unit for the IPES system
- Experiment module E18/EV

Theory:

Introduction

The bistable multivibrator, commonly called flip- flops, are the most common form of digital memory elements. A memory element is generally a device which can store the logic state 0 or 1, called information "**bit**". The memory elements enable the storing of digital information for further uses. They permit to carry out complex sequential digital circuits, which took to the construction of modern calculators.

R-S Flip-flop (latch)

A main memory circuit can be carried out with the crossed coupling of two NAND ports: this kind of connection is called R-S flip- flop. Fig. 9.1 a) shows the diagram carried out with NAND ports, while fig.9.1 b) shows the symbol.
Similarly, to carry out the same flip- flop, it is also possible to use some NOR ports.

TRUTH TABLE OF THE R-S FLIP FLOP
X= Last state
?= indefinite state

S	R	Q	Q`
0	0	X	X
0	1	0	1
1	0	1	0
1	1	?	?

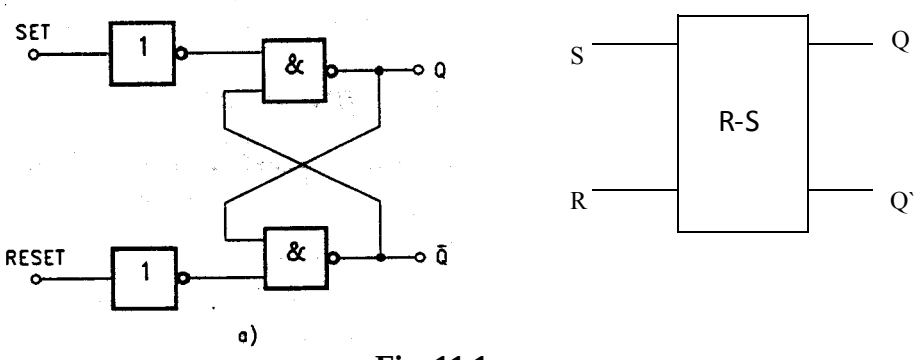


Fig. 11.1

Suppose a data is to be inserted in the flip-flop; the input levels are: SET = 1 and RESET = O. The output level of the port 1 is low (0) and this determines a high state across the output of port 3 (Q = 1). The output of port 2 is instead at 1, so port 4 finds two high levels (port 2 and 3) across its inputs, and takes its output to a low level (Q = 0).

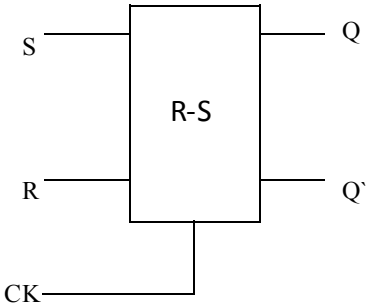
The flip-flop is now on SET, with memorized information. Now, applying a high level across the RESET terminal, keeping the SET to a low level (s = 0 and R = 1), the flip- flop switches, i.e. it changes state, and the output becomes Q = 0 and Q = 1. In this case we say that the flip-flop is in RESET state. If the inputs SET and RESET are simultaneously applied to a high logic level (S = R = 1), you obtain an indeterminate state:

Q=Q`=1.

When the still state (R=S=O) is reset, the output having the lower transition time is taken high.

R-S Flip-flop with Clock

In sequential systems, the change of state in the flip-flops is often required to occur in synchronism with the clock pulse. This is carried out by modifying the diagram of fig.9.1 into the one of fig. 9.2.



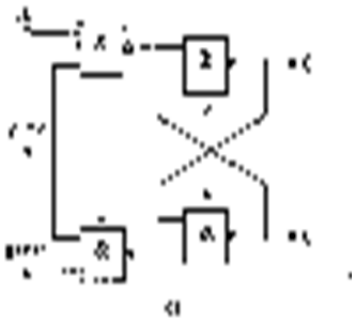


Fig. 11.2

While no input pulse is applied, the flip-flop keeps as it is, independently from the value of Rand S. Applying a clock pulse, if the inputs are R=S=O, the flip-flop keeps stable with the last output (Qn+1 = Qn). If instead we have: R = 0 and S = 1 the output of port 1 goes to 0 enabling the switching. In correspondence to a new clock pulse, if: R=1 and S=O, the latch changes state again and its outputs are: Q=O and Q=1.
In the case in which: R=S=1 on arrival of the clock pulse, the outputs of the flip-flops should both go to 1.

J-K flip-flop

The J-K flip-flop is formed by the R-S with clock, in which the outputs are taken back to the input, as in fig. 11.3

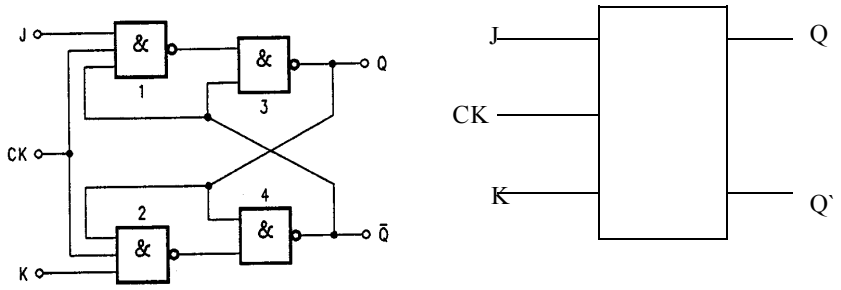


Fig. 11.3

Suppose that the flip-flop is in the state: Q = 0; Q' = 1. If the data input J is at the level 1 in correspondence to the clock pulse, the output of port 1 gets to 0, and the memory cell composed by ports 3-4 changes state: Q = 1 and Q' = 0
This flip-flop enables the removal of the uncertainty there was in the flip-flops R-S with clock, when the inputs were both at level 1. In fact, if:

Q=1 Q'=O J=K=1

on arrival of the clock pulse, only port 2 enables the passage of the input data, while port 1 blocks them. The level 0 obtained across the output of port 2 makes the memory element switch (port 3 and 4). So, we have seen that when the inputs are both high there is no uncertainty, but the output state changes.

J-K Master-Slave Flip-flop

In the J-K flip-flops there can be possibility of uncertainty, if the clock pulse duration is too long in respect to the propagation times.
Considering that the flip-flop is in the following conditions:

Q=O Q'=1 J=K=1

When the clock pulse is applied, after the propagation time "t" of the ports, the output becomes: Q = 1 and Q' = 0
But being all the inputs signals still active, the outputs would tend to oscillate between 0 and 1, and at the end of the pulse, the state of the flip-flop is uncertain. To solve this inconvenience, the flip-flop type J-K Master-Slave has been introduced, which is commonly called J-K and can be seen in fig. 11.4.

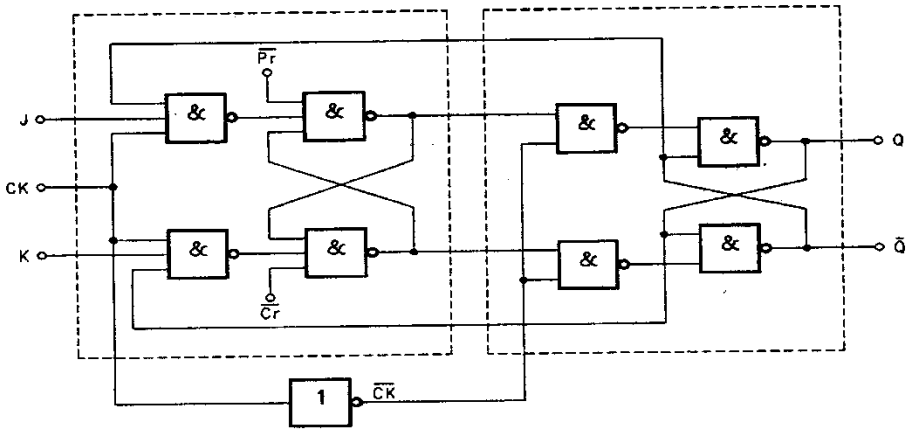


Fig 11.4

It consists in a cascade connection of two R-S flip-flops, with reaction from the output of the second one, called SLAVE, to the input of the first, and called MASTER. Some pulses inverted in respect to the ones applied to the Master are applied across the input of the Slave. If the PRESET and CLEAR inputs are not active (Pr=Cr=1), on arrival of the clock pulse, the Master can change logic state according to the following truth table:

Pr = Cr = 1

t_n		t_{n+1}
J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n

As, during the period in which the clock pulse is high, the Slave keeps blocked, the outputs Q and Q` are not changed. When the clock passes from 1 to 0, the Slave switches, and the Master blocks. In other words, the data present across J and K are transferred first to the Master, during the positive part of the clock pulse, and then to the Slave, during the negative part: in this way, the uncertainties across the outputs are removed.

D Flip-flop

If a J-K flip-flop is modified by adding an inverter (as shown in fig.11.5 a), so that the input K is complement of J, the set is known as flip-flop type D, in which D=DATA (fig.9.5 b). Its operation is simple: when a clock pulse arrives, the data present across the input is transferred and kept across the output.

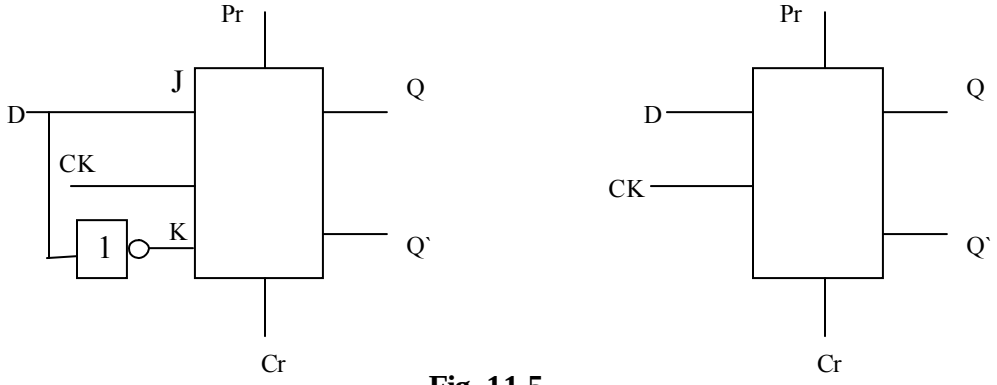


Fig. 11.5

T Flip-flop

If the inputs J and K are set always at logic level 1 on a flip-flop J-K, so this is a flip-flop commonly called type T (T means TOGGLE).It inverts the state of the outputs each time the input pulse applied to line T passes from the state 1 to the state O. Fig.9.6 shows the diagram (a) and the logic symbol (b) of a flip-flop type T.

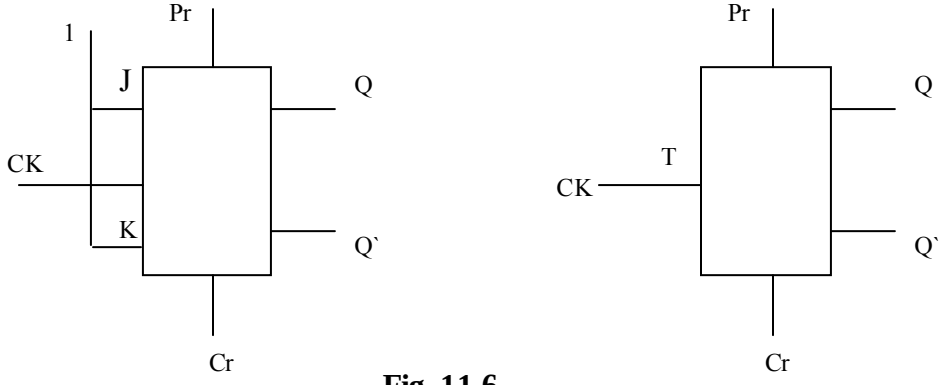


Fig. 11.6

Procedure:

Analysis of an R-S Flip-flop

Procedure

- Carry out a flip-flop type R-S using NAND and NOT ports, as in fig.11.1
- Connect the SET and RESET inputs to two switches.
- Connect the outputs Q and Q to two LEDs.
- Power the module.
- Turn the SET input, with the switch, to 1 and then to 0.
- Analyze the behavior of the outputs.
- Set the RESET line to 1, and then to 0.

- Analyze the behavior of the outputs again.
- Repeat some times the operations with the switches and check the carried out memorizations.
- Now, try to set both inputs to 1 and explain what the reason of the uncertain state is.

S	R	Q	Q`
0	0		
0	1		
1	0		
1	1		

Construction and Analysis of a J-K Flip-flop

Procedure

- Carry out the circuit of a J-K flip-flop as in fig. 11.3.
- Connect the inputs J and K to two switches, and the outputs to two LEDs.
- Connect the terminal of the clock at the bottom on the left to the input CK of the built up flip-flop, as well as to a led, to display the behavior.
- Power the module. ,
- Set the switches connected to the inputs alternatively high. :

- Analyze the behavior of the LEDs.
- Now, set both switches to the logic level 1, and explain the behavior of the flip-flop.

Comparison between J-K and J-K Master Slave Flip-flop

- Keep the circuit of the last exercise.
- Connect the switch of the input J also to J of an integrated flip-flop J-K (Master-Slave) present on the module.
- Carry out the same connection also for the inputs K and CK.
- Connect the outputs of the new flip-flops to other 2 LEDs.
- Power the module.
- Set the switches alternatively high and detect the differences between the two devices.
- Now, set both switches to 1 and analyze the behavior of the new flip-flop.

t_n		t_{n+1}
J	K	Q_{n+1}
0	0	
0	1	
1	0	
1	1	

Checking the Operation of a Flip-flop D

- Carry out the circuit of fig. 11.5 a) of a flip-flop type D by means of J-K flip-flops
- Connect the inputs P and R to 1.
- Check the operation of the flip-flop D by means of switches 0-1 of the input D and the Clock.

t_n	t_{n+1}
D	Q_{n+1}

Checking the Operation of a Flip-flop T

- Carry out the circuit of fig. 11.6 a) of a flip-flop type T by means of J-K flip-flop
- Connect the inputs P and R to 1.
- Check the operation of the flip-flop T by means of switches 0-1 to the Clock input.

t_n	t_{n+1}
T	Q_{n+1}

Lab No.12

PURPOSE:
To implement

a) 2-bit counter circuit
b) Frequency divider circuit

Using JK-Flip-Flop

EQUIPMENT REQUIRED:
Base unit for IPES system
Experiment module E18/EV
Oscilloscope

THEORY:
Counters are digital integrated devices which can state in a well-defined sequence, applying a train pulse across the input.

They are carried out with flip-flop and logic port stages, where each stage supplies an output which, together with the others, indicate the number of pulses received in binary form.

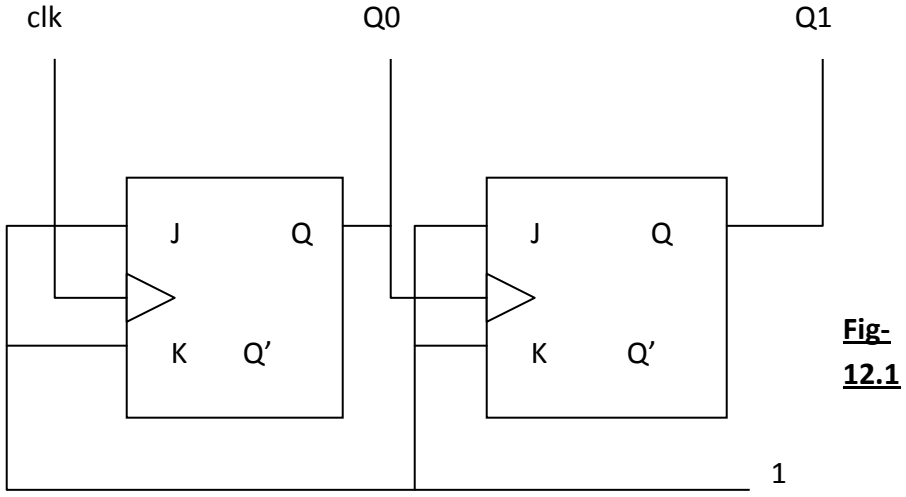


Fig-12.1

These counters are also called 'BINARY COUNTERS' and can be used apart as counters as frequency dividers, supplying the o/p with a pulse after 'n' input pulses.

If we apply a fixed frequency pulse train to a counter, rather than individual pulses coming at random intervals, we begin to notice some interesting characteristics and useful relationships between the input clock signal ad the output signal.

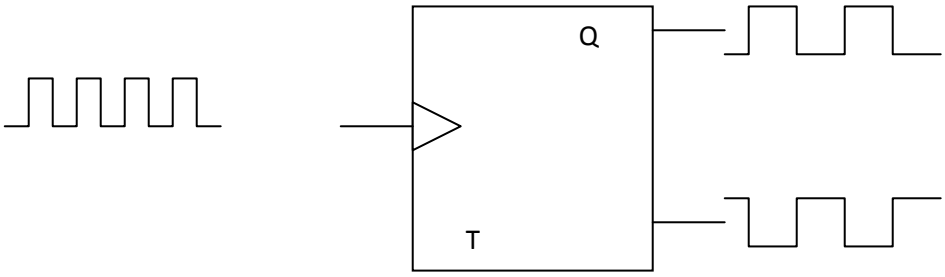


Fig 12.2

Consider a single flip flop with a continuous succession of clock pulses at a fixed frequency, such as the one shown above. We note three useful facts about the output signals seen at Q and Q' :

a) They are exactly inverted to each other
b) They are perfect square waves (50% duty cycle)
c) They have a frequency just half that of the clock pulse train

The duty cycle of any rectangular waveform refers to the percentage of the full cycle that the signal remains at logic 1. If the signal spends half its time at logic 1 and the other half at logic 0, we have a waveform with a 50% duty cycle. This describes a perfect, symmetrical square wave.

Frequency division by an odd number is also possible. The circuit shown below is a demonstration of a divide-by-3 counter. No gates are required to control the sequence if JK-flip flops are used; feeding the output signals back to the appropriate inputs is sufficient.

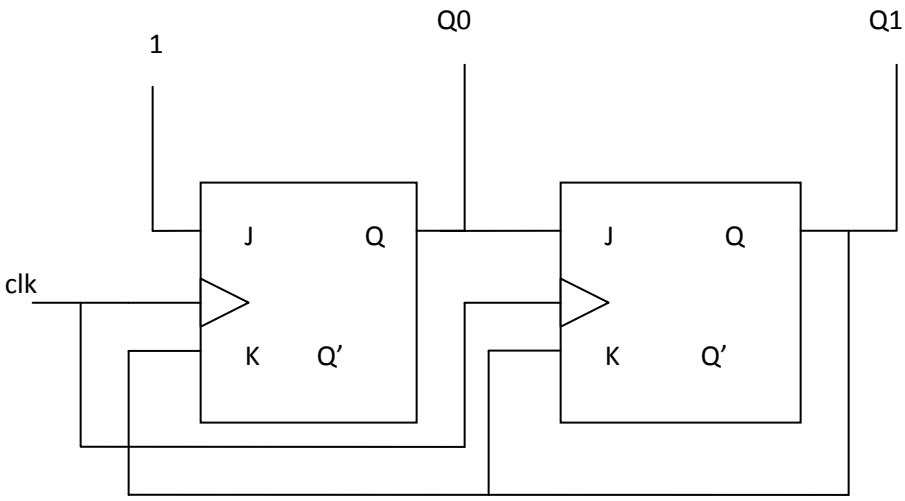


Fig-12.3

Of course it is not possible to get a symmetrical (50% duty cycle) square wave with this circuit. Q0 is at logic 1 for two clock pulses out of three; Q1 is at logic 1 for one clock pulse out of 3. Thus duty cycle of 1/3 (33.33%) and 2/3 (66.67%) are available.

Other counting sequences are also possible. If a need exist to have two or more signals in a particular frequency relationship with each other, some extension or variation on the circuits shown can be designed to meet the need.

PROCEDURE:

a) 2-bit Asynchronous Counter:

- Carry out the circuit of Fig 12.1, a 2-stage asynchronous counter
- Connect all inputs, J and K to logic 1 (i.e +5V)
- Connect 1Hz clock to input CK of first flip-flop
- Connect Q0 to CK of second flip-flop
- Connect the two outputs, Q0 and Q1, to decoder/driver
- Connect the outputs of decoder/driver to respective inputs of display
- Power the module and analyze the operation of complete system

b) Frequency Divider

- Carry out the circuit of Fig 12.3
- Connect the CK (clock) input of both flip-flops to external 1Hz clock
- Connect both the K input to Q1
- Connect Q0 to J input of second flip-flop
- Connect J-input of first flip-flop to logic 1 (+5V)

- Connect first channel of oscilloscope to clock input and second to Q0
- Now disconnect second channel and connect it to Q1
- Observe the frequencies of Q0 and Q1 with respect to input clock frequency

OUTCOME:

The output frequency at Q0 = _____.

The output frequency at Q1 = _____.

Lab No.13

PURPOSE:
To observe the propagation and transition times of CMOS and TTL gates

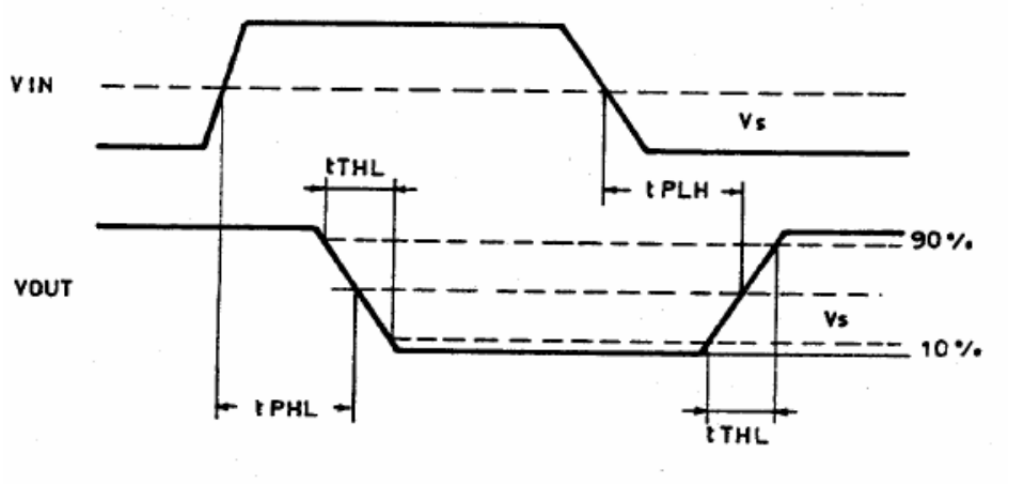
EQUIPMENT REQUIRED
- Module mod.E05a
- Power supply unit (+5 V and ±12 V)
- Dual trace oscilloscope
- Function generator

THEORY:

INTRODUCTION:

Propagation delay times
The following values are normally specified by the manufacturers for any log1C gate:
a) $\mathbf{t_{PHL}}$: propagation delay time with output changing to the low level.
b) $\mathbf{t_{PLH}}$: propagation delay time with output changing to the high level.
The propagation delay times must be measured inside the fixed threshold values, which for the most part is the 50% of the whole signal varia tion.

Transition times
The following transition times are normally declared by the manufacturer:
a) $\mathbf{t_{THL}}$: transition time with output changing to the low level.
b) $\mathbf{t_{TLH}}$: transition time with output changing to the high level.
The time measurement is between the 10% and the 90% of the whole signal variation.
Fig. 13.1 shows the propagation delay time and the transition time of an inverting gate.



PROCEDURE:

Fig 13.1

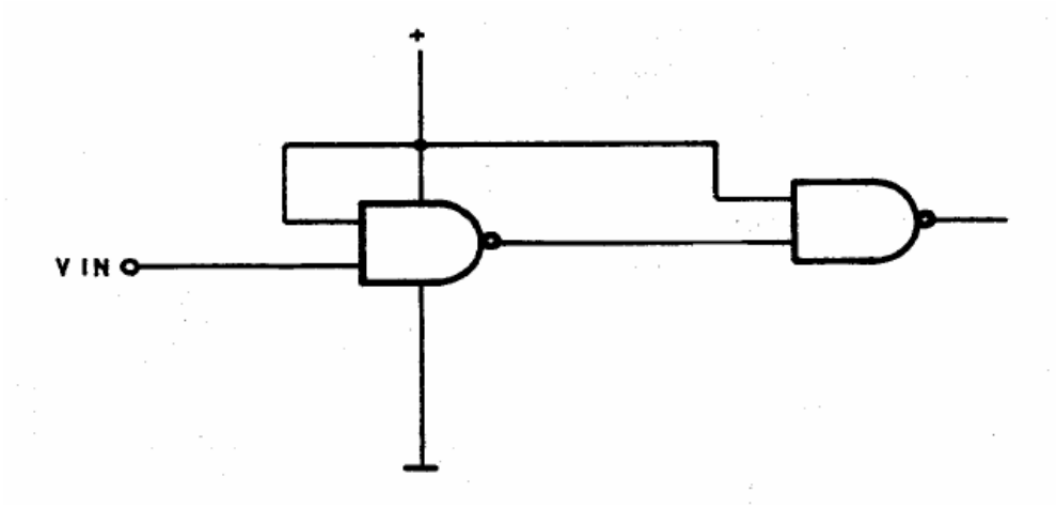


Fig 13.2

- ✍ Assemble the circuit of figure 10.2 with CMOS gates:
- ✍ Set the function generator for a 0-12V square wave and a frequency of 1 MHz.
- ✍ Connect the module to the power supply (+12V).
- ✍ Connect one of the CMOS gate input to the function generator output and the other one to the positive of the power supply input.

NOTE: Connect the input signal to the devices only when the func tion generator is ON, after the input signal has been correctly set and the device itself has been powered.

- ✍ Connect the gate output to the first input of the oscilloscope.
- ✍ Connect the output of the first gate to another CMOS gate input and to the second input of the oscilloscope.
- ✍ Superimpose the present signals and find the output signal delay time in respect to the input one, for 1 to 0 and 0 to 1 transitions.
- ✍ Measure the 0 to 1 and the 1 to 0 transition, times considering the voltages equal to 10% and 90% of the signal maximum;
- ✍ Repeat the procedure with TTL gate.
- ✍ Compare the speed of the devices, with other families. Figure 13.2

OUTCOME:

- ✍ The **t PHL** of CMOS gates comes out to be: _____
- ✍ The **t PLH** of CMOS gates comes out to be: _____
- ✍ The **t THL** of CMOS gates comes out to be: _____
- ✍ The **t TLH** of CMOS gates comes out to be: _____

- ✍ The **t PHL** of TTL gates comes out to be: _____
- ✍ The **t PLH** of TTL gates comes out to be: _____
- ✍ The **t THL** of TTL gates comes out to be: _____
- ✍ The **t TLH** of TTL gates comes out to be: _____