PRACTICAL WORK BOOK

For Academic Session 2014

DIGITAL ELECTRONICS

(EL-335) For T.E (EL)

Name: ____________________

Roll Number: ____________________

Batch: ____________________

Department: ____________________

Year: ____________________

Department of Electronic Engineering

NED University of Engineering & Technology, Karachi

LABORATORY WORK BOOK

For The Course

EL-335 Digital Electronics

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The Board of Studies of Department of Electronic Engineering

Introduction

The work book emphasizes on the basic components of digital electronics including op-amps, analog switches, different ICs, sample-and-hold circuit, ADC and DACs. All these components are pre fabricated on experiment modules, so students do not need to assemble any thing manually. These study modules are provided with complete power supply block and different electronic components so that different circuits can be established through jumpers and connecting wires. This makes it easy to observe the circuit and more time is at its disposal for observation rather then wasting time in assembling. Apart from this students will acquire comprehensive knowledge of equipments like Digital Multimeter, Function Generator and Digital Oscilloscope.

By attaining knowledge of these equipments, components and accouterments students will be capable of designing, analyzing and observing an electronic circuit.

Digital Electronics Laboratory

CONTENTS

Lab No.1

PURPOSE:
To produce an astable multivibrator with:
Symmetrical square wave output
Non-symmetrical square wave output

EQUIPMENT REQUIRED:

- Base unit for the IPES system
- Experiment module MCM7/EV
- Digital multimeter
- Function generator
- Oscilloscope

Theory:
With an astable multivibrator, the op amp operates only in the non-linear region. So its output has only two voltage levels, Vmin and Vmax. The astable continually switches from one state to the other, staying in each state for a fixed length of time. The circuit of an astable multivibrator is shown in figure f7.01. Note that this circuit does not need an input signal. To find out the relations governing the operation of the astable, we start with the usual hypothesis that the operational amplifier has an ideal behavior. Suppose the output is in the state Vo = Vmax. When Vo takes this value the voltage V_{Al} of the non inverting input is:

$$V_{Al} = Vmax .R\ 1/ (R1 + R2)$$

The capacitor C starts charging through resistor R towards the value Vmax. This charging continues until the voltage V_B of the inverting input reaches the value V_{Al}. At this point, as the inverting input voltage is more than the non-inverting input, the output switches low, to Vmin. The voltage V_{A2} is now given by:

$$V_{A2}= Vmin .R1 / (R1 + R2)$$

At this point, the capacitor C starts discharging through R towards the voltage Vmin until it reaches the value V_{A2}, at which point the output switches to Vmax .The cycle then starts again.
We have seen that the voltage across the capacitor C can vary from V_{Al} to V_{A2}, so in the period of time when the output is low, at Vmin, the voltage on the capacitor is given by:

$$V_B(t)=Vmin - (Vmin-Vmax*R1/(R1 + R2))*e^{-t/R*C}$$

While in the period of time when the output is at *Vmax,* the capacitor voltage is:

$$V_B(t)=Vmax - (Vmax-Vmin*R1/(R1 + R2))*e^{-t/R*C}$$

The period T1 for which the output voltage is at *Vmax* can be found by calculating the time the capacitor voltage takes to equal V_{Al}. So:

$$Vmax/(R1+R2) = (Vmin/(R1+R2)-Vmax)*e^{-T1/R*C} + Vmax$$

From which:

$$T1=R*C*\ln \frac{Vmax-R1/(R1+R2)*Vmin}{Vmax-R1/(R1+R2)*Vmax}$$

Similarly we can find the period T2 for which the output stays at *Vmin:*

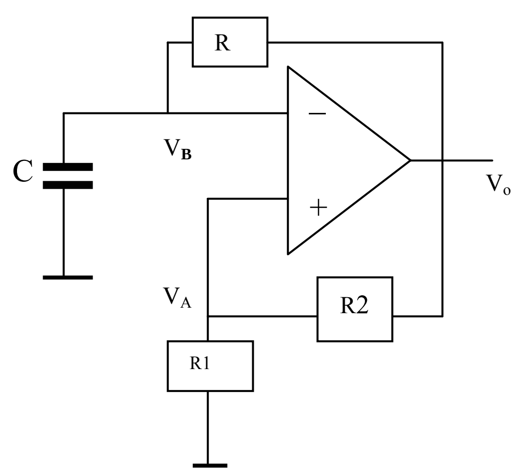
$$T2=R*C*\ln \frac{Vmax*R1/(R1+R2)-Vmin}{Vmax*R1/ (R1+R2)-Vmin}$$

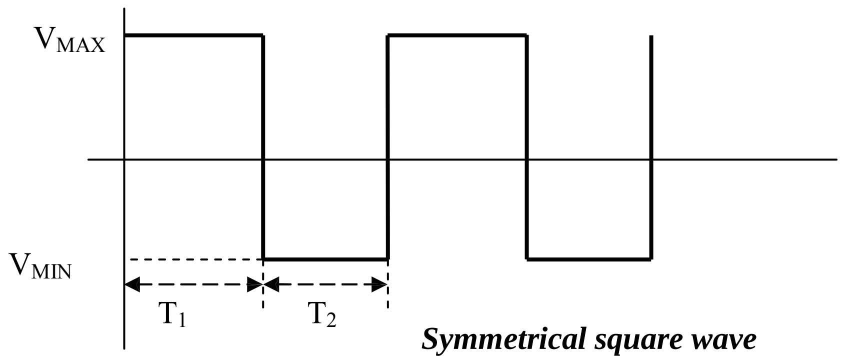
Supposing that *Vmin* = -*Vmax* we obtain:

$$T1=T2=R*C*\ln \frac{1+R1/ (R1+R2)}{1-R1/ (R1+R2)}$$

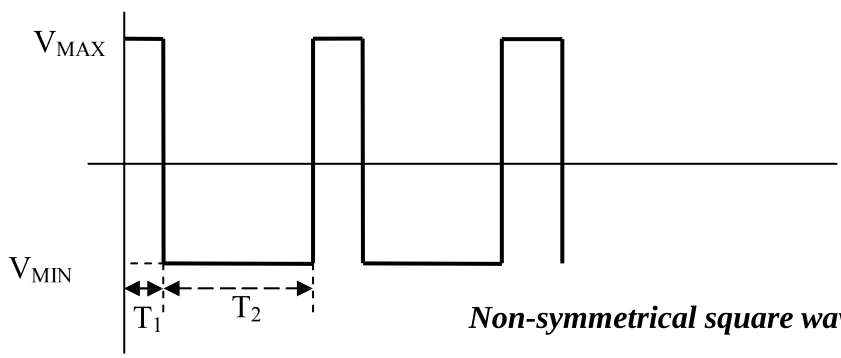
The total period *T* of the square-wave is given by the sum of *T* 1 and *T2.* We can see that the square-wave period and so the frequency can be varied by varying the values of R1, R2, R and C. To obtain an asymmetrical square-wave (duty cycle not 50%) we can make the capacitor charge and discharge through resistors of different values.

Figure
F1.1





Symmetrical square wave

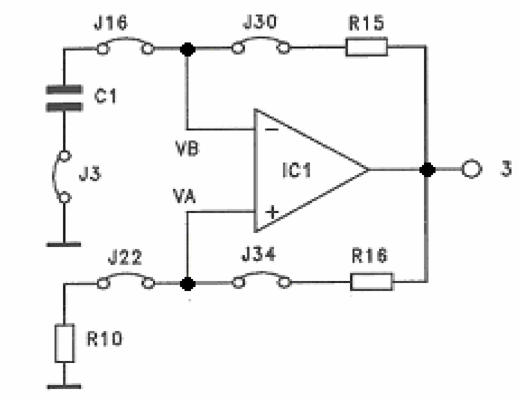


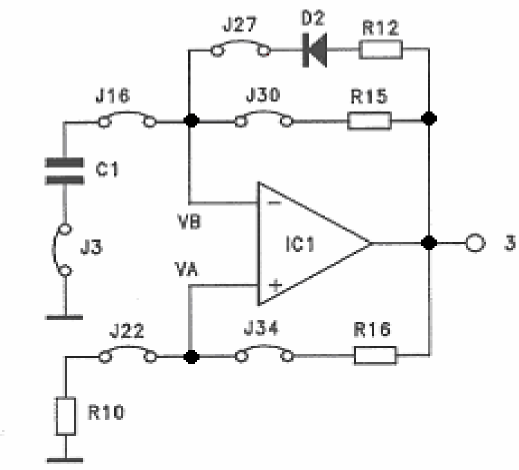
Non-symmetrical square wave

Procedure:

- Insert jumpers J3, J16, J22, J30, J34 to produce the circuit of figure F7.02
- Calculate the output frequency with the formulae.
- Connect the first probe of the oscilloscope to the output V_o of the amplifier and the second probe to the inverting input V_B
- -Measure the frequency with the oscilloscope, and compare it with the theoretical result
- Calculate the capacitor voltages at which output switching occurs, according to the formulae
- Measure the capacitor voltages at which output switching occurs and compare the results with those calculated from theory

Figure F1.2 Figure F1.3





- Now connect jumper J27, to produce the circuit of figure F7.03
- Connect the first probe of the oscilloscope to the output of the A_l operational amplifier and the second to the inverting input VB
- Calculate the values of T1 and T2 as given by the formulae.
- Measure the values of T1 and T2 with the oscilloscope.

Observation(Symmetrical square wave):

S.NO.	Quantity	Observed Value	Calculated Value
1	$V_{B\ (P\text{-}P)}$		
2	$V_{O(P\text{-}P)}$		
3	Frequency		
4	Vmax		
5	Vmin		
6	Capacitor charging time		
7	Capacitor discharging time		

Outcome:

- The approximate frequency of the oscillation of the astable multivibrator (Symmetrical square wave), when R1=R2=10k and R=100K, C = 68nf and Vmin = -Vmax comes out to be: $1 / T_1+T_2 =$

Observation(Non symmetrical square wave):

S.NO.	Quantity	Observed Value	Calculated Value
1	$V_{B\ (P-P)}$		
2	$V_{O(P-P)}$		
3	Frequency		
4	Vmax		
5	Vmin		
6	Capacitor charging time		
7	Capacitor discharging time		

Outcome:

- The approximate frequency of the oscillation of the astable multivibrator (Non symmetrical square wave), when R1=R2=10k and R=100K, C = 68nf and Vmin
  = -Vmax comes out to be: $1 / T_1+T_2$ =

Lab No.2

PURPOSE:
To determine the frequency and output amplitude of a triangular wave generator
To determine the frequency and output amplitude of a ramp generator

EQUIPMENT REQUIRED:

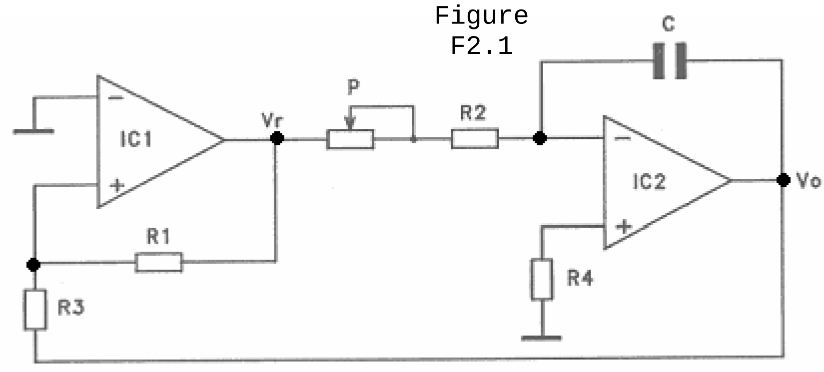
- Base unit for the IPES system
- Experiment module MCM7/EV
- Digital multimeter
- Oscilloscope

Theory:
Among the waveforms that can be generated with op amps, the most common are the triangular, the ramp and the square-wave. A triangular wave can be generated with the circuit of figure F8.01.in which two operational amplifiers are used. The first operates as a comparator, while the second as an integrator. V_O is the output voltage of the integrator, Vr the output voltage of the comparator. The saturation voltages Vmax and Vmin are equal in amplitude, and so can be called +Vr and –Vr respectively. Suppose the output of the comparator is +Vr. The voltage V_O will be a negative ramp which will continue to grow until the voltage of the non-inverting input of the comparator rises above zero. The minimum value of the output voltage V_O, applying the superposition principle, will be given by:

$$0=\frac{Vr*R3 + V_O*R1}{R1+R3}$$

From which we get: $$V_O = -Vr*R3/R1$$

Figure
F2.1



The same principles apply for the maximum voltage the output reaches, with the only difference that the ramp is raising and the voltage Vr is negative: defining this voltage as V_O' we have:

Vo' = Vr *R3 / Rl

To calculate the time T taken to rise from V_O to V_O' remember that the capacitor C charges with a constant current given by:

$$I = Vr / (P+R2)$$

So, from:

$$I = - C*dVo / dt$$

We find that:

$$\frac{Vr}{P+R2} = \frac{-C^* (Vo' - Vo)}{T}$$

From which:

$$V o' - Vo = - \frac{Vr^*T}{C^*(P+R2)}$$

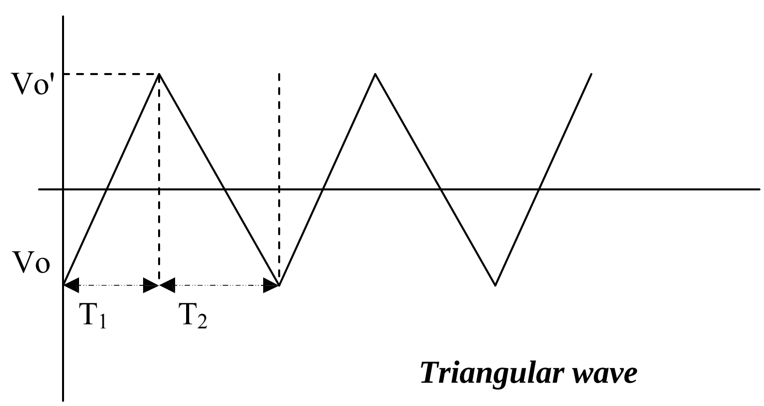
As: $$Vo' - Vo = 2^*Vr^*R3 / Rl$$

we have:

$$T = 2^*R3^*(P + R2)^*C / Rl$$

The time T is equal to half period, so the output frequency F will be the inverse of twice T:

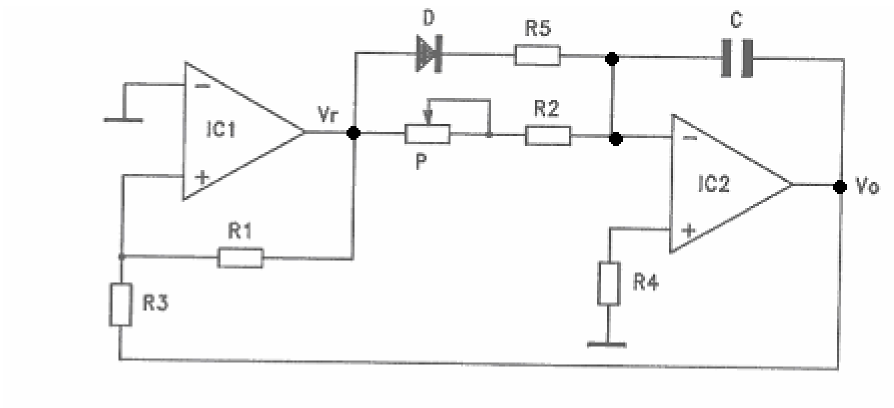
$$F = R1/ [4^*R3^*(R2+P)^*C]$$



Triangular wave

To convert the triangular wave generator to a ramp generator (also known as a saw-tooth) simply insert a diode and resistor in parallel with the potentiometer P and resistor R2. The diagram is shown in figure F2.2

Figure F2.2



Just as with the triangular wave generator, the positive ramp is generated by the current flowing through P and R2 (the diode D is reverse biased), while for the negative ramp the capacitor discharges through a smaller resistance (given by R5 in parallel with the series of P and R2) and so it is faster.
So the time T1 to go from –Vr*R3/Rl to +Vr*R3/Rl is the same as a triangular wave generator, while the time T2 of the return to –Vr*R3/R1 is given by:

$$T2 = \frac{2*R3*R_P*C}{R1}$$

Where: $R_P = (P+R2) // R5$

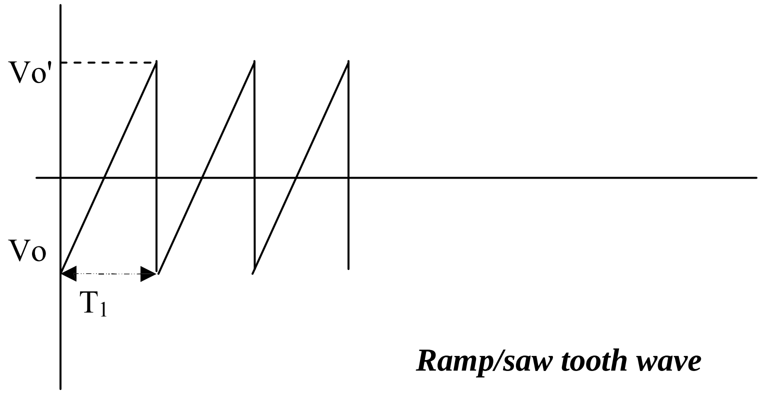
As in module MCM7 the resistance R5 is much less than the value of P and R2, R_P can be considered equal to R5. With this approximation:

$$T2=\frac{2*R3*R5*C}{RI}$$

With the values used in the module, and with the potentiometer all inserted, T2 = 4.4 µsec which can be neglected in comparison with T1 which is about few milliseconds. The frequency of the ramp generator is equal to:

$$F = R1/ [2*R3*(R2+P)*C]$$

To obtain a square wave generator, take the signal from the output of the first op amp, and if the charge and discharge times of the integrator are equal, the output voltage will be symmetrical.



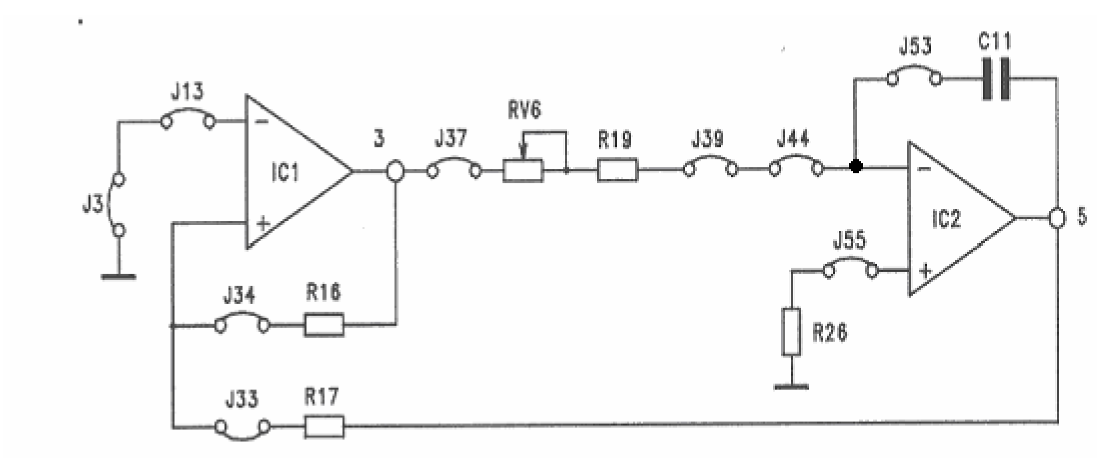
Ramp/saw tooth wave

<u>Procedure:</u>

Triangular waveform generator

- Insert jumpers J3, J13, J33, J34, J37, J39, J44, J53, J55 to the circuit of figure F2.3
- Adjust RV6 completely CCW to obtain zero resistance and the output voltage value of the comparator (terminal 3) using oscilloscope.
- Adjust the trimmer RV6 to half value.
- Calculate the amplitude of the output voltage (terminal 5).
- Measure the amplitude of the output voltage with the oscilloscope.
- Calculate the output voltage frequency according to the formulae.
- Measure the output frequency with the oscilloscope.
- Check the presence of a square wave at the output of the comparator (terminal 3).

Figure F2.3

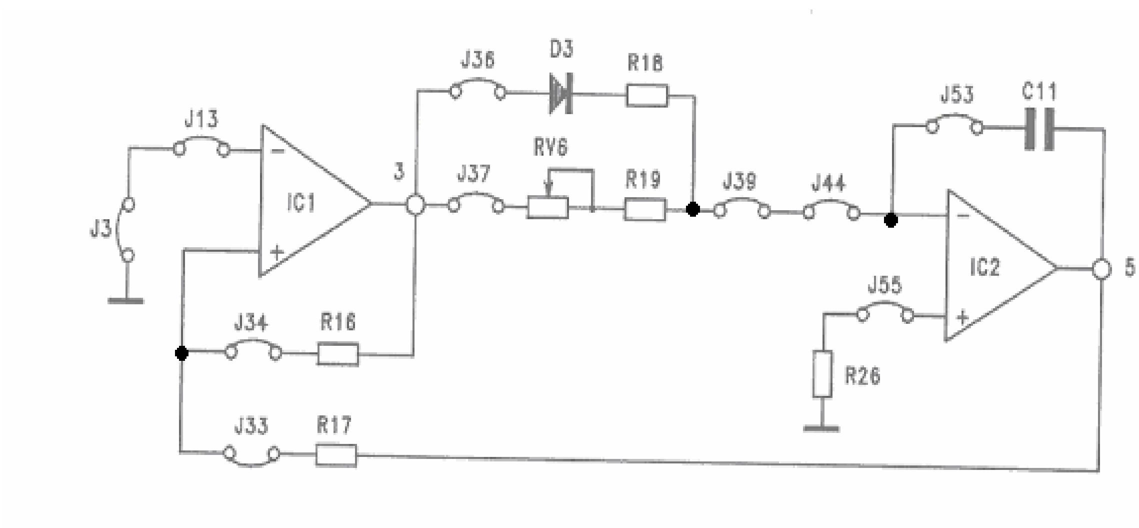


Ramp generator:

- From previous circuit insert J36 to produce the circuit of figure F8.04.
- Adjust RV6 completely CCW to obtain zero resistance.
- Measure the amplitude of the output voltage with the oscilloscope

- Calculate the output frequency using formulae
- Measure the output frequency with the oscilloscope
- Measure the charge and discharge times of the capacitor

Figure F2.4



Observation:

S.NO.	Quantity	Observed Value	Calculated value
1	V_O(triangular)		
2	Frequency (triangular)		
3	V_O (Ramp)		
4	Frequency (Ramp)		

Outcome:

Triangular:

- The approximate frequency of the oscillation of the astable multivibrator comes out to be: ___________.
- The output voltage of the oscillation of the astable multivibrator comes out to be: ___________.

Ramp:

- The approximate frequency of the oscillation of the astable multivibrator comes out to be: ___________.
- The output voltage of the oscillation of the astable multivibrator comes out to be: ___________.

Lab No.3

PURPOSE:

To illustrate the operation and characteristics of the analog switches.

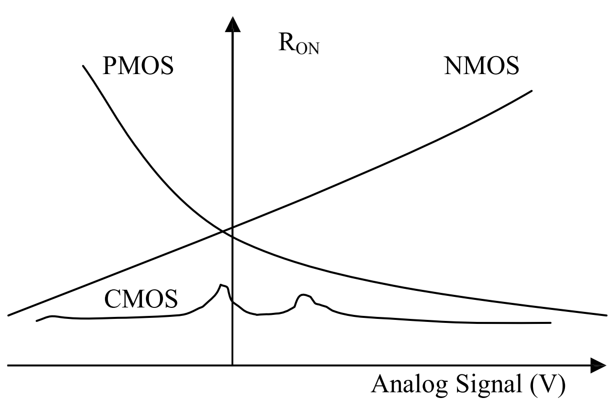
EQUIPMENT REQUIRED:

- Base unit for the IPES system
- Experiment module G33/EV
- Digital multimeter

Basic theory:

CMOS Switches

MOSFETs are easily integrated into driver circuits on a single chip, and are therefore suitable for use as analog signal switches. The main disadvantage in switches featuring PMOS and NMOS transistors is there sensitivity to ON resistance at the analog signal voltage.
This problem can almost entirely eliminated by the use of CMOS switch consists of two parallel switches one featuring a channel-p MOSFET, the other with a channel-n MOSFET this parallel combination gives a relatively flat ON resistance/ analog signal voltage curve .

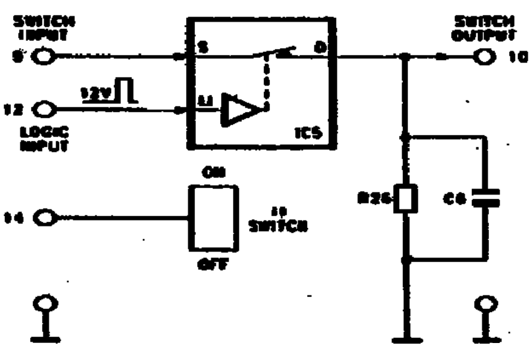


DESCRIPTION OF THE MODULE

ANALOG SWITCH

The section of the circuit denominated" ANALOG SWITCH" consists of the integrated analog switch ICs (DG 200 CJ).
The data sheet shows that this is a two-channel single-pole single-throw (SPST) analog switch which employs CMOS technology to ensure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in both directions with no offset voltage in the ON condition and block voltages up to 30 Vp-p in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With logic "0" at the input to the driver, the switch will be ON; logic "1" will turn the switch OFF. A voltage of between 0 and 0.8V is required for logic "0", while logic "1" is given by a voltage of between 2.4 and 15V. The input can therefore be directly interfaced with TTL, DTL, RTL and CMOS circuits.
The switch action is break-before-make, in order to prevent any shorting in the input signal. For the sake of convenience in the execution of the exercises, and as the switch is bidirectional, the two terminals of the analog switch are indicated on the trainer panel as SWITCH IN and SWITCH OUT. The driver logic input may be manual (ON/OFF operation via special switch) or external. This is selected by fitting a jumper between jack 12 and jack 14.

Figure F3.1



Procedure:

Measuring r_{DS} (ON) without current

Purpose of the exercise

The purpose of this exercise is to measure the drain-source resistance present in the analog switch without current.

Procedure

Connect the ±12V and ground jacks on the panel to a corrected power supply.

Connect jack 12 to jack 14.
Connect the digital multimeter (set to measure ohms) between jacks 9 and 10.
Set switch I_1 to ON; read the value of r_{DS} (ON) indicated on the digital multimeter.

Measuring r_{DS} (ON) with current

Purpose of the exercise

The purpose of this exercise is to measure the drain-source resistance present in the analog switch in the ON state as the current increases.

Procedure

Connect the ±12V and ground jacks on the panel to a corrected power supply.
Connect jacks 12 and 14.
Connect a variable 0 => + 12V DC power supply between jack 9 and ground.
Set switch I_1 to ON.
Increase the input voltage gradually until voltage can be measured at the terminals of R_{26}, as shown in column 1 of table 9.1. For each R_{26} voltage, measure the voltage between jacks 9 and 10 and list these voltages in column
Care should be taken to avoid exceeding 12V, as this might damage the unit.
Given R_{26} equivalent to 1.2KΩ.
Calculate the current circulating between drain and source.
From V_{DS} and I_{DS}, calculate the value of R_{DS} and list in column 4.
Plot the drain source current values (I_{DS} - mA) on the x-axis and the drain source resistance values (R_{DS} - Ω) on the y-axis.

Table 3.1.

S.N.	V_{R26}(volts)	$I_{DS(mA)}$	$V_{DS\ (mV)}$	$R_{DS\ (\Omega)}$
1				
2				
3				
4				
5				
6				

Outcome:

The R_{DS} (ON) without current comes out to be: ________________
The R_{DS} (ON) with current 2 mA comes out to be: ________________

Lab No.4

PURPOSE:

To illustrate the switching times and switching threshold of the analog switches.

EQUIPMENT REQUIRED:

- Base unit for the IPES system
- Experiment module G33/EV
- Digital multimeter
- Function generator
- Oscilloscope

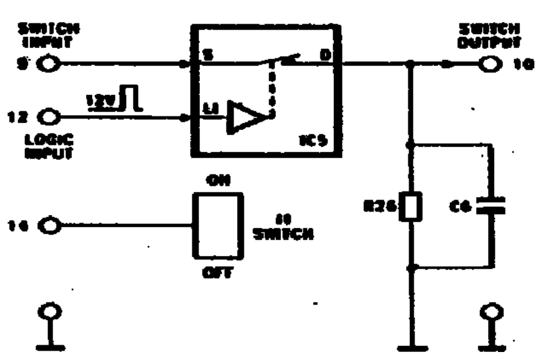
Basic theory:

One of the main specifications regarding the application of analog switches is the TURN ON TIME and the TURN OFF TIME. When a switch is commanded to change from ON to OFF, and vice-versa, a propagation delay occurs in the circuit driver. The T_{ON} and T_{OFF} times may be used to determine when a switch begins operation and whether multiple switches connected in a multiplexer configuration will be "make-before-break" or "break-before-make", i.e. whether the switches are triggered and then pause, or whether the pause precedes their action. The propagation delay should not be confused with the settling time, which is also effected by the load impedance. Two transitions will therefore apply:

OFF to ON $t_{settling} = t_{ON} + t_l \uparrow$ where $t_l \uparrow = f\,(R_{ON}, R_{LOAD}, C_D, C_{LOAD})$

ON to OFF $t_{settling} = t_{OFF} + t_l \downarrow$ where $t_l \downarrow. = f\,(R_{LOAD}, C_{LOAD}, C_D)$

Figure F4.1



Measurement of the switching time

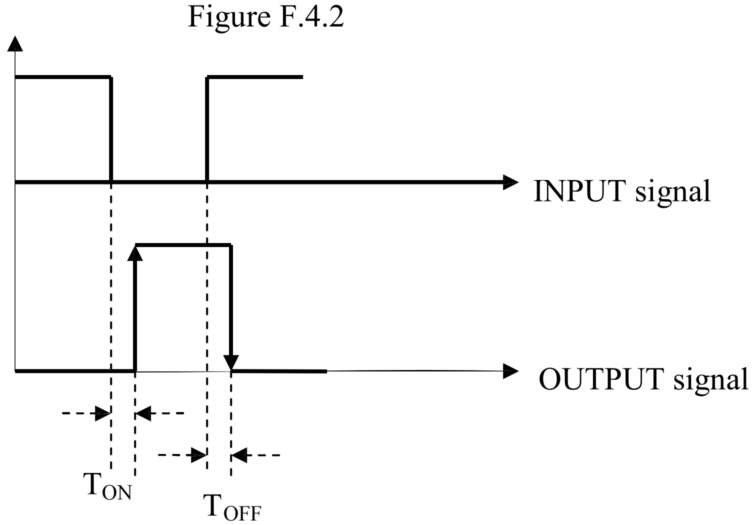
Purpose of the exercise

The purpose of this exercise is to determine the time required by the analog switch to open and close.

Procedure

Connect the ±12V and ground jacks on the panel to a corrected power supply.
Connect a + 10V DC power supply between jack 9 and ground.
Send a rectangular signal from the function generator between jack 12 and ground (amplitude 5V positive, frequency 50 KHz).
Connect one of the probes of the oscilloscope to the generator signal and the other to the output signal present between jack 10 and ground.
Measure the switching times between the output signal and the control signal; i.e. the rise time which corresponds to the closing of the analog switch and the fall time which corresponds to its opening.

Figure F.4.2



Measurement of the switching threshold

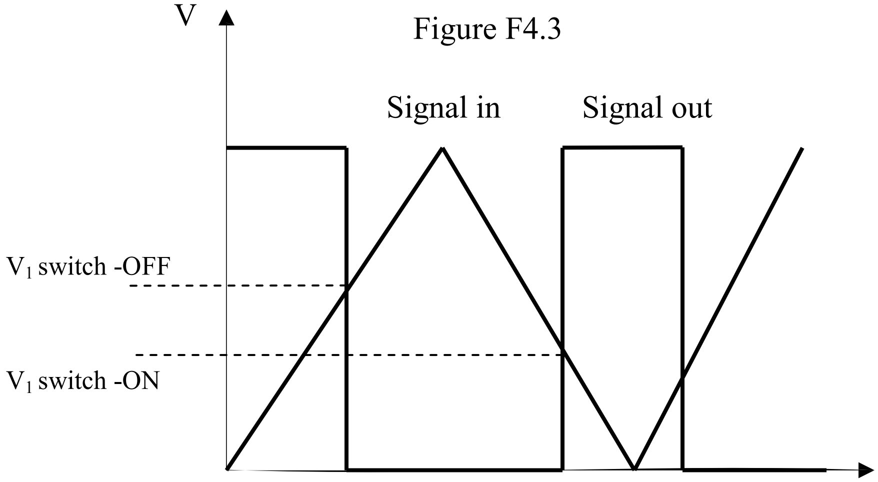
Purpose of the exercise

The purpose of this exercise is to measure the voltages at which the analog switch opens and closes.

Procedure

Connect the ±12V and ground jacks on the panel to a corrected power supply.
Connect a +5V DC power supply between jack 9 and ground.
Send a triangular signal from the function generator between the 12 jack and ground (amplitude 5V positive, frequency 1 KHz).
Connect one of the probes of the oscilloscope to the generator signal and the other to the output signal present between jack 10 and ground.
Measure the switching threshold by comparing the output signal with the control signal, i.e. the amplitude of the control signal at which the analog switch opens (V_1) and the amplitude at which it closes (V_2).

Figure 6.01 shows measurements carried out on a sample switch.



Outcome:

The t_{ON} (Turn ON time) of the analog switch comes out to be: _________________
The t_{OFF} (Turn OFF time) of the analog switch comes out to be: _________________
The voltages at which the analog switch opens comes out to be: _________________
The voltages at which the analog switch closes comes out to be: _________________

Lab No.5

PURPOSE:

To illustrate the operation and characteristics of the sample and hold circuit

EQUIPMENT REQUIRED:

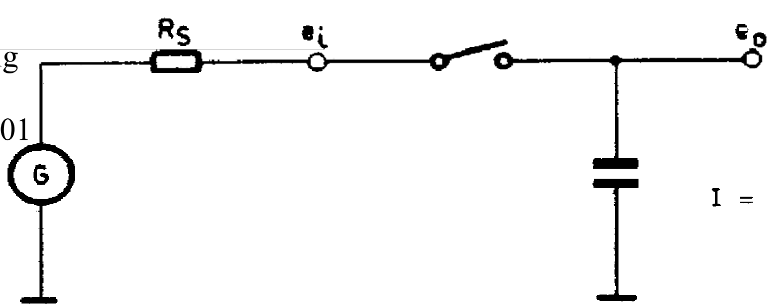
Base unit for the IPES system
Experiment module G33/EV
Function generator
Oscilloscope

Theory:

Introduction

The most simple sample and hold circuit consists of a switch and a capacitance. Two important specifications may be easily illustrated using the basic circuit. These are the aperture time and the acquisition time. The aperture time is the delay (reaction time) between the moment in which the control logic instructs the switch to open and the moment in which the aperture actually occurs. When extremely long aperture times (in the order of milliseconds) are tolerated, a relay may be used for the switch. For aperture times of less than 100 μs, FETs or BJTs are used as switches.
In variable-time systems, the input signal to the sample and hold circuit changes; the sample and hold circuit holds the last signal measured. The acquisition time is the time required by the sample and hold circuit to acquire the input signal value (within a predetermined degree of accuracy) when the control logic passes from hold to sample. Clearly, the most onerous condition is that in which the output must alter over its entire range (e.g. from + 10V to -10V and vice-versa).

Fig 5.01



$$I = C \frac{de_0}{dt} < I\ max$$

Module Description

Sample and hold device featuring operational amplifiers and analog switches

This circuit represents a non-inverting sample and hold with four operational amplifiers and four analog switches.

Operational amplifiers IC_8 and IC_{10}, together with analog switches IC_9a and IC_9c, make up the classic sample and hold circuit.

As the two analog switches must operate in opposing modes:

HOLD phase:	IC9a = closed	IC9c = open
SAMPLE phase:	IC9a = open	IC9c = close

And as there is only one command, switch IC9b is used to carry out an inversion.

Capacitor C_9 is the HOLD capacitor, and is also referred to as the "data storage capacitor".

Input amplifier IC_8, configured as non-inverting, has a high input resistance and features a potentiometer for calibration of the offset voltage.

Operational IC_{10} is of the FET type, and therefore has a very high input resistance (being connected in a non-inverting configuration). This means that the discharge of capacitor C_9 in the HOLD phase is minimal.

The circuit consisting of IC_{9d} and IC_{11} is added in order to minimize the errors introduced by analog switch IC_{9c} and operational amplifier IC_{10}. The errors introduced by these two parts of the circuit are identical (also considering that R_{42} corresponds approximately to the output resistance of operational amplifier IC_8) and are therefore cancelled when applied to the two differential inputs of amplifier IC_{12} It is important that capacitors IC_9 and IC_{10} are almost identical.

By connecting jack 17 to jack 19, the SAMPLE/HOLD status may be controlled via the SAMPLE/HOLD switch. If jack 17 is connected to jack 18, the SAMPLFJHOLD status is controlled by the signal from the GENERATOR. **Figure F 5.02**

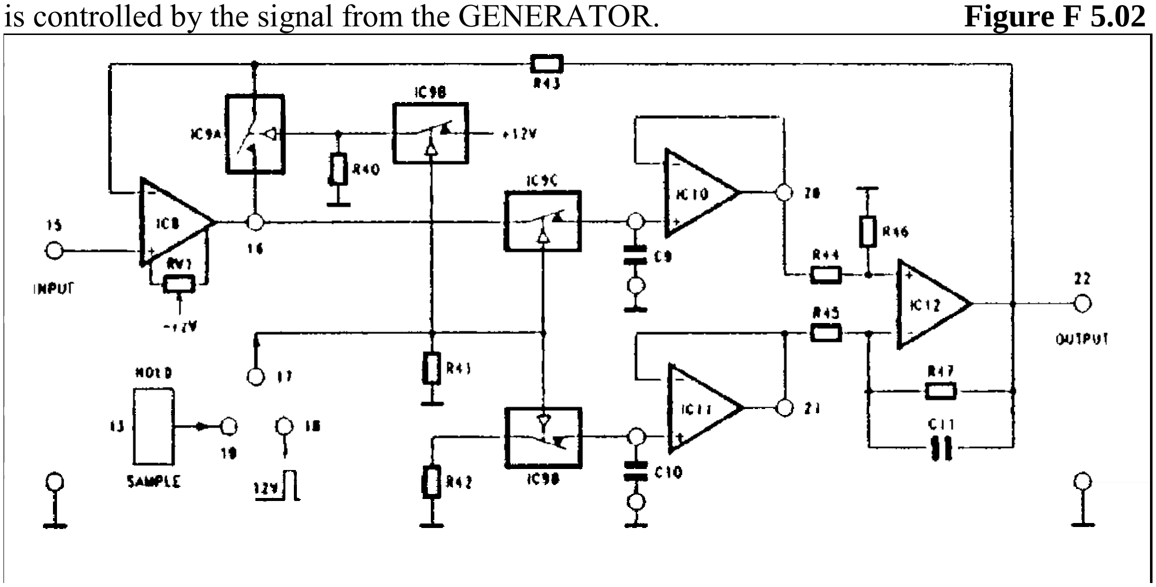
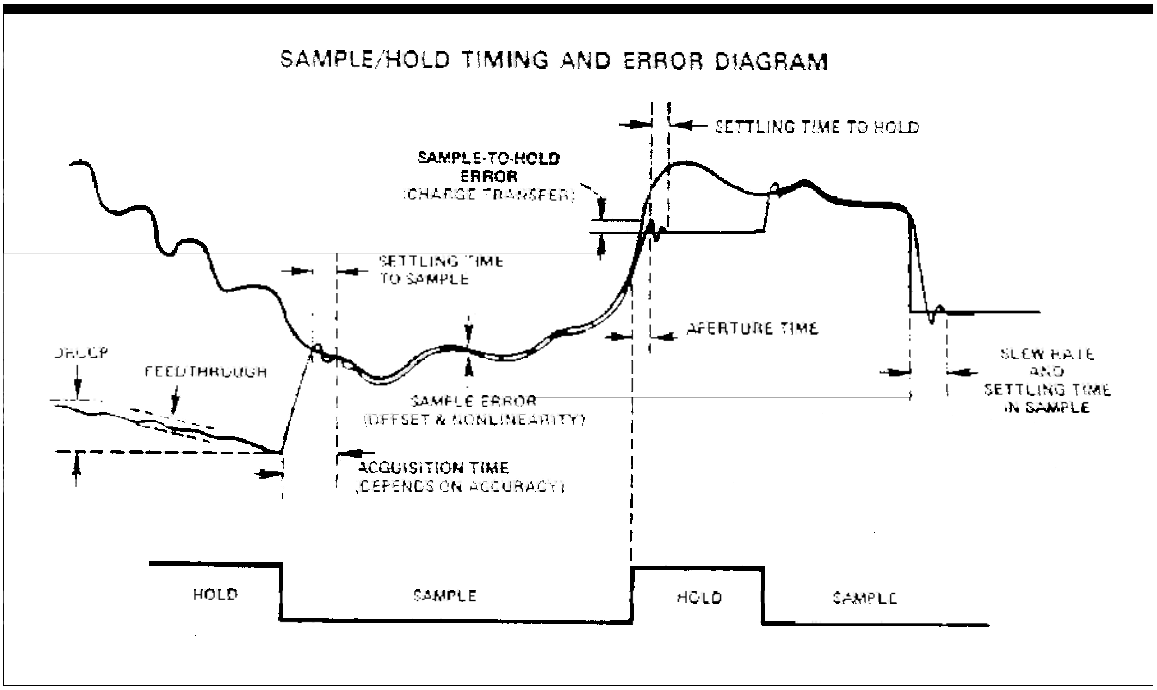


Figure F 5.03



<u>Procedure:</u>

Measuring the acquisition time

Purpose of the exercise

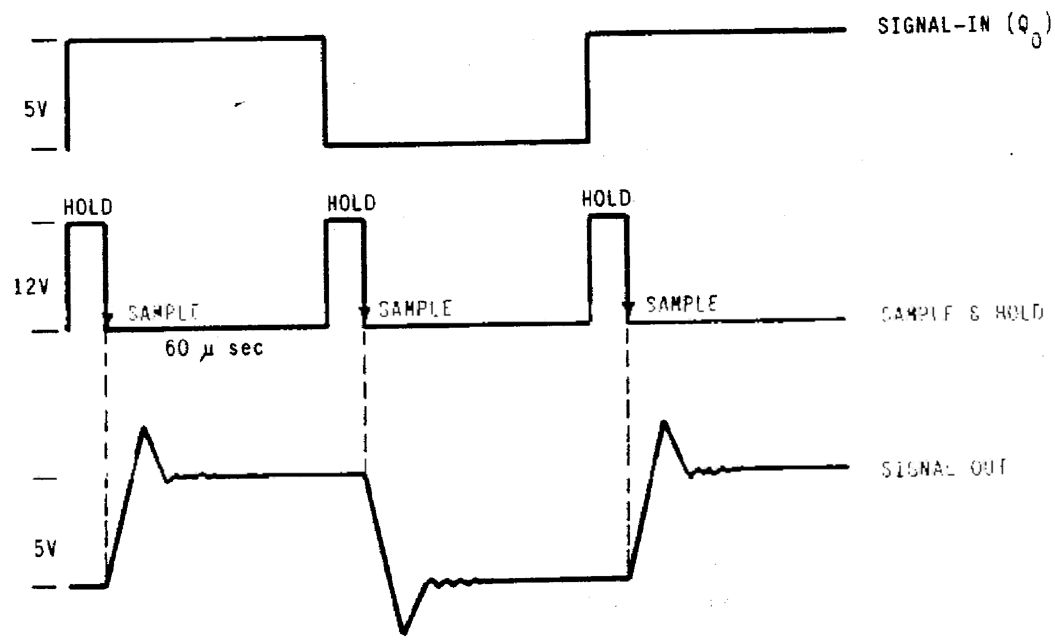
The purpose of this exercise is to measure the time required for transformation of the input signal into an output signal (starting from the beginning of the sampling phase).

Procedure

Connect the ±12V and ground jacks of the panel to a corrected power supply.
Connect jack 17 to jack 18.
Connect jack 7 to jack 5.
Set switch I_2 to 10 KHz.
Adjust the duty-cycle of the potentiometer so that the sample time is 60 µsec and the hold time 10 µsec (turn the knob completely counterclockwise).
Connect jack 3 to jack 15.
Connect one of the probes of the oscilloscope to the output signal between jack 22 and ground. The second probe should be connected first to the sample and hold signal and then to the input signal.
Fig. F5.4 shows the behavior in time of the three signals.

Note the existence of a delay (acquisition time) is approximately 10 to 15µsec between the "start sampling" command signal and the settling of the output signal.

Figure F5.4



Vary the duty cycle of controlling signal (connected to jack 17), and take observations.

Vary the duty cycle and take observations.

Connect the jack 15 and ground to function generator (sine wave of 5V positive with 5 KHz).

Vary the duty cycle of controlling signal (connected to jack 17).

Observe the acquisition times for different duty cycles of sample and hold signal.

Repeat the procedure with triangular wave input

Outcome:

The time required for transformation of the square wave input signal into an output signal comes out to be as follows:

Aperture Times:

Rise Time =
Fall Time =

Acquisition Times:

Rise Time =
Fall Time =

Lab No.6

PURPOSE:

General considerations on the Digital-to-Analog and Analog-to-Digital Conversion. And observation of its different parameters.

EQUIPMENT REQUIRED:

- Base unit for the IPES system
- Experiment module F03A
- Digital multimeter.

Basic theory:

An analog-to-digital (A/D) conversion means quantizing the amplitude of a physical quantity (e.g. a voltage) into a discrete levels class. Thus obtaining a series of digits, forming a number of a proper code. Generally the binary code and, consequently, binary numbers are used. Analog data can be obtained again through digital-to-analog (D/A) conversion.
Due to the quantization, each value V of the analog signal included within the interval V_i to V_{i+1} is always quantized at the same level $N_{i.}$
The interval: V_{i+1} to V_1 = Q, is defined as "quantum level".
Another important parameter of A/D converters is the conversion time since it defines the capacity of the converter to operate the conversion of a variable signal; in fact, remember that the sequence of the quantized levels must allow the regeneration of the original analog signal.
A time-variable signal can be converted into a discrete values class carrying out the sampling and holding operations. The sampling and holding operations are carried out through proper circuits called "Sample and Hold".

Resolution

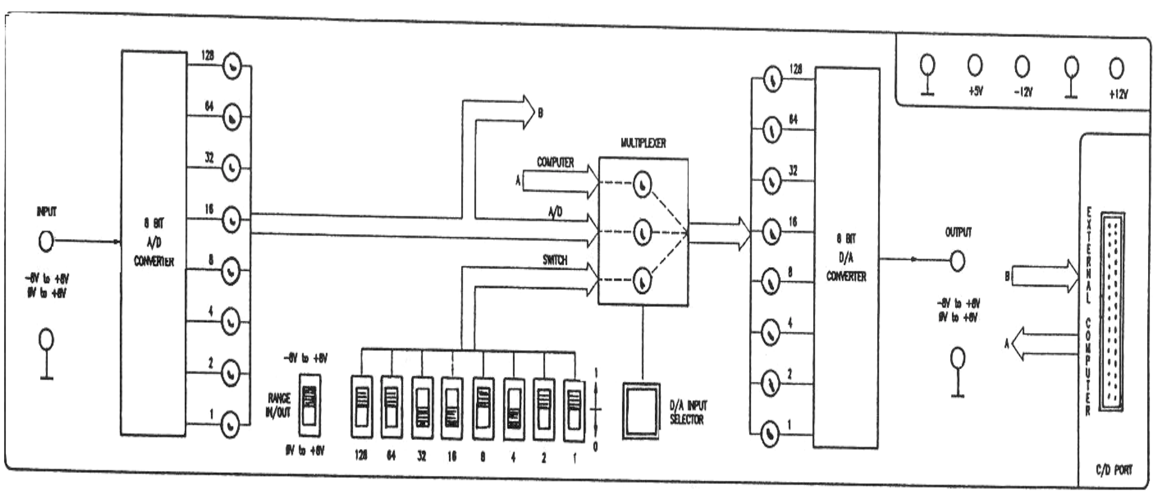
It defines the smallest standard incremental change in. the output voltage of a DAC or the amount of input voltage change required to increment the output of an
ADC between a code change and the next adjacent code change. A converter with "n" switches can divide the input in 2^n parts: the least significant increment is then 2^{-n}, or one least significant bit (LSB). On the contrary the Most Significant Bit carries a weight of 2-1. Resolution is applied to DACs and ADCs and may be expressed in percent of full scale or in binary bits.

Quantization error
The "ideal" quantization error obtained from the ideal characteristic of the A/D converter. It is the maximum deviation of a straight line of a perfect ADC, from a transfer function. As, by its very nature, an ADC quantizes the analog input into a finite number of output codes, only an infinite resolution would exhibit zero quantizing error. The quantizing error cannot strictly be applied to a DAC; in fact, the equivalent effect is more precisely a resolution error.

DESCRIPTION OF THE MODULE F03A

This module carries out an educational system of analog-to-digital and digital-to-analog conversion. This system consists of two 8-bit converters of large diffusion. A signal adapter is inserted before the A/D converter. This device permits the conversion of signals coming from conditioners with output range not coinciding with the converter output. The input range is chosen by acting on the IN/OUT selector and can be from 0 to +8V with the selector down and from -8 to +8V with the selector up. The input of the digital-to-analog converter can come from the analog-to-digital converter, from the computer or from a series of switches installed on the panel. The input connection is chosen through the pushbutton (D/A INPUT SELECTOR) and displayed on the LEDS of the multiplexer. The equipment must be power supplied with regulated D.C. voltages of +12,-12V and +5V.

Figure F6.01



A/D converter

The A/D converter (ADCO804LCN) operates with an input range included from 0V to +5 V, that is, an input voltage of 0 V generates a digital output signal consisting of a sequence of all 0s , whereas an input voltage of +5volts generates a digital signal of all 1s. Therefore the input signal must be adapted so that the minimum value of its range can generate an output signal of all 0 and the maximum value of the range generates a digital signal of all 1.

D/A Converter

The digital signal (8 bits) which must be sent to the input of the D/A converter (DACO800) can come from the A/D converter, from the computer or from a set of the 8 switches.

The operational amplifier IC_{1A} has a gain of 0.5 and carries out a shift range of the input signal if the range -8 to +8 is selected, the operational amplifier IC_{1B} makes the extreme range values coincide with 0v and 5v.

Range:

The range of module can be selected through *Range IN/OUT* switch. The range can be 0v to +8v, i.e.

OV = 00000000
+8V = 11111111

or -8v to +8v, i.e.

-8V = 00000000
+8V = 11111111

Procedure:

Set switch *Range IN/OUT* to 0V to 8V.

Resolution measurement:

- Connect the ±12V, +5V and ground jacks of the panel to a corrected power supply.
- Select *SWITCH* option through *D/A input selector*.
- Set the switches (S_{128} to S_1) to any position and note the analog voltage output through multimeter.
- Change the position of switch S_1 (LSB), and note the analog voltage output through multimeter.
- The change in voltages is equal to one resolution.

Binary codes for different voltage levels:

- Taking resolution as voltage required for LSB change, assign the binary codes to different voltage levels, starting as

  OV = 00000000
  +8V = 11111111
- Check the assigned values to the values, observed through LEDs output.

Quantization error:

- Apply some voltage to ADC input.
- Increase the input voltage to maximum value so that the output of ADC does not change.
- Apply maximum change in input voltage for which output shows same value as previous. The change is Quantization error, normally equal to half of the resolution.

Now set the switch *Range IN/OUT* to -8 V to +8 V, and repeat the procedure.

Observation:

Input Voltage	**Binary Code(0 V to +8 V)**	**Output voltage**
Input Voltage	**Binary Code(-8 V to +8 V)**	**Output voltage**

Outcome:

- The resolution of the ADC and DAC, for the switch *Range IN/OUT* position 0 V to 8 V, is….
- The quantization error of the ADC and DAC, for the switch *Range IN/OUT* position 0 V to 8 V, is….
- The resolution of the ADC and DAC, for the switch *Range IN/OUT* position -8 V to +8 V, is….
- The quantization error of the ADC and DAC, for the switch *Range IN/OUT* position -8 V to +8 V, is….

Lab No.7

PURPOSE:

Frequency analysis of the Digital-to-Analog and Analog-to-Digital Conversion, and observation of its different parameters:

EQUIPMENT REQUIRED:

- Base unit for the IPES system
- Experiment module F03A
- Digital multimeter.
- Function generator
- Oscilloscope

Basic theory:

A time-variable signal can be converted into a discrete values class carrying out the following operations:
Sampling operations: This is conversion of continuous time into discrete time, through which the instantaneous values of the analog signal are separated. The frequency of the sampling signal must guarantee the complete regeneration of the original signal. At this point, consider the sampling theorem stating that, if B is the bandwidth of the analog signal, the minimum sampling frequency must be equal to 2 B.
Therefore $F \geq 2B$
Sampling frequency: Analog signal is sampled at sampling frequency. The relation between analog and digital frequencies is:
Digital frequency = analog frequency / sampling frequency

$$f = F/Fs$$

Periodic sampling of continuous-time signal implies a mapping of the infinite frequency range for the variable F (or Ω) into a finite frequency range for the variable f (or ω). Since the highest frequency in a discrete time signal is $\omega = \pi$ or $f = ½$, it follows that, with a sampling rate F_s, the corresponding highest values of F and Ω are

$$Fmax = Fs/2 = 1/2T$$

$$\Omega max = \pi * Fs = \pi/T$$

Quantization operation: This is conversion of discrete time continuous valued into a discrete time discrete valued (digital) signal. it holds a constant value during the whole conversion time of the A/D converter. Actually the sampled value is held until the next sampling.
Coding: In the coding process, each discrete value is represented by a binary sequence.

Procedure:

- Connect the ±12V, +5V and ground jacks of the panel to a corrected power supply.
- Select *A/D* option through *D/A input selector*.
- Apply different voltage values to the analog input.
- Read the corresponding binary values on LEDs.
- Note the analog output values of the D/A converter corresponding to the different digital values and compare with the analog input value.

Response to a square, triangular, sine wave:

Set the selector of IN/OUT RANGE to "-8 to +8 V".

- Select *A/D* option through *D/A input selector*.
- Apply a sine wave with frequency of 1 kHz and amplitude not exceeding, ±8 V, to the input.
- Display the signal after the double conversion on oscilloscope.
- Compare its wave shape, amplitude, and phase shift with those of the input signal.
- Repeat the test with a triangular wave and with a square one.

Frequency response:

- Repeat the last test and increase the frequency of the input signal.
- Note the frequency up to which the signal reconstruction is correct.

Set the selector of IN/OUT RANGE to "0 to +8 V".
Check the response to a sine, triangular, and square wave, with different frequencies.

Outcome:

The maximum frequency of the sine wave input up to which output can be reconstructed comes out to be: ___________.
The most effected wave type by increasing frequency is: _________.
The least effected wave type by increasing frequency is: _________.

Lab No.8

PURPOSE:

Description of the module E18/EV and to illustrate the gate delay of a TTL Inverter:

EQUIPMENT REQUIRED:

- Base unit for the IPES system
- Experiment module E18/EV
- Digital multimeter
- Function generator
- Oscilloscope

Basic theory:

DESCRIPTION OF THE MODULE

The educational module E18 consists in a printed circuit on which digital logic circuits (TTL and CMOS) are mounted performing the following functions:

NO. of circuits	Name of circuit	IC
-6	Inverters	74LS04
-4	2- input AND ports	74LS08
-4	2-input NAND ports	74LSOO
-4	2- input OR ports	74LS32
-4	2-input NOR ports	74LS02
-4	2-input EX-OR ports	74LS86
-2	TTL-CMOS and CMOS-TTL interfaces	MM74C906
-4	J-K Flip-Flops	74LS76
-1	4-bit full Adder	74LS83
-1	4-bit Shift-register	74LS95
-1	Synchronous BCD counter	74LS160
-1	BCD decoder and display driver	74LS247
-1	7-segment display	HDSP5301
-1	Sync up/down counter	74LS192
-1	9-bit parity generator	74LS280
-1	Monostable	74LS221
-1	Multiplexer	74LS153
-1	Demultiplexer	74LS155
-1	BCD to decimal decoder	74LS42

-1	Encoder	74LS147
-1	Three state buffer	74LS125
-1	Latch	74LS75
-1	4-bit comparator	74LS85
-1	4-bit preselector	PICO-D-137-AK-1
-1	Clock generator (1 Hz, 10 kHz)	74LS14
-2	Push- buttons	4/6417
-8	Switches	4/7201
-10	LEDs	TIL210
-4	NAND ports with two CMOS inputs	CD4011
-2	20-pin terminals	

The components are mounted to carry out the experiments more quickly especially more complex circuits.
The connections between terminals of the devices are carried out by means of electrical cables and proper tubes present on the module and, electrically connected to the terminals of the integrated circuits. Each integrated circuit shows the silk screen printed logical diagram. The functions related to the IC are shown and terminals (In-Out) are indicated.

Implementation of the full-adder circuit, using the module E18/EV:

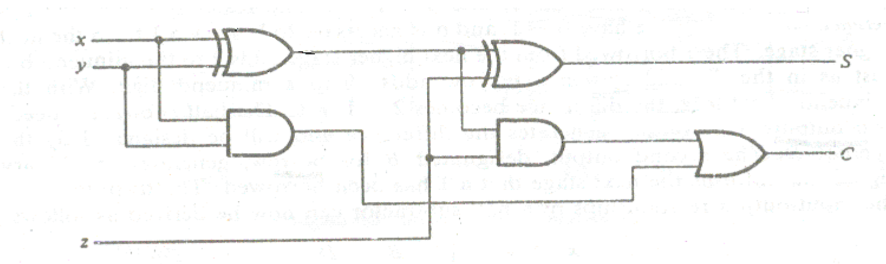
Full- Adder

A full-adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two of the input variables, denoted by *x* and *y*, represent two significant bits to be added. The third input *z*, represents the carry from the previous lower significant position. Two outputs are necessary because the arithmetic sum of three binary digits ranges in value from 0 to3 and binary 2or 3 needs two digits. The binary variable *S* indicates the sum and *C* the carry. The binary variable *S* gives the value if the least significant bit of the sum. The binary variable *C* gives the output carry.

Procedure:

- Connect the ±12V and ground jacks on the panel to a corrected power supply.
- Make connections as shown in fig.8.1.
- The connections between terminals of the devices should be carried out by electrical cables and proper tubes present on the module.
- Supply the required power (5V) to ICs AND OR and XOR.
- Connect the inputs *x, y, and z* to switches (SW_O to SW_7).
- Connect the output *C and S* to LEDs (LD_O to LD_9).
- Check different logics by changing switch position.

Fig.8.1



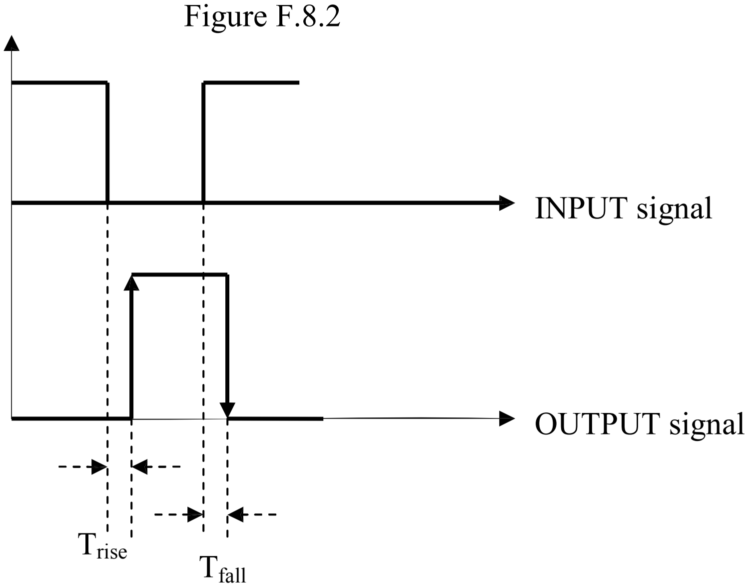
Measurement of gate delay of a TTL inverter:

Gate delay: Gate delay is the time taken by an IC to respond the change in input.

Procedure

Connect the +12V, +5V and ground jacks on the module to a corrected power supply.
Connect +5V and ground of the HEX INVERTER to a corrected power supply.
Send a rectangular signal from the function generator to input of HEX INVERTER (amplitude 5V positive, frequency 50 KHz).
Connect one of the probes of the oscilloscope to the generator signal and the other to the corresponding output signal of the HEX INVERTER.
Measure the gate delay between the output signal and the input signal.

Figure F.8.2



Outcome:

The gate delay of a TTL Inverter comes out to be: ________
The resulting truth table of the adder circuit is as follows:

x	*y*	*z*	*C*	*S*
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Lab No.9

PURPOSE:
To study the Basic Characteristics of Flip-Flops

EQUIPMENT REQUIRED:

- Base unit for the IPES system
- Experiment module E18/EV

Theory:

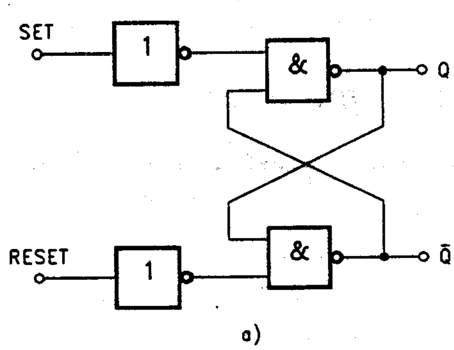
Introduction
The bistable multivibrator, commonly called flip- flops, are the most common form of digital memory elements. A memory element is generally a device which can store the logic state 0 or 1, called information "**bit**". The memory elements enable the storing of digital information for further uses. They permit to carry out complex sequential digital circuits, which took to the construction of modern calculators.

R-S Flip-flop (latch)

A main memory circuit can be carried out with the crossed coupling of two NAND ports: this kind of connection is called R-S flip- flop. Fig. 9.1 a) shows the diagram carried out with NAND ports, while fig.9.1 b) shows the symbol.
Similarly, to carry out the same flip- flop, it is also possible to use some NOR ports.

TRUTH TABLE OF THE
R-S FLIP FLOP
X= Last state
?= indefinite state

S	R	Q	Q`
0	0	X	X
0	1	0	1
1	0	1	0
1	1	?	?



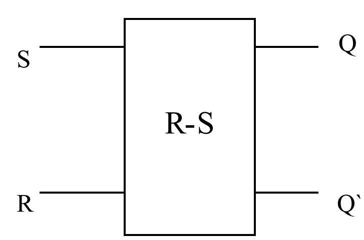


Fig. 9.1

Suppose a data is to be inserted in the flip-flop; the input levels are: SET = 1 and RESET = O. The output level of the port 1 is low (0) and this determines a high state across the output of port 3 (Q = 1). The output of port 2 is instead at 1, so port 4 finds two high levels (port 2 and 3) across its inputs, and takes its output to a low level (Q = 0).

The flip-flop is now on SET, with memorized information. Now, applying a high level across the RESET terminal, keeping the SET to a low level (s = 0 and R = 1), the flip- flop switches, i.e. it changes state, and the output becomes Q = 0 and Q = 1. In this case we say that the flip-flop is in RESET state. If the inputs SET and RESET are simultaneously applied to a high logic level (S = R = 1), you obtain an indeterminate state:

Q=Q`=1.

When the still state (R=S=O) is reset, the output having the lower transition time is taken high.

R-S Flip-flop with Clock

In sequential systems, the change of state in the flip-flops is often required to occur in synchronism with the clock pulse. This is carried out by modifying the diagram of fig.9.1 into the one of fig. 9.2.

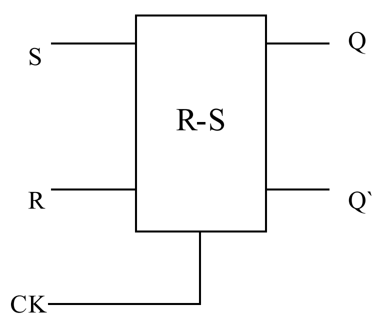
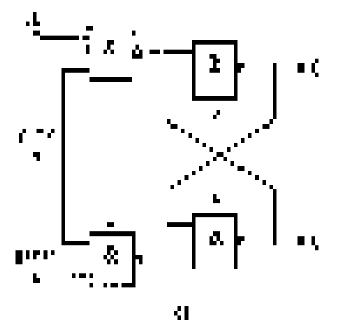


Fig. 9.2



While no input pulse is applied, the flip-flop keeps as it is, independently from the value of Rand S. Applying a clock pulse, if the inputs are R=S=O, the flip-flop keeps stable with the last output (Qn+1 = Qn). If instead we have: R = 0 and S = 1 the output of port 1 goes to 0 enabling the switching. In correspondence to a new clock pulse, if: R=1 and S=O, the latch changes state again and its outputs are: Q=O and Q=1.

In the case in which: R=S=1 on arrival of the clock pulse, the outputs of the flip-flops should both go to 1.

J-K flip-flop

The J-K flip-flop is formed by the R-S with clock, in which the outputs are taken back to the input, as in fig. 9.3

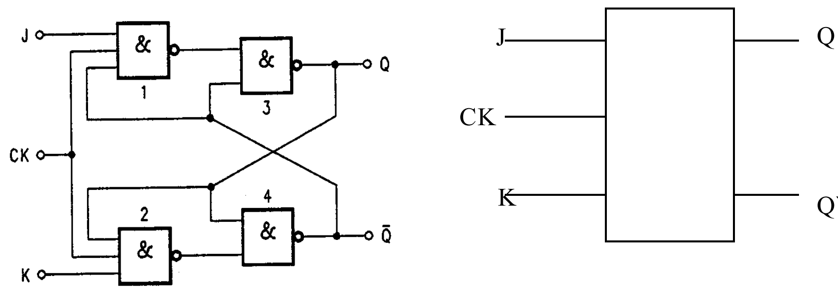


Fig. 9.3

Suppose that the flip-flop is in the state: Q = 0; Q' = 1. If the data input J is at the level 1 in correspondence to the clock pulse, the output of port 1 gets to 0, and the memory cell composed by ports 3-4 changes state: Q = 1 and Q' = 0
This flip-flop enables the removal of the uncertainty there was in the flip-flops R-S with clock, when the inputs were both at level 1. In fact, if:

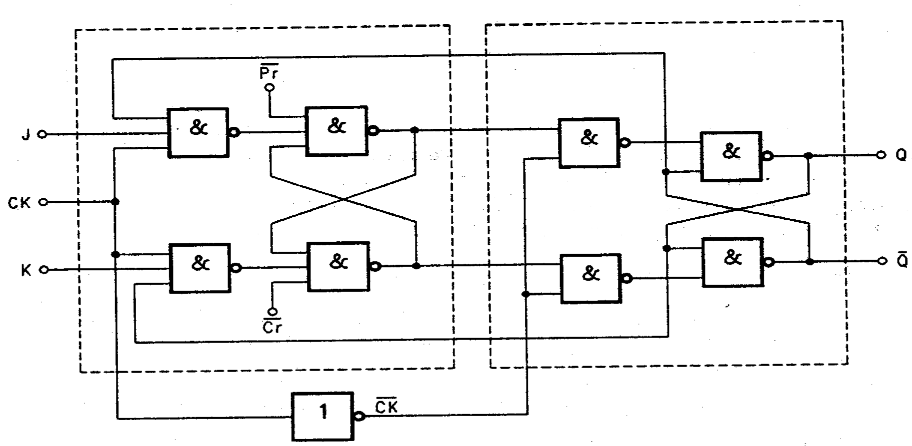
Q=1 Q'=O J=K=1

on arrival of the clock pulse, only port 2 enables the passage of the input data, while port 1 blocks them. The level 0 obtained across the output of port 2 makes the memory element switch (port 3 and 4). So, we have seen that when the inputs are both high there is no uncertainty, but the output state changes.

J-K Master-Slave Flip-flop
In the J-K flip-flops there can be possibility of uncertainty, if the clock pulse duration is too long in respect to the propagation times.
Considering that the flip-flop is in the following conditions:

Q=O Q'=1 J=K=1

When the clock pulse is applied, after the propagation time "t" of the ports, the output becomes: Q = 1 and Q' = 0
But being all the inputs signals still active, the outputs would tend to oscillate between 0 and 1, and at the end of the pulse, the state of the flip-flop is uncertain. To solve this inconvenience, the flip-flop type J-K Master-Slave has been introduced, which is commonly called J-K and can be seen in fig. 9.4.



It consists in a cascade connection of two R-S flip-flops, with reaction from the output of the second one, called SLAVE, to the input of the first, and called MASTER. Some pulses inverted in respect to the ones applied to the Master are applied across the input of the Slave. If the PRESET and CLEAR inputs are not active (Pr=Cr=1), on arrival of the clock pulse, the Master can change logic state according to the following truth table:

Pr = Cr = 1

t_n		t_{n+1}
J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n'

As, during the period in which the clock pulse is high, the Slave keeps blocked, the outputs Q and Q` are not changed. When the clock passes from 1 to 0, the Slave switches, and the Master blocks. In other words, the data present across J and K are transferred first to the Master, during the positive part of the clock pulse, and then to the Slave, during the negative part: in this way, the uncertainties across the outputs are removed.

D Flip-flop

If a J-K flip-flop is modified by adding an inverter (as shown in fig.9.5 a), so that the input K is complement of J, the set is known as flip-flop type D, in which D=DATA (fig.9.5 b). Its operation is simple: when a clock pulse arrives, the data present across the input is transferred and kept across the output.

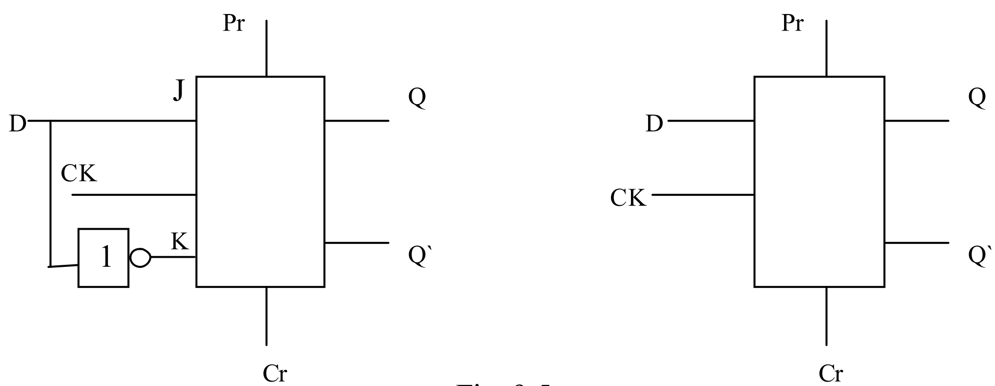


Fig. 9.5

T Flip-flop

If the inputs J and K are set always at logic level 1 on a flip-flop J-K, so this is a flip-flop commonly called type T (T means TOGGLE).It inverts the state of the outputs each time the input pulse applied to line T passes from the state 1 to the state O. Fig.9.6 shows the diagram (a) and the logic symbol (b) of a flip-flop type T.

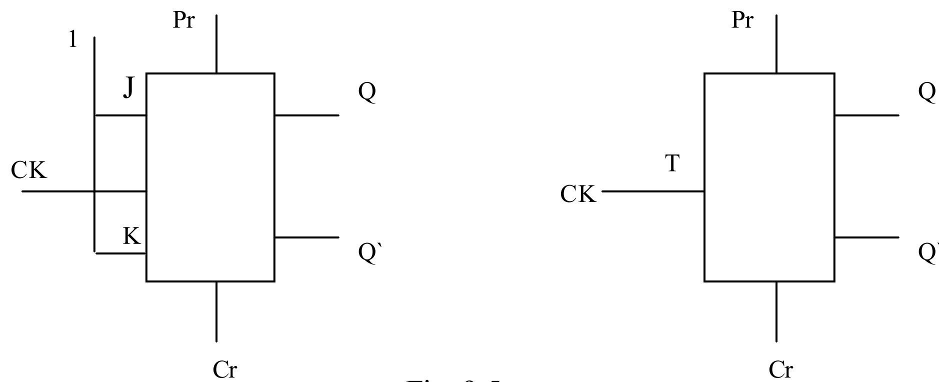


Fig. 9.5

Procedure:

Analysis of an R-S Flip-flop

Procedure

- Carry out a flip-flop type R-S using NAND and NOT ports, as in fig.9.1
- Connect the SET and RESET inputs to two switches.
- Connect the outputs Q and Q to two LEDs.
- Power the module.
- Turn the SET input, with the switch, to 1 and then to 0.
- Analyze the behavior of the outputs.
- Set the RESET line to 1, and then to 0.
- Analyze the behavior of the outputs again.
- Repeat some times the operations with the switches and check the carried out memorizations.
- Now, try to set both inputs to 1 and explain what the reason of the uncertain state is.

S	R	Q	Q`
0	0		
0	1		
1	0		
1	1		

Construction and Analysis of a J-K Flip-flop

Procedure

- Carry out the circuit of a J-K flip-flop as in fig. 9.3.
- Connect the inputs J and K to two switches, and the outputs to two LEDs.
- Connect the terminal of the clock at the bottom on the left to the input CK of the built up flip-flop, as well as to a led, to display the behavior.
- Power the module. ,
- Set the switches connected to the inputs alternatively high. :

- ✍ Analyze the behavior of the LEDs.
- ✍ Now, set both switches to the logic level 1, and explain the behavior of the flip-flop.

Comparison between J-K and J-K Master Slave Flip-flop

- ✍ Keep the circuit of the last exercise.
- ✍ Connect the switch of the input J also to J of an integrated flip-flop J-K (Master-Slave) present on the module.
- ✍ Carry out the same connection also for the inputs K and CK.
- ✍ Connect the outputs of the new flip-flops to other 2 LEDs.
- ✍ Power the module.
- ✍ Set the switches alternatively high and detect the differences between the two devices.
- ✍ Now, set both switches to 1 and analyze the behavior of the new flip-flop.

t_n		t_{n+1}
J	K	Q_{n+1}
0	0	
0	1	
1	0	
1	1	

Checking the Operation of a Flip-flop D

- ✍ Carry out the circuit of fig. 9.5 a) of a flip-flop type D by means of J-K flip-flops
- ✍ Connect the inputs P and R to 1.
- ✍ Check the operation of the flip-flop D by means of switches 0-1 of the input D and the Clock.

t_n	t_{n+1}
D	Q_{n+1}

Checking the Operation of a Flip-flop T

- ✍ Carry out the circuit of fig. 9.6 a) of a flip-flop type T by means of J-K flip-flop
- ✍ Connect the inputs P and R to 1.
- ✍ Check the operation of the flip-flop T by means of switches 0-1 to the Clock input.

t_n	t_{n+1}
T	Q_{n+1}

Lab No.10

PURPOSE:
To observe the propagation and transition times of CMOS and TTL gates:

EQUIPMENT REQUIRED:
- Module mod.E05a
- Power supply unit (+5 V and ±12 V)
- Dual trace oscilloscope
- Function generator

Theory:

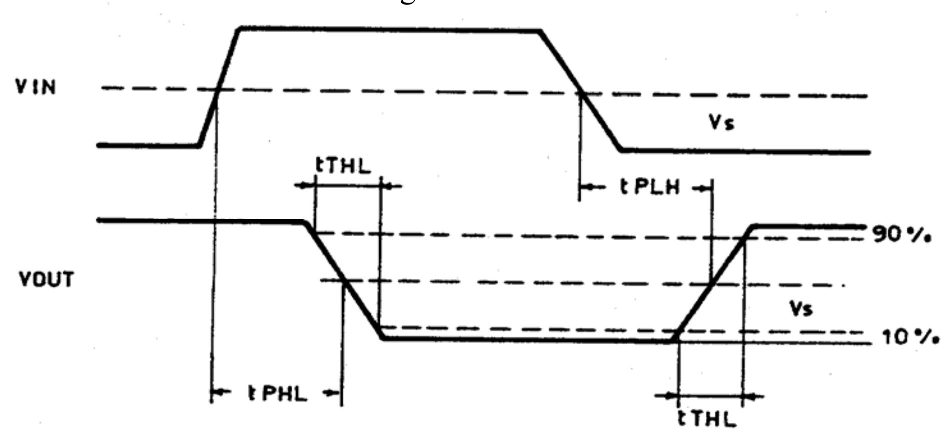
Introduction
Propagation delay times

The following values are normally specified by the manufacturers for any log1C gate:
a) **t** $_{\mathbf{PHL}}$: propagation delay time with output changing to the low level.
b) **t** $_{\mathbf{PLH}}$: propagation delay time with output changing to the high level.
The propagation delay times must be measured inside the fixed threshold values, which for the most part is the 50% of the whole signal variation.

Transition times

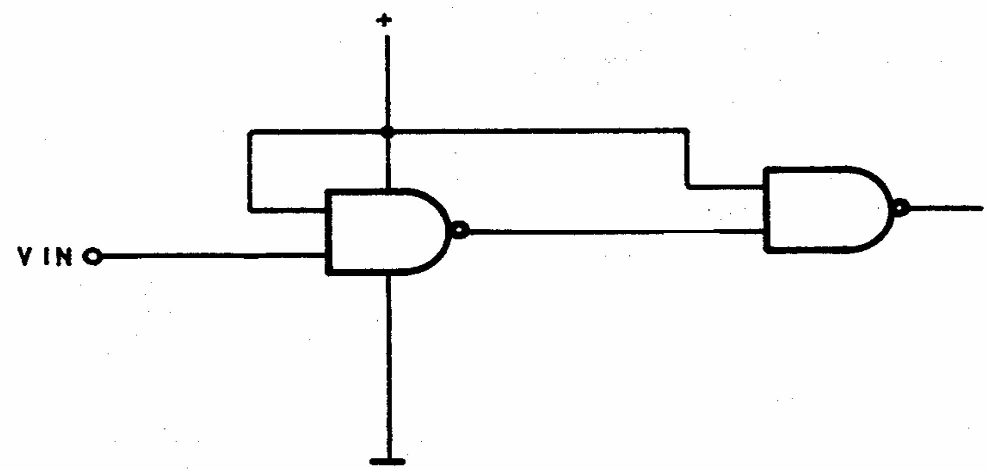
The following transition times are normally declared by the manufacturer:
a) **t** $_{\mathbf{THL}}$: transition time with output changing to the low level.
b) **t** $_{\mathbf{TLH}}$: transition time with output changing to the high level.
The time measurement is between the 10% and the 90% of the whole signal variation.
Fig. 10.1 shows the propagation delay time and the transition time of an inverting gate.

Figure 10.1



Procedure:

Figure 10.2



- ✍ Assemble the circuit of figure 10.2 with CMOS gates:
- ✍ Set the function generator for a 0-12V square wave and a frequency of 1 MHz.
- ✍ Connect the module to the power supply (+12V).
- ✍ Connect one of the CMOS gate input to the function generator output and the other one to the positive of the power supply input.

NOTE: Connect the input signal to the devices only when the function generator is ON, after the input signal has been correctly set and the device itself has been powered.

- ✍ Connect the gate output to the first input of the oscilloscope.
- ✍ Connect the output of the first gate to another CMOS gate input and to the second input of the oscilloscope.
- ✍ Superimpose the present signals and find the output signal delay time in respect to the input one, for 1 to 0 and 0 to 1 transitions.
- ✍ Measure the 0 to 1 and the 1 to 0 transition, times considering the voltages equal to 10% and 90% of the signal maximum;
- ✍ Repeat the procedure with TTL gate.
- ✍ Compare the speed of the devices, with other families.

Outcome:

- ✍ The **t** $_{PHL}$ of CMOS gates comes out to be: ___________
- ✍ The **t** $_{PLH}$ of CMOS gates comes out to be: ___________
- ✍ The **t** $_{THL}$ of CMOS gates comes out to be: ____________
- ✍ The **t** $_{TLH}$ of CMOS gates comes out to be: ____________
- ✍ The **t** $_{PHL}$ of TTL gates comes out to be: ____________
- ✍ The **t** $_{PLH}$ of TTL gates comes out to be: ____________
- ✍ The **t** $_{THL}$ of TTL gates comes out to be: ______________
- ✍ The **t** $_{TLH}$ of TTL gates comes out to be: ______________

<u>**LAB NO. 11**</u>

PURPOSE:

To implement

a) 2-bit counter circuit
b) Frequency divider circuit

Using JK-Flip-Flop

EQUIPMENT REQUIRED:

Base unit for IPES system

Experiment module E18/EV

Oscilloscope

THEORY:

Counters are digital integrated devices which can state in a well-defined sequence, applying a train pulse across the input.

They are carried out with flip-flop and logic port stages, where each stage supplies an output which, together with the others, indicate the number of pulses received in binary form.

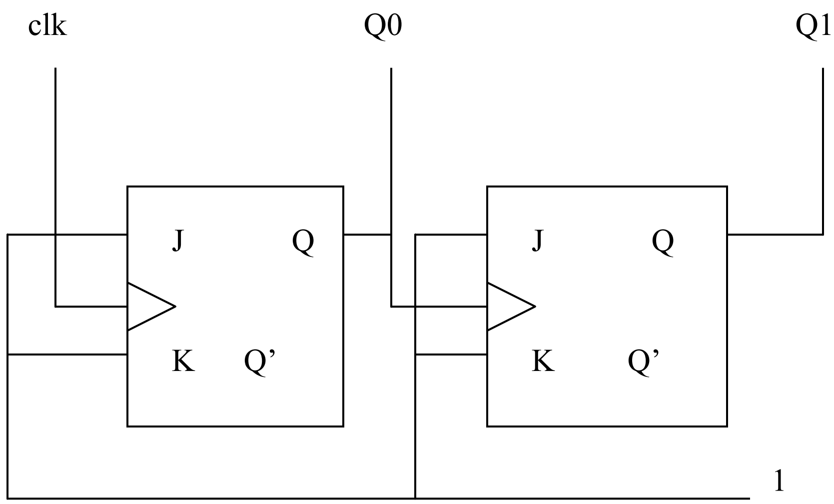
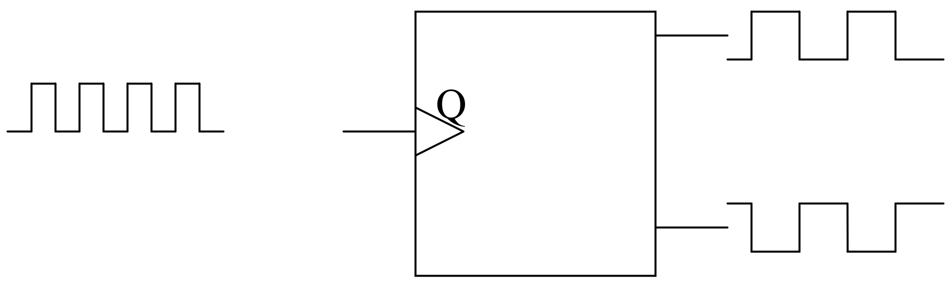


Fig-1

These counters are also called 'BINARY COUNTERS' and can be used apart as counters as frequency dividers, supplying the o/p with a pulse after 'n' input pulses.

If we apply a fixed frequency pulse train to a counter, rather than individual pulses coming at random intervals, we begin to notice some interesting characteristics and useful relationships between the input clock signal ad the output signal.



Consider a single flip flop with a continuous succession of clock pulses at a fixed frequency, such as the one shown above. We note three useful facts about the output signals seen at Q and Q' :

a) They are exactly inverted to each other
b) They are perfect square waves (50% duty cycle)
c) They have a frequency just half that of the clock pulse train

The duty cycle of any rectangular waveform refers to the percentage of the full cycle that the signal remains at logic 1. If the signal spends half its time at logic 1 and the other half at logic 0, we have a waveform with a 50% duty cycle. This describes a perfect, symmetrical square wave.

Frequency division by an odd number is also possible. The circuit shown below is a demonstration of a divide-by-3 counter. No gates are required to control the sequence if JK-flip flops are used; feeding the output signals back to the appropriate inputs is sufficient.

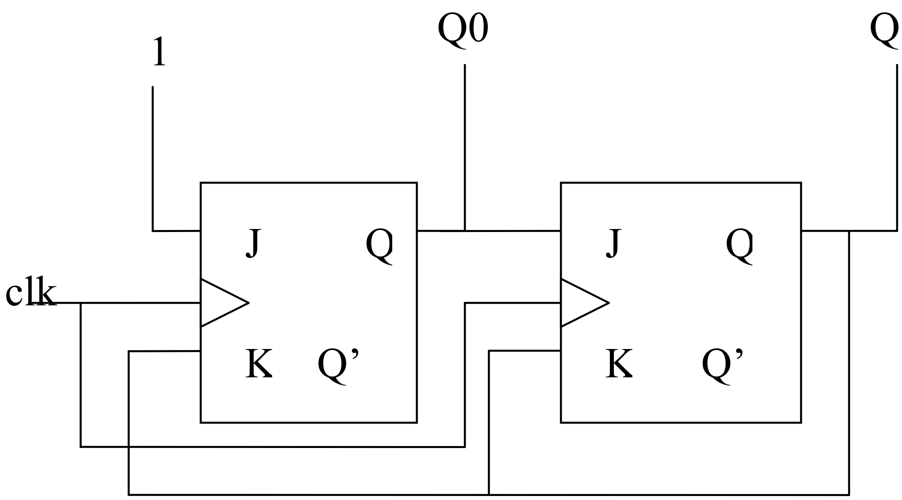


Fig-

Of course it is not possible to get a symmetrical (50% duty cycle) square wave with this circuit. Q0 is at logic 1 for two clock pulses out of three; Q1 is at logic 1 for one clock pulse out of 3. Thus duty cycle of 1/3 (33.33%) and 2/3 (66.67%) are available.

Other counting sequences are also possible. If a need exist to have two or more signals in a particular frequency relationship with each other, some extension or variation on the circuits shown can be designed to meet the need.

PROCEDURE:

a) ***2-bit Asynchronous Counter:***

- Carry out the circuit of Fig-1, a 2-stage asynchronous counter
- Connect all inputs, J and K to logic 1 (i.e +5V)
- Connect 1Hz clock to input CK of first flip-flop
- Connect Q0 to CK of second flip-flop
- Connect the two outputs, Q0 and Q1, to decoder/driver
- Connect the outputs of decoder/driver to respective inputs of display
- Power the module and analyze the operation of complete system

b) ***Frequency Divider***

- Carry out the circuit of Fig-2
- Connect the CK (clock) input of both flip-flops to external 1Hz clock
- Connect both the K input to Q1
- Connect Q0 to J input of second flip-flop
- Connect J-input of first flip-flop to logic 1 (+5V)
- Connect first channel of oscilloscope to clock input and second to Q0
- Now disconnect second channel and connect it to Q1
- Observe the frequencies of Q0 and Q1 with respect to input clock frequency

OUTCOME:

The output frequency at Q0 = ____________.____

The output frequency at Q1 = ____________.

LAB NO. 12

PURPOSE:

To implement a circuit complement number and then compare it with another number using a magnitude comparator and start a counter when certain condition true.

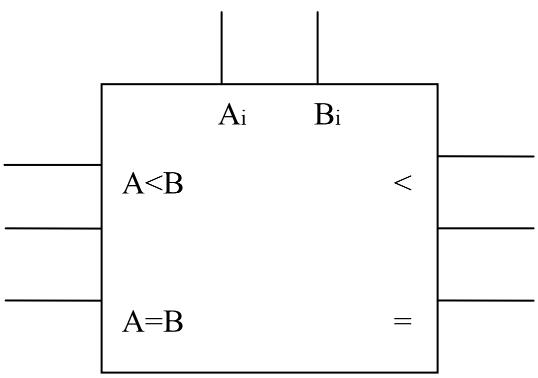
EQUIPMENT REQUIRED:

Base unit the IPES system

Experiment module E18/EV

THEORY:

A comparator compares two binary numbers and produces an output to show if the two numbers are equal, or if one is higher than other.



<	=	>	**Ai**	**Bi**	**A<B**	**A=B**	**A>B**
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	0	0	1
0	0	1	1	1	0	0	1
0	1	0	0	0	0	1	0
0	1	0	0	1	1	0	0
0	1	0	1	0	0	0	1
0	1	0	1	1	0	1	0
1	0	0	0	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	0	0	0	1
1	0	0	1	1	1	0	0

The counter used is a synchronous BCD counter, in a synchronous counter all flip-flop stages changes state contemporarily to the arrival of the clock pulse. A higher operating speed can be reached, so that they are more largely used in industrial applications.

We represent negative numbers by putting the symbol "-" in front of number. But a computer doesn't have it so easy. All it knows is bits, so we need to find some way to encode a negative number into a bit pattern so that the computer knows it's a negative value.

Several schemes have been used over the years:

1) Sign and magnitude
2) 1's complement
3) 2's complement

If we use binary comparator for numbers in sign magnitude, 1's or 2's complement representation, the result isn't correct. It is caused by sign bit, which is equal 1 for negative numbers but in binary numbers has the biggest weight. To obtain correct result the negative numbers should be complemented (in 1's and 2's complement representation), or both numbers should be tested like during addition (in sign magnitude representation).

Therefore, we have to find out the magnitude for 2's complemented 3-bit numbers in order to compare it with other binary number, to construct a circuit which will calculate the magnitude we have to find out the logic equation of the output using the following table(A,B,C are inputs and D,E are the outputs)

	A	**B**	**C**	**D**	**E**
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	1	0
3	0	1	1	1	1
-4	1	0	0	X	X
-3	1	0	1	1	1
-2	1	1	0	1	0
-1	1	1	1	0	1

For designing the logic circuit we are neglecting the -4 value.

The simplified logic equations for obtaining two bit magnitude are:

$D = A'B + A\,[B'C + BC']$

$E = C$

PROCEDURE:

- Implement the equations to generate two bit magnitude of the 3-bit 2's complemented number using the negative gates and switches.
- Connect the signal D and E to the A1 and A0 respectively of comparator's input.
- Connect the B1 and B0 input to the switches.
- Connect the comparators inputs A2, A3 B2, and B3 to ground.
- Connect the RES of counter to the A>B output of the comparator
- Connect the input "CK" of counter to clock of 1 Hz.
- Connect both the enablers EN to logic level high.
- Connect the outputs "QA" "QB" "QC" "QD" respectively to the LEDs.
- Observe the counter's output.

OUTCOME

National Semiconductor

November 1999

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder — similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

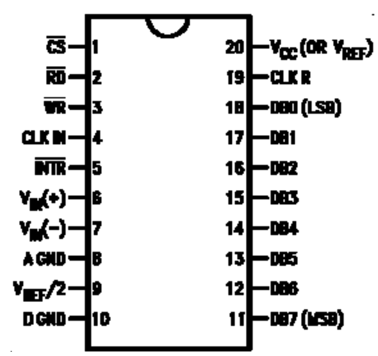
- Compatible with 8080 µP derivatives — no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates “stand alone”
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

- Resolution: 8 bits
- Total error: ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time: 100 µs

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages



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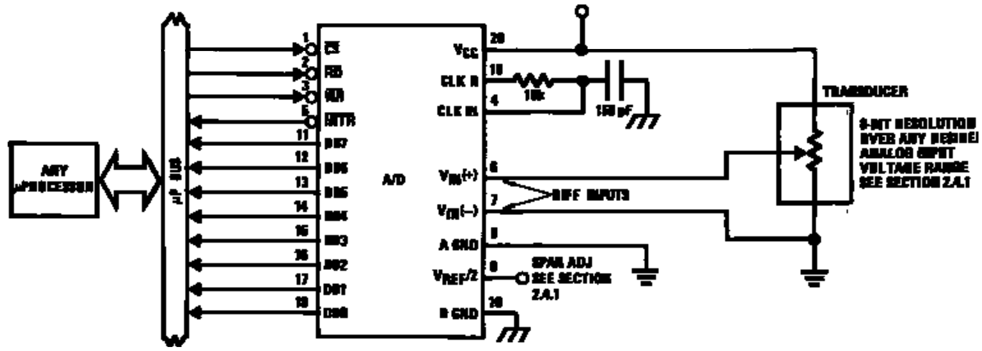
See Ordering Information

Ordering Information

TEMP RANGE		0˚C TO 70˚C	0˚C TO 70˚C	−40˚C TO +85˚C
ERROR	±¼ Bit Adjusted			ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM		ADC0802LCN
	±½ Bit Adjusted			ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCN	ADC0805LCN/ADC0804LCJ
PACKAGE OUTLINE		M20B — Small Outline	N20A — Molded DIP	

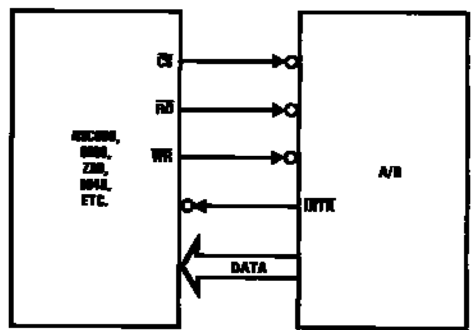
Z-80® is a registered trademark of Zilog Corp.

Typical Applications



DS005671-1

8080 Interface



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Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	**Full-Scale Adjusted**	**V_{REF}/2=2.500 V_{DC} (No Adjustments)**	**V_{REF}/2=No Connection (No Adjustments)**
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260˚C
Dual-In-Line Package (ceramic)	300˚C
Surface Mount Package	
Vapor Phase (60 seconds)	215˚C
Infrared (15 seconds)	220˚C
Storage Temperature Range	−65˚C to +150˚C
Package Dissipation at T_A=25˚C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN}≤T_A≤T_{MAX}$
ADC0804LCJ	−40˚C≤T_A≤+85˚C
ADC0801/02/03/05LCN	−40˚C≤T_A≤+85˚C
ADC0804LCN	0˚C≤T_A≤+70˚C
ADC0802/04LCWM	0˚C≤T_A≤+70˚C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC}, $T_{MIN}≤T_A≤T_{MAX}$ and f_{CLK}=640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	V_{REF}/2-No Connection			±1	LSB
V_{REF}/2 Input Resistance (Pin 9)	ADC0801/02/03/05	2.5	8.0		kΩ
	ADC0804 (Note 9)	0.75	1.1		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd–0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC} ±10% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN}≤T_A≤T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK}=640 kHz (Note 6)	103		114	µs
T_C	Conversion Time	(Notes 5, 6)	66		73	1/f_{CLK}
f_{CLK}	Clock Frequency	V_{CC}=5V, (Note 5)	100	640	1460	kHz
	Clock Duty Cycle		40		60	%
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ =0 V_{DC}, f_{CLK}=640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ =0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN}=5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN}=0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T−	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis (V_T+)−(V_T−)		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O=360 µA V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O=−360 µA V_{CC}=4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 I_{OUT}=1.6 mA, V_{CC}=4.75 V_{DC} I_{OUT}=1.0 mA, V_{CC}=4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−360 µA, V_{CC}=4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−10 µA, V_{CC}=4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT}=0 V_{DC} V_{OUT}=5 V_{DC}	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A=25˚C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A=25˚C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCWM	f_{CLK}=640 kHz, V_{REF}/2=NC, T_A=25˚C and $\overline{CS}$ =5V		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see Figure 4 and section 2.0.

AC Electrical Characteristics (Continued)

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

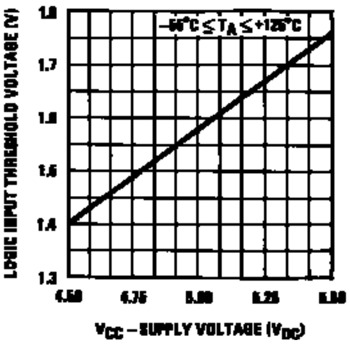
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and Figure 7.

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

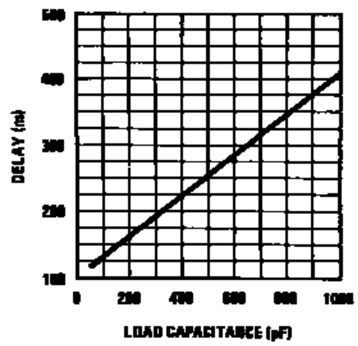
Typical Performance Characteristics

Logic Input Threshold Voltage vs. Supply Voltage



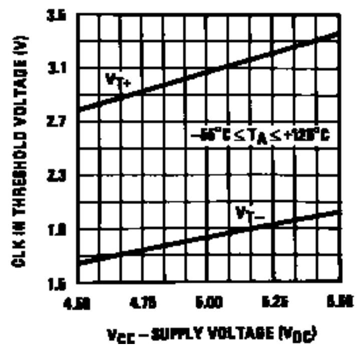
DS005671-38

Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance



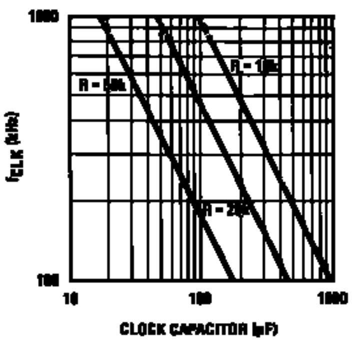
DS005671-39

CLK IN Schmitt Trip Levels vs. Supply Voltage



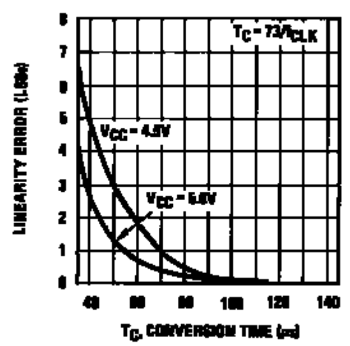
DS005671-40

f_{CLK} vs. Clock Capacitor



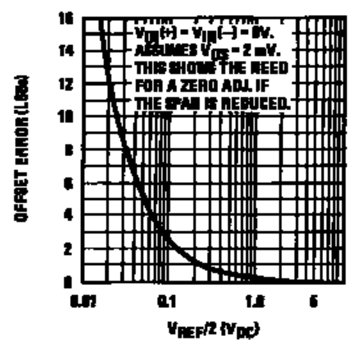
DS005671-41

Full-Scale Error vs Conversion Time



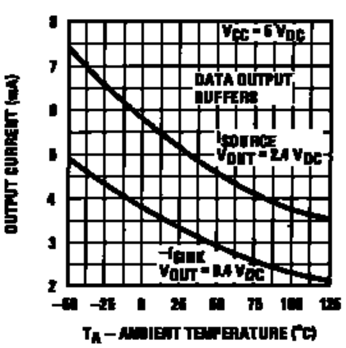
DS005671-42

Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



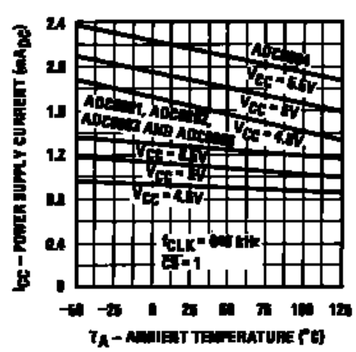
DS005671-43

Output Current vs Temperature



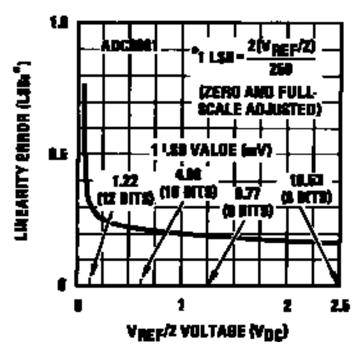
DS005671-44

Power Supply Current vs Temperature (Note 9)



DS005671-45

Linearity Error at Low $V_{REF}/2$ Voltages



DS005671-46

National Semiconductor

June 1999

DAC0800/DAC0802
8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in Figure 1. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

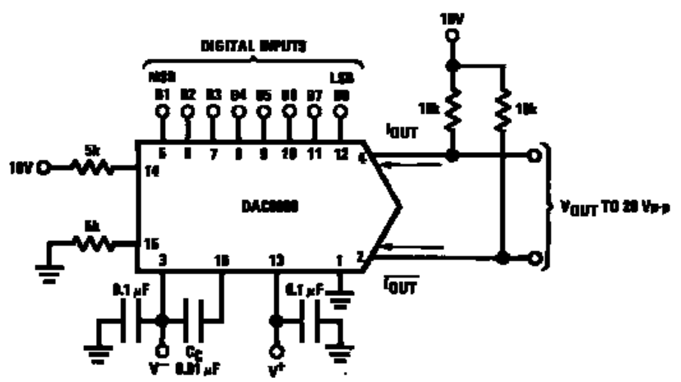
The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC}, grounded. Changing the V_{LC} potential will allow direct interface to other logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33 mW with ±5V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, and DAC-08H, respectively.

Features

- Fast settling output current: 100 ns
- Full scale error: ±1 LSB
- Nonlinearity over temperature: ±0.1%
- Full scale current drift: ±10 ppm/˚C
- High output compliance: −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range: ±4.5V to ±18V
- Low power consumption: 33 mW at ±5V
- Low cost

Typical Applications



DS005686-1

FIGURE 1. ±20 V_{P-P} Output Digital-to-Analog Converter (Note 5)

Ordering Information

Non-Linearity	Temperature Range	Order Numbers				
		J Package (J16A) (Note 1)		**N Package (N16E)** (Note 1)		**SO Package (M16A)**
~~±0.1% FS~~	~~$0˚C \le T_A \le +70˚C$~~	~~DAC0802LCJ~~	~~DAC-08HQ~~	~~DAC0802LCN~~	~~DAC-08HP~~	~~DAC0802LCM~~
±0.19% FS	$-55˚C \le T_A \le +125˚C$	DAC0800LJ	DAC-08Q			
±0.19% FS	$0˚C \le T_A \le +70˚C$	DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP	DAC0800LCM

Note 1: Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	±18V or 36V
Power Dissipation (Note 3)	500 mW
Reference Input Differential Voltage (V14 to V15)	V^- to V^+
Reference Input Common-Mode Range (V14, V15)	V^- to V^+
Reference Input Current	5 mA
Logic Inputs	V^- to V^- plus 36V
Analog Current Outputs ($V_S- = -15V$)	4.25 mA
ESD Susceptibility (Note 4)	TBD V
Storage Temperature	−65˚C to +150˚C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260˚C
Dual-In-Line Package (ceramic)	300˚C
Surface Mount Package	
Vapor Phase (60 seconds)	215˚C
Infrared (15 seconds)	220˚C

Operating Conditions (Note 2)

	Min	Max	Units
Temperature (T_A)			
DAC0800L	−55	+125	˚C
DAC0800LC	0	+70	˚C
DAC0802LC	0	+70	˚C

Electrical Characteristics

The following specifications apply for $V_S = \pm15V$, $I_{REF} = 2$ mA and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Nonlinearity				±0.1			±0.19	%FS
t_s	Settling Time	To ±½ LSB, All Bits Switched "ON" or "OFF", T_A=25˚C		100	135				ns
		DAC0800L					100	135	ns
		DAC0800LC					100	150	ns
tPLH, tPHL	Propagation Delay	T_A=25˚C							
	Each Bit			35	60		35	60	ns
	All Bits Switched			35	60		35	60	ns
TCI_{FS}	Full Scale Tempco			±10	±50		±10	±50	ppm/˚C
V_{OC}	Output Voltage Compliance	Full Scale Current Change <½ LSB, R_{OUT}>20 MΩ Typ	−10		18	−10		18	V
I_{FS4}	Full Scale Current	V_{REF}=10.000V, R14=5.000 kΩ R15=5.000 kΩ, T_A=25˚C	1.984	1.992	2.000	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4}-I_{FS2}$		±0.5	±4.0		±1	±8.0	μA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0	μA
I_{FSR}	Output Current Range	V^-=−5V	0	2.0	2.1	0	2.0	2.1	mA
		V^-=−8V to −18V	0	2.0	4.2	0	2.0	4.2	mA
	Logic Input Levels								
V_{IL}	Logic "0"	V_{LC}=0V			0.8			0.8	V
V_{IH}	Logic "1"		2.0			2.0			V
	Logic Input Current	V_{LC}=0V							
I_{IL}	Logic "0"	$-10V \le V_{IN} \le +0.8V$		−2.0	−10		−2.0	−10	μA
I_{IH}	Logic "1"	$2V \le V_{IN} \le +18V$		0.002	10		0.002	10	μA
V_{IS}	Logic Input Swing	V^-=−15V	−10		18	−10		18	V
V_{THR}	Logic Threshold Range	V_S=±15V	−10		13.5	−10		13.5	V
I_{15}	Reference Bias Current			−1.0	−3.0		−1.0	−3.0	μA
dI/dt	Reference Input Slew Rate	(Figure 11)	4.0	8.0		4.0	8.0		mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	$4.5V \le V^+ \le 18V$		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS-}$		$-4.5V \le V^- \le 18V$		0.0001	0.01		0.0001	0.01	%/%
		I_{REF}=1mA							

Electrical Characteristics (Continued)

The following specifications apply for V_S = ±15V, I_{REF} = 2 mA and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
	Power Supply Current	V_S=±5V, I_{REF}=1 mA							
I+				2.3	3.8		2.3	3.8	mA
I−				−4.3	−5.8		−4.3	−5.8	mA
		V_S=5V, −15V, I_{REF}=2 mA							
I+				2.4	3.8		2.4	3.8	mA
I−				−6.4	−7.8		−6.4	−7.8	mA
		V_S=±15V, I_{REF}=2 mA							
I+				2.5	3.8		2.5	3.8	mA
I−				−6.5	−7.8		−6.5	−7.8	mA
P_D	Power Dissipation	±5V, I_{REF}=1 mA		33	48		33	48	mW
		5V,−15V, I_{REF}=2 mA		108	136		108	136	mW
		±15V, I_{REF}=2 mA		135	174		135	174	mW

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

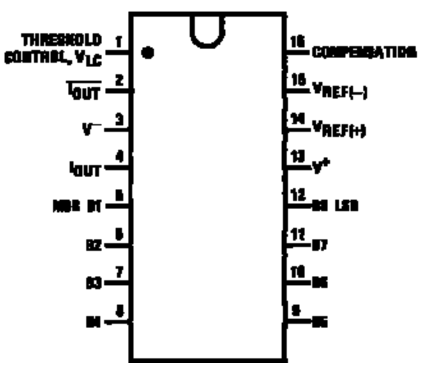
Note 3: The maximum junction temperature of the DAC0800 and DAC0802 is 125˚C. For operating at elevated temperatures, devices in the Dual-In-Line J package must be derated based on a thermal resistance of 100˚C/W, junction-to-ambient, 175˚C/W for the molded Dual-In-Line N package and 100˚C/W for the Small Outline M package.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Pin-out numbers for the DAC080X represent the Dual-In-Line package. The Small Outline package pin-out differs from the Dual-In-Line package.

Connection Diagrams

Dual-In-Line Package



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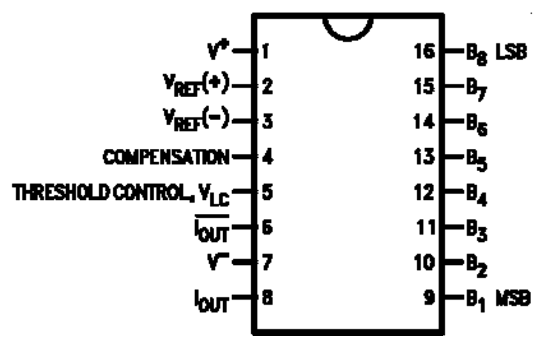
Top View

Small Outline Package

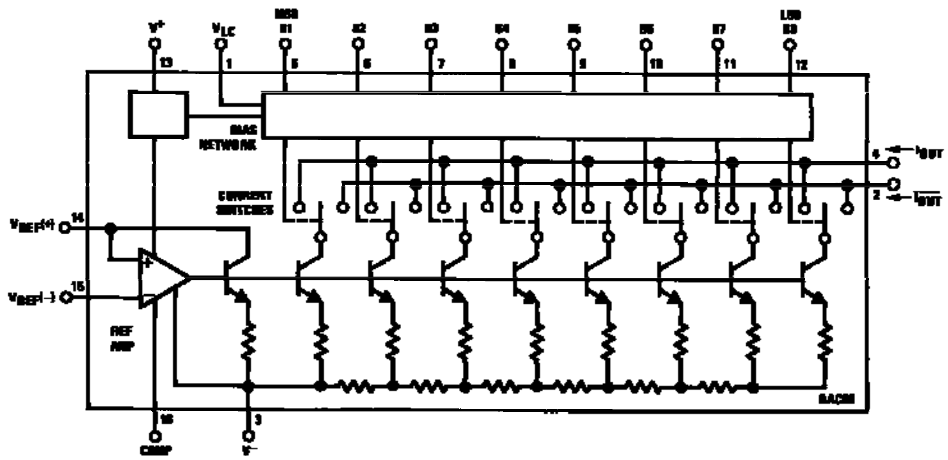


DS005686-14

Top View

See Ordering Information

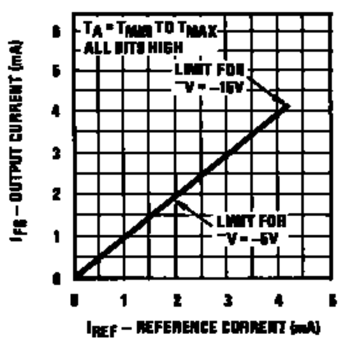
Block Diagram (Note 5)



DS005686-2

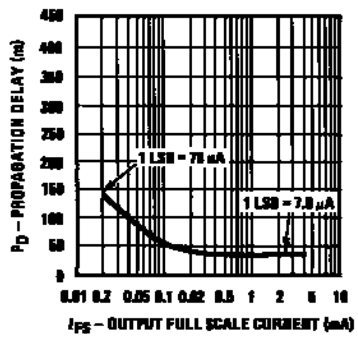
Typical Performance Characteristics

Full Scale Current vs Reference Current



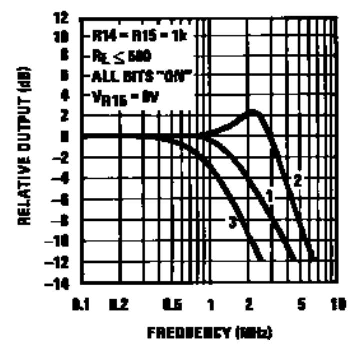
DS005686-22

LSB Propagation Delay vs I_{FS}



DS005686-23

Reference Input Frequency Response



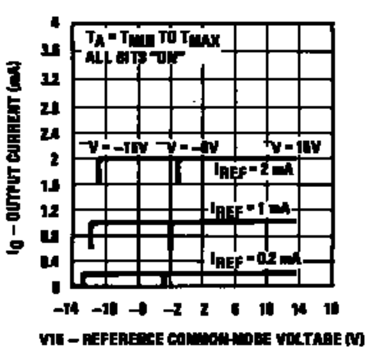
DS005686-24

Curve 1: C_C=15 pF, V_{IN}=2 Vp-p centered at 1V.

Curve 2: C_C=15 pF, V_{IN}=50 mVp-p centered at 200 mV.

Curve 3: C_C=0 pF, V_{IN}=100 mVp-p centered at 0V and applied through 50Ω connected to pin 14.2V applied to R14.

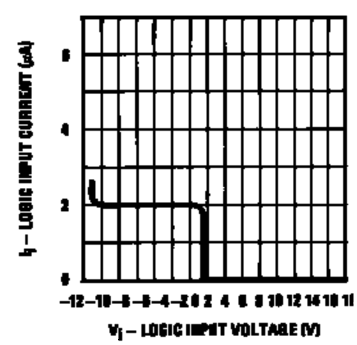
Reference Amp Common-Mode Range



DS005686-25

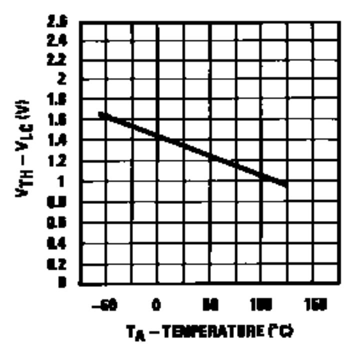
Note. Positive common-mode range is always (V+) − 1.5V.

Logic Input Current vs Input Voltage



DS005686-26

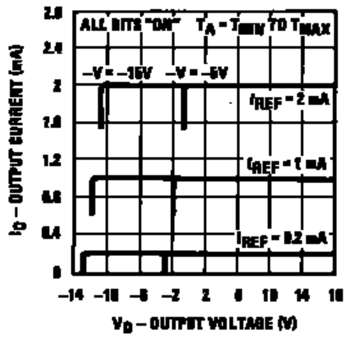
V_{TH} — V_{LC} vs Temperature



DS005686-27

Typical Performance Characteristics (Continued)

Output Current vs Output Voltage (Output Voltage Compliance)



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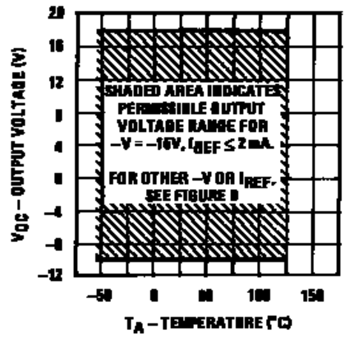
Output Voltage Compliance vs Temperature



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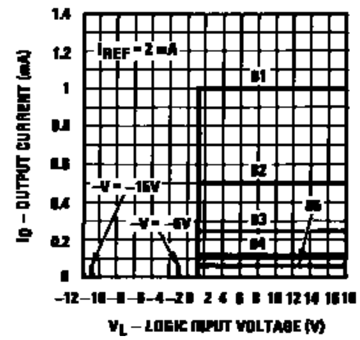
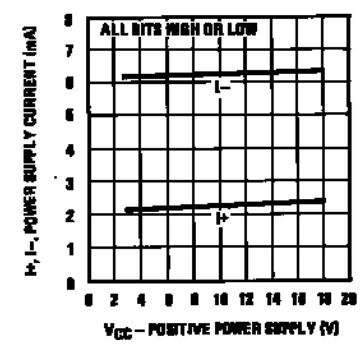
Bit Transfer Characteristics



DS005686-30

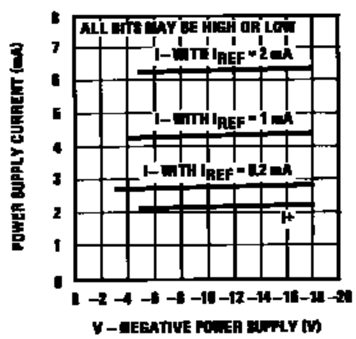
Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than ½ LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range (V_{LC} = 0V).

Power Supply Current vs +V



DS005686-31

Power Supply Current vs −V



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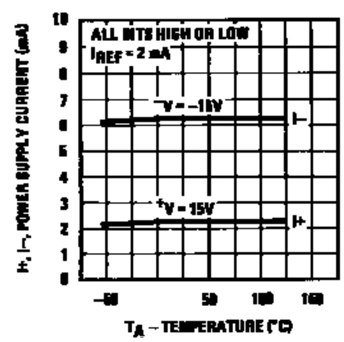
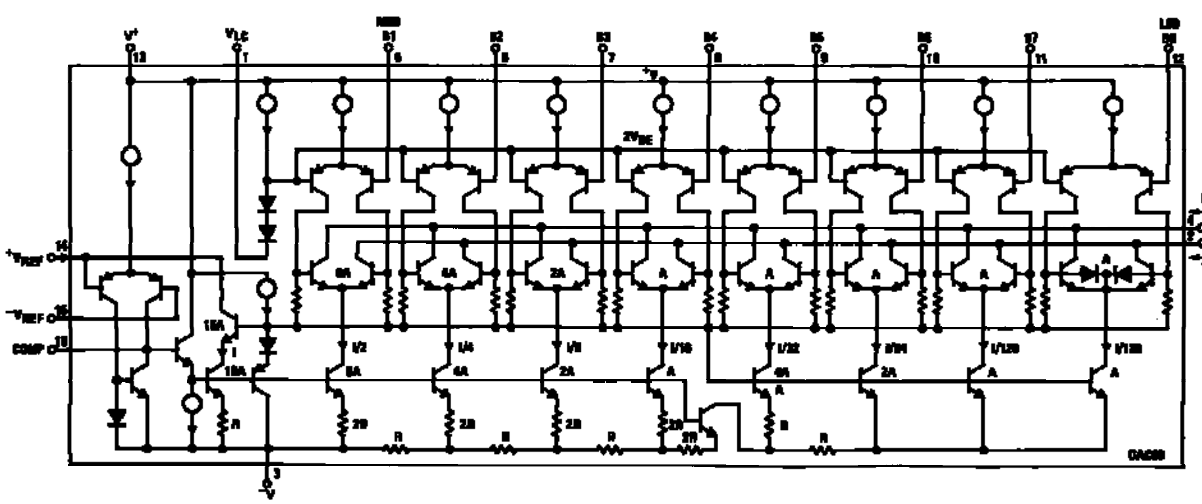
Power Supply Current vs Temperature



DS005686-33

Equivalent Circuit



DS005686-15

FIGURE 2.

19-0484; Rev 1; 5/96

MAXIM

Dual Monolithic SPST CMOS Analog Switch

DG200A

General Description

The DG200A is a dual, normally closed, single-pole-single-throw (SPST) analog switch. This CMOS switch can be operated with power supplies ranging from ±4.5V to ±18V. The DG200A has guaranteed break-before-make switching. Its maximum turn-off time is 500ns, and its maximum turn-on time is 100ns.

Maxim guarantees that the DG200A will not latch-up if the power supplies are turned off with input signals still connected as long as absolute maximum ratings are not violated.

Compared to the original manufacturer's product, Maxim's DG200A consumes significantly lower power, making it better suited for portable applications.

Applications

Winchester Disk Drives

Test Equipment

Communications Systems

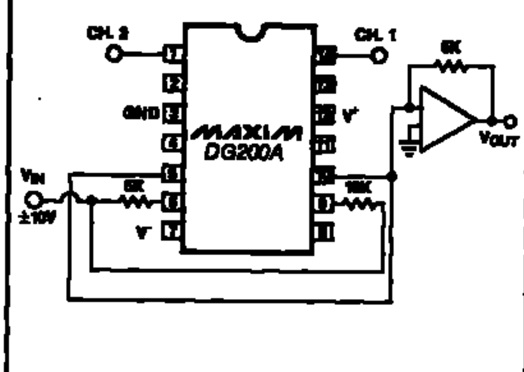
PBX, PABX

Guidance and Control Systems

Head up Displays

Military Radios

Typical Operating Circuit



Programmable Gain Amplifier

Features

- ◆ Improved 2nd Source! Power Supply Current <300µA
- ◆ Wide Supply Range ±4.5V to ±18V
- ◆ Single Supply Operation
- ◆ Non-Latching with Supplies Turned-off and Input Signals Present
- ◆ CMOS and TTL Logic Compatible
- ◆ Monolithic, Low Power CMOS Design

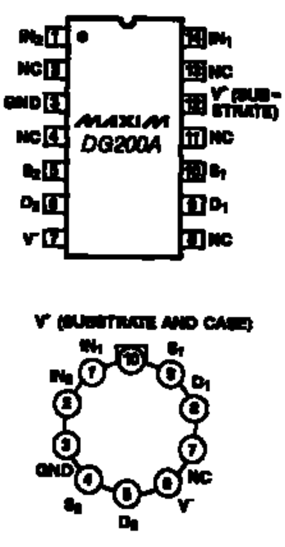
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
DG200AAK	-55°C to +125°C	14 Lead CERDIP
DG200ABK	-25°C to +85°C	14 Lead CERDIP*
DG200ACK	0°C to +70°C	14 Lead CERDIP
DG200ACJ	0°C to +70°C	14 Lead Plastic DIP
DG200ADJ	-40°C to +85°C	14 Lead Plastic DIP
DG200ACY	0°C to +70°C	14 Lead SO
DG200ADY	-40°C to +85°C	14 Lead SO
DG200AC/D	0°C to +70°C	Dice
DG200AAA	-55°C to +125°C	10 Pin Metal Can*
DG200ABA	-25°C to +85°C	10 Pin Metal Can*
DG200ACA	0°C to +70°C	10 Pin Metal Can*

*Contact factory for availability.

Pin Configuration

Top View



DG200A

Dual Monolithic SPST CMOS Analog Switch

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V^-
V^+ 44V
GND 25V
Digital Inputs V_S, V_D (Note 1) .... -2V to (V^+ +2V) or 20mA, whichever occurs first.
Current, Any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
(Pulsed at 1msec, 10% duty cycle max) 100mA
Storage Temperature (A & B Suffix) .... -65 to 150°C
(C Suffix) .... -65 to 125°C

Operating Temperature (A Suffix) .... -55 to 125°C
(B Suffix) .... -25 to 85°C
(C Suffix) .... -25 to 85°C
(D Suffix) .... -40 to 85°C
Power Dissipation (Package)*
Metal Can** 450mW
14 Pin Ceramic DIP*** 825mW
14 Pin Plastic DIP**** 470mW
* All leads soldered or welded to PC board.
** Derate 6mW/°C above 75°C.
*** Derate 11mW/°C above 75°C.
**** Derate 6.5mW/°C above 25°C.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = +15V, V^- = −15V, GND = 0V, T_A = 25° C, unless otherwise indicated.)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS DG200A MIN (Note 2)	TYP (Note 3)	MAX	LIMITS DG200 B/C/D MIN (Note 2)	TYP (Note 3)	MAX	UNITS
SWITCH										
Analog Signal Range (Note 1)	V_{ANALOG}			−15		15	−15		15	V
Drain-Source ON Resistance	$r_{DS(on)}$	V_D = ±10V, V_{in} = 0.8V, I_S = 1mA			45	70		45	80	Ω
Source OFF Leakage Current	$I_{S(off)}$	V_{in} = 2.4V	V_S = 14V, V_D = −14V		0.01	2.0		0.01	5.0	nA
			V_S = −14V, V_D = 14V	-2.0	-0.02		-5.0	-0.02		
Drain OFF Leakage Current	$I_{D(off)}$		V_S = −14V, V_D = 14V		0.01	2.0		0.01	5.0	
			V_S = 14V, V_D = −14V	-2.0	-0.02		-5.0	-0.02		
Drain ON Leakage Current (Note 4)	$I_{D(on)}$	V_{in} = 0.8V	V_S = V_D = 14V		0.1	2.0		0.1	5.0	
			V_S = V_D = −14V	-2.0	-0.1		-5.0	-0.1		
INPUT										
Input Current with Input Voltage High	I_{INH}	V_{in} = 2.4V, V_{in} = 15V		−1.0	0.0009		−1.0	0.0009		µA
					0.005	1.0		0.005	1.0	
Input Current with Input Voltage Low	I_{INL}	V_{in} = 0V		−1.0	-0.0015		−1.0	-0.0015		
DYNAMIC										
Turn-ON Time	t_{on}	See Switching Time Test Circuit (Figure 1)			440	1000		440	1000	ns
Turn-OFF Time	t_{off}				70	500		70	500	
Charge Injection	Q	C_L = 1000pF, V_{GEN} = 0V, R_{GEN} = 0Ω (Figure 2)			10			10		pC
Source OFF Capacitance	$C_{S(off)}$	f = 140kHz V_{in} = 5V or V_S = 0V	V_S = 0V		9.0			9.0		pF
Drain OFF Capacitance	$C_{D(off)}$		V_D = 0V		9.0			9.0		
Channel ON Capacitance	$C_{D(on)}$ + $C_{S(on)}$		V_D = V_S = 0V		25			26		
OFF Isolation Figure 3 (Note 5)		V_{in} = 5V, Z_L = 75Ω V_S = 2.0V, f = 1MHz			75			75		dB
Crosstalk Figure 4 (Channel to Channel)					90			90		

ELECTRICAL CHARACTERISTICS (continued)

($V^+ = +15V$, $V^- = -15V$, GND = 0V, $T_A = 25°C$, unless otherwise indicated.)

PARAMETER	SYMBOL	TEST CONDITIONS	DG200A MIN (Note 2)	DG200A TYP (Note 3)	DG200A MAX	DG200 B/C/D MIN (Note 2)	DG200 B/C/D TYP (Note 3)	DG200 B/C/D MAX	UNITS
SUPPLY									
Positive Supply Current	I+	Both Channels ON or OFF V_{in} = 0 and 2.4V		180	300		200	500	µA
Negative Supply Current	I−		−10	−0.1		−100	−0.1		

ELECTRICAL CHARACTERISTICS (Over Temperature)

($V^+ = +15V$, $V^- = -15V$, GND = 0V, T_A = Over Temperature Range, unless otherwise indicated.)

PARAMETER	SYMBOL	TEST CONDITIONS		DG200A MIN (Note 2)	DG200A TYP (Note 3)	DG200A MAX	DG200 B/C MIN (Note 2)	DG200 B/C TYP (Note 3)	DG200 B/C MAX	UNITS
SWITCH										
Analog Signal Range (Note 1)	V_{ANALOG}			−15		15	−15		15	V
Drain-Source ON Resistance	$r_{DS(on)}$	$V_D = \pm 10V$, $V_{in} = 0.8V$, $I_S = 1mA$				100			100	Ω
Source OFF Leakage Current	$I_{S(off)}$	$V_{in} = 2.4V$	$V_S = 14V$, $V_D = -14V$			100			100	nA
			$V_S = -14V$, $V_D = 14V$	−100			−100			
Drain OFF Leakage Current	$I_{D(off)}$		$V_S = -14V$, $V_D = 14V$			100			100	
			$V_S = 14V$, $V_D = -14V$	−100			−100			
Drain ON Leakage Current (Note 4)	$I_{D(on)}$	$V_{in} = 0.8V$	$V_S = V_D = 14V$			200			200	
			$V_S = V_D = -14V$	−200			−200			
INPUT										
Input Current/ Voltage High	I_{INH}	$V_{in} = 2.4V$, $V_{in} = 15V$		−10			−10			µA
						10			10	
Input Current/ Voltage Low	I_{INL}	$V_{in} = 0V$		−10			−10			

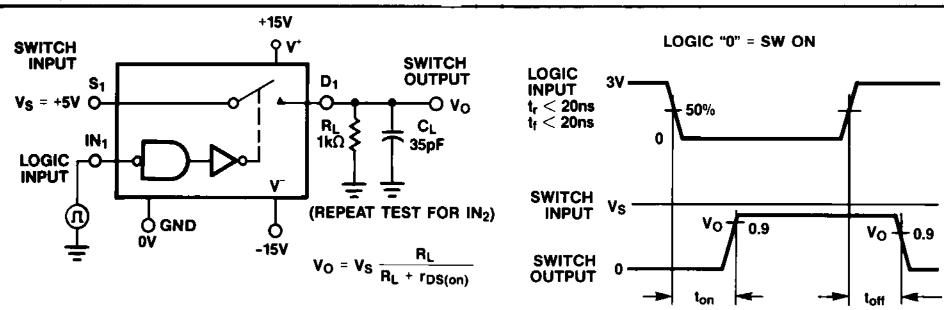
Note 1: Signals on S_X, D_X, or IN_X, exceeding V^- or V^+ will be clamped by internal diodes. LIMIT FORWARD DIODE CURRENT to maximum current ratings.

Note 2: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.

Note 3: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Note 4: $I_{D(on)}$ is leakage from driver into "ON" switch.

Note 5: "OFF" isolation = 20 log V_S/V_D, V_S = input to OFF switch, V_D = output.



NOTE: Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

Figure 1. Switching Time Test Circuit

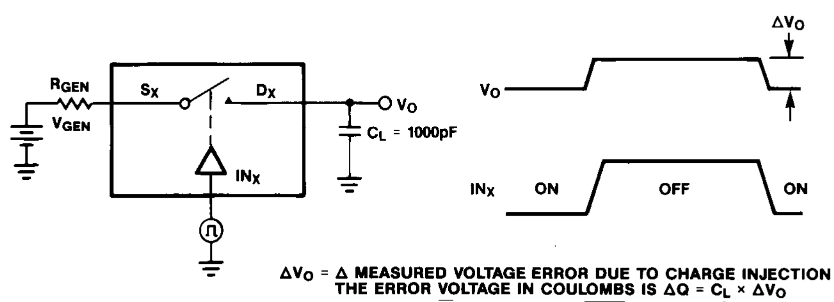


Figure 2. Charge Injection Test Circuit

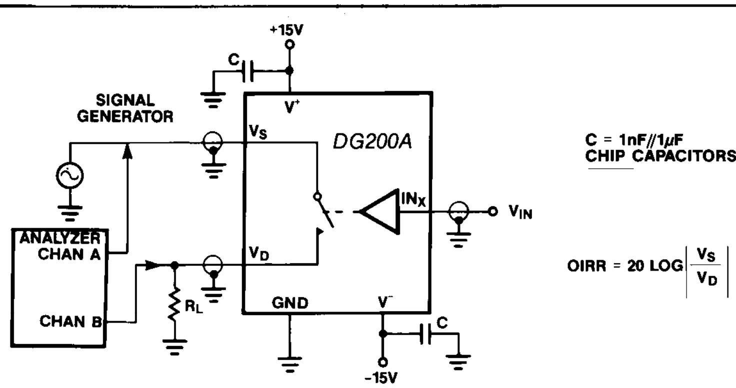


Figure 3. OFF Isolation Test Circuit

National Semiconductor

August 2000

LM741
Operational Amplifier

General Description

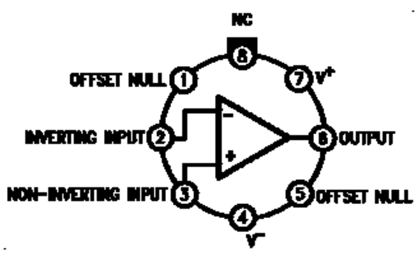
The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0˚C to +70˚C temperature range, instead of −55˚C to +125˚C.

Connection Diagrams

Metal Can Package

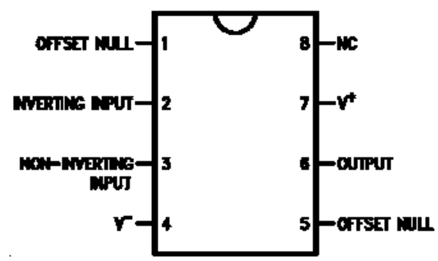


DS009341-2

Note 1: LM741H is available per JM38510/10101

Order Number LM741H, LM741H/883 (Note 1), **LM741AH/883 or LM741CH**
See NS Package Number H08C

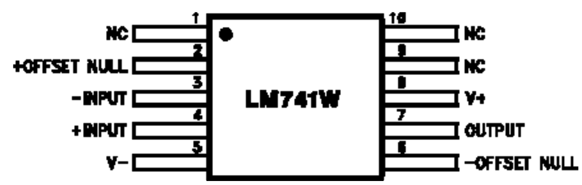
Dual-In-Line or S.O. Package



DS009341-3

Order Number LM741J, LM741J/883, LM741CN
See NS Package Number J08A, M08A or N08E

Ceramic Flatpak

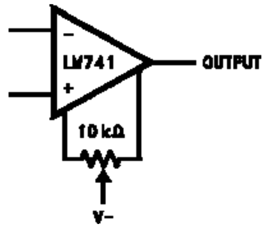


DS009341-6

Order Number LM741W/883
See NS Package Number W10A

Typical Application

Offset Nulling Circuit



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 DS009341

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 7)

	LM741A	LM741	LM741C
Supply Voltage	±22V	±22V	±18V
Power Dissipation (Note 3)	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V
Input Voltage (Note 4)	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	150°C	100°C
Soldering Information			
N-Package (10 seconds)	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C
M-Package			
Vapor Phase (60 seconds)	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

	LM741A	LM741	LM741C
ESD Tolerance (Note 8)	400V	400V	400V

Electrical Characteristics (Note 5)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C										
	$R_S \le 10\ k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \le 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 50\Omega$			4.0							mV
	$R_S \le 10\ k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							μV/°C
Input Offset Voltage Adjustment Range	T_A = 25°C, V_S = ±20V	±10				±15			±15		mV
Input Offset Current	T_A = 25°C		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	T_A = 25°C		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	μA
Input Resistance	T_A = 25°C, V_S = ±20V	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, V_S = ±20V	0.5									MΩ
Input Voltage Range	T_A = 25°C							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V

Electrical Characteristics (Note 5) (Continued)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	T_A = 25˚C, $R_L \geq 2$ kΩ										
	V_S = ±20V, V_O = ±15V	50									V/mV
	V_S = ±15V, V_O = ±10V				50	200		20	200		V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $R_L \geq 2$ kΩ,										
	V_S = ±20V, V_O = ±15V	32									V/mV
	V_S = ±15V, V_O = ±10V				25			15			V/mV
	V_S = ±5V, V_O = ±2V	10									V/mV
Output Voltage Swing	V_S = ±20V										
	$R_L \geq 10$ kΩ	±16									V
	$R_L \geq 2$ kΩ	±15									V
	V_S = ±15V										
	$R_L \geq 10$ kΩ				±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ				±10	±13		±10	±13		V
Output Short Circuit Current	T_A = 25˚C	10	25	35		25			25		mA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Common-Mode Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
	$R_S \leq 10$ kΩ, V_{CM} = ±12V				70	90		70	90		dB
	$R_S \leq 50Ω$, V_{CM} = ±12V	80	95								dB
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
	V_S = ±20V to V_S = ±5V										
	$R_S \leq 50Ω$	86	96								dB
	$R_S \leq 10$ kΩ				77	96		77	96		dB
Transient Response	T_A = 25˚C, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		µs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 6)	T_A = 25˚C	0.437	1.5								MHz
Slew Rate	T_A = 25˚C, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current	T_A = 25˚C					1.7	2.8		1.7	2.8	mA
Power Consumption	T_A = 25˚C										
	V_S = ±20V		80	150							mW
	V_S = ±15V					50	85		50	85	mW
LM741A	V_S = ±20V										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741	V_S = ±15V										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 2: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Electrical Characteristics (Note 5) (Continued)

Note 3: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100˚C/W	100˚C/W	170˚C/W	195˚C/W
θ_{jC} (Junction to Case)	N/A	N/A	25˚C/W	N/A

Note 4: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

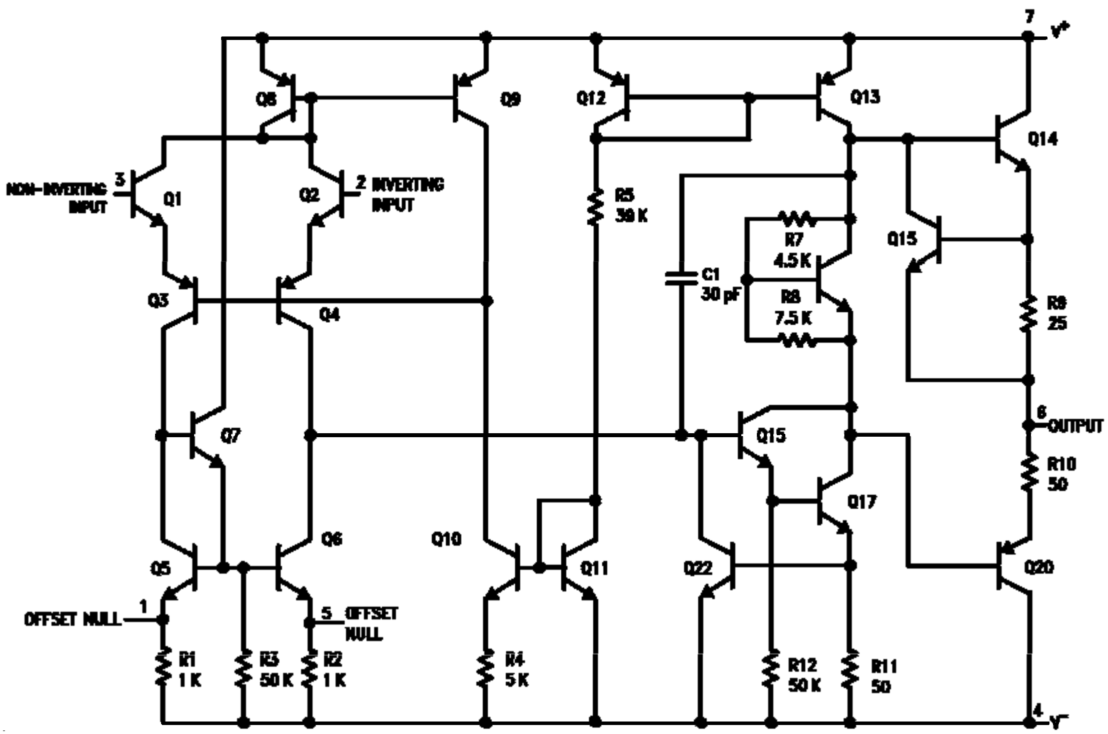
Note 5: Unless otherwise specified, these specifications apply for V_S = ±15V, −55˚C ≤ T_A ≤ +125˚C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0˚C ≤ T_A ≤ +70˚C.

Note 6: Calculated value from: BW (MHz) = 0.35/Rise Time(µs).

Note 7: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Schematic Diagram



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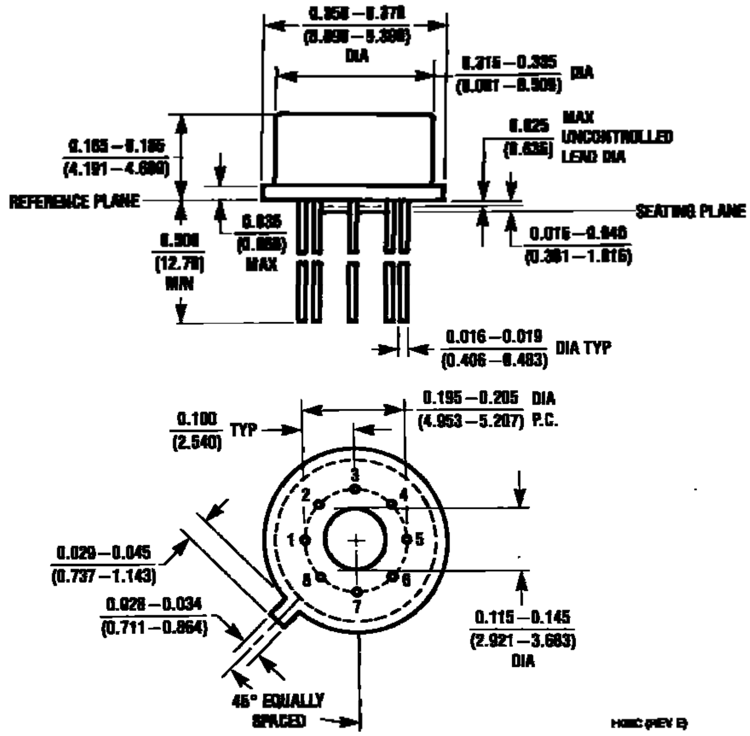
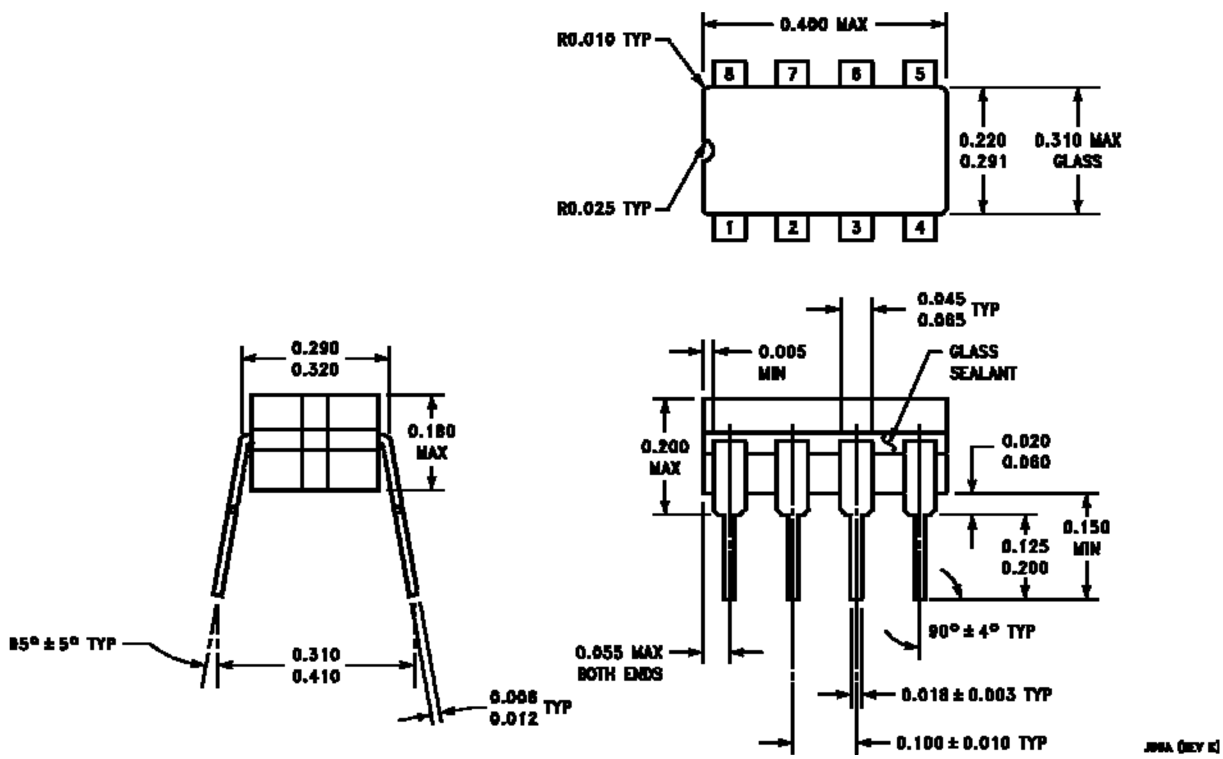
Physical Dimensions inches (millimeters) unless otherwise noted

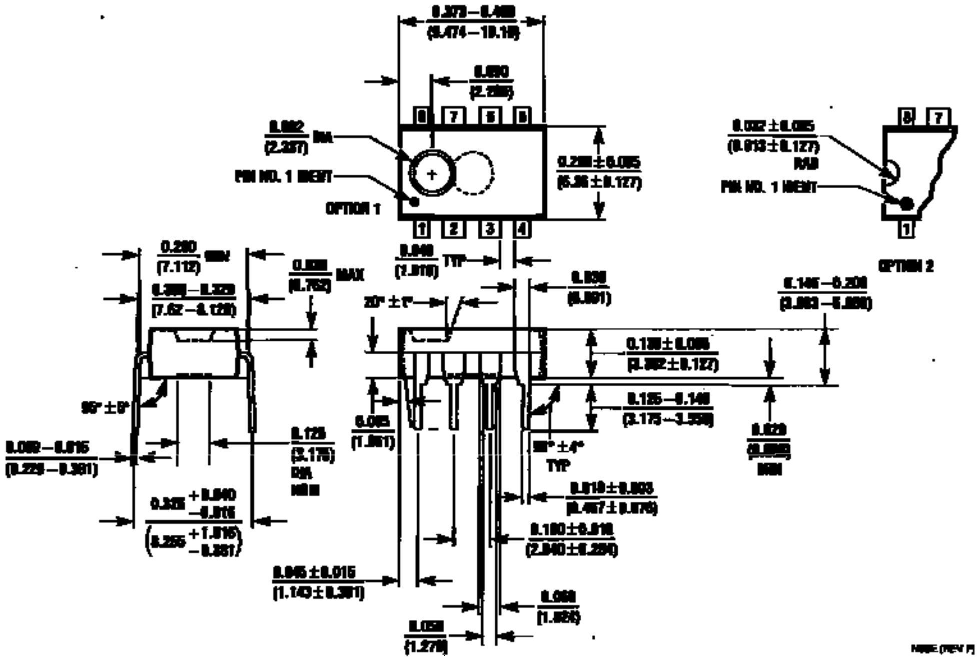


Metal Can Package (H)
Order Number LM741H, LM741H/883, LM741AH/883, LM741AH-MIL or LM741CH
NS Package Number H08C

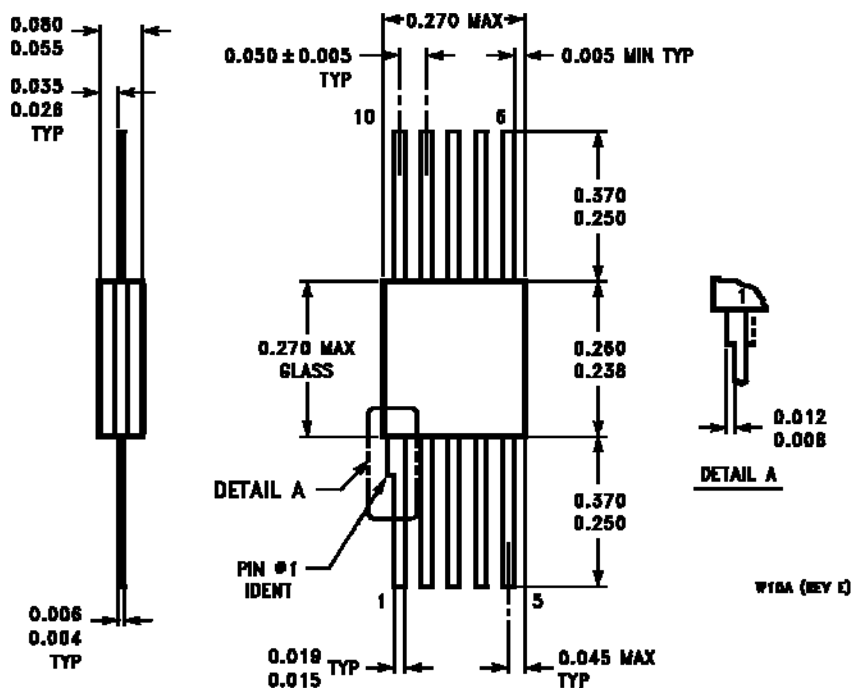


Ceramic Dual-In-Line Package (J)
Order Number LM741J/883
NS Package Number J08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Dual-In-Line Package (N)
Order Number LM741CN
NS Package Number N08E



10-Lead Ceramic Flatpak (W)
Order Number LM741W/883, LM741WG-MPR or LM741WG/883
NS Package Number W10A

Notes

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National Semiconductor

July 2000

LF198/LF298/LF398, LF198A/LF398A Monolithic Sample-and-Hold Circuits

General Description

The LF198/LF298/LF398 are monolithic sample-and-hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 µs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 µF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

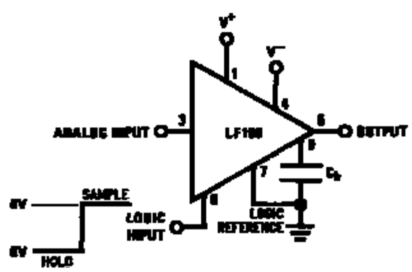
Features

- Operates from ±5V to ±18V supplies
- Less than 10 µs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at C_h = 0.01 µF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth
- Space qualified, JM38510

Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies.

An "A" version is available with tightened electrical specifications.

Typical Connection and Performance Curve



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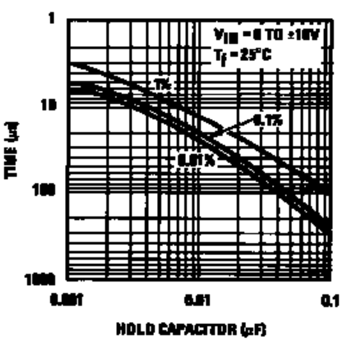
Acquisition Time



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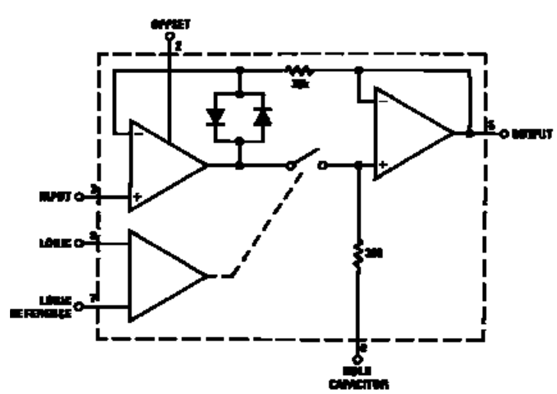
Functional Diagram



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 DS005692

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Package Limitation) (Note 2)	500 mW
Operating Ambient Temperature Range	
LF198/LF198A	−55˚C to +125˚C
LF298	−25˚C to +85˚C
LF398/LF398A	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C
Input Voltage	Equal to Supply Voltage
Logic To Logic Reference Differential Voltage (Note 3)	+7V, −30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Note 4)	
H package (Soldering, 10 sec.)	260˚C
N package (Soldering, 10 sec.)	260˚C
M package:	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C

Thermal Resistance (θ_{JA}) (typicals)

H package 215˚C/W (Board mount in still air)

85˚C/W (Board mount in 400LF/min air flow)

N package 115˚C/W

M package 106˚C/W

θ_{JC} (H package, typical) 20˚C/W

Electrical Characteristics

The following specifcations apply for $-V_S + 3.5V \le V_{IN} \le +V_S - 3.5V$, $+V_S = +15V$, $-V_S = -15V$, $T_A = T_j = 25˚C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0V, LOGIC HIGH = 2.5V, LOGIC LOW = 0V unless otherwise specified.

Parameter	Conditions	LF198/LF298			LF398			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage, (Note 5)	T_j = 25˚C		1	3		2	7	mV
	Full Temperature Range			5			10	mV
Input Bias Current, (Note 5)	T_j = 25˚C		5	25		10	50	nA
	Full Temperature Range			75			100	nA
Input Impedance	T_j = 25˚C		10^{10}			10^{10}		Ω
Gain Error	T_j = 25˚C, R_L = 10k		0.002	0.005		0.004	0.01	%
	Full Temperature Range			0.02			0.02	%
Feedthrough Attenuation Ratio at 1 kHz	T_j = 25˚C, C_h = 0.01 µF	86	96		80	90		dB
Output Impedance	T_j = 25˚C, “HOLD” mode		0.5	2		0.5	4	Ω
	Full Temperature Range			4			6	Ω
“HOLD” Step, (Note 6)	T_j = 25˚C, C_h = 0.01 µF, V_{OUT} = 0		0.5	2.0		1.0	2.5	mV
Supply Current, (Note 5)	T_j≥25˚C		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	T_j = 25˚C		2	10		2	10	µA
Leakage Current into Hold Capacitor (Note 5)	T_j = 25˚C, (Note 7) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	ΔV_{OUT} = 10V, C_h = 1000 pF		4			4		µs
	C_h = 0.01 µF		20			20		µs
Hold Capacitor Charging Current	V_{IN}−V_{OUT} = 2V		5			5		mA
Supply Voltage Rejection Ratio	V_{OUT} = 0	80	110		80	110		dB
Differential Logic Threshold	T_j = 25˚C	0.8	1.4	2.4	0.8	1.4	2.4	V
Input Offset Voltage, (Note 5)	T_j = 25˚C		1	1		2	2	mV
	Full Temperature Range			2			3	mV
Input Bias Current, (Note 5)	T_j = 25˚C		5	25		10	25	nA
	Full Temperature Range			75			50	nA

Electrical Characteristics

The following specifcations apply for $-V_S + 3.5V \leq V_{IN} \leq +V_S - 3.5V$, $+V_S = +15V$, $-V_S = -15V$, $T_A = T_j = 25^\circ C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0V, LOGIC HIGH = 2.5V, LOGIC LOW = 0V unless otherwise specified.

Parameter	Conditions	LF198A			LF398A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Impedance	$T_j = 25^\circ C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25^\circ C$, $R_L = 10k$		0.002	0.005		0.004	0.005	%
	Full Temperature Range			0.01			0.01	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25^\circ C$, $C_h = 0.01\ \mu F$	86	96		86	90		dB
Output Impedance	$T_j = 25^\circ C$, “HOLD” mode		0.5	1		0.5	1	Ω
	Full Temperature Range			4			6	Ω
“HOLD” Step, (Note 6)	$T_j = 25^\circ C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	1		1.0	1	mV
Supply Current, (Note 5)	$T_j \geq 25^\circ C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25^\circ C$		2	10		2	10	µA
Leakage Current into Hold Capacitor (Note 5)	$T_j = 25^\circ C$, (Note 7) Hold Mode		30	100		30	100	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000\ pF$		4	6		4	6	µs
	$C_h = 0.01\ \mu F$		20	25		20	25	µs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	90	110		90	110		dB
Differential Logic Threshold	$T_j = 25^\circ C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Note 1: “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$, or the number given in the Absolute Maximum Ratings, whichever is lower. The maximum junction temperature, T_{JMAX}, for the LF198/LF198A is 150˚C; for the LF298, 115˚C; and for the LF398/LF398A, 100˚C.

Note 3: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 4: See AN-450 “Surface Mounting Methods and their effects on Product Reliability” for other methods of soldering surface mount devices.

Note 5: These parameters guaranteed over a supply voltage range of ±5 to ±18V, and an input range of $-V_S + 3.5V \leq V_{IN} \leq +V_S - 3.5V$.

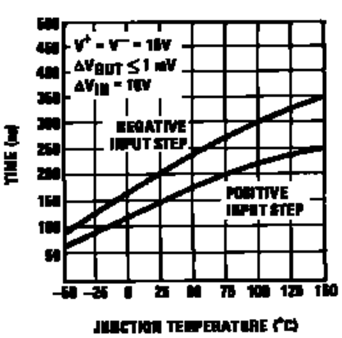
Note 6: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01µF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 7: Leakage current is measured at a junction temperature of 25˚C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25˚C value for each 11˚C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 8: A military RETS electrical test specification is available on request. The LF198 may also be procured to Standard Military Drawing #5962-8760801GA or to MIL-STD-38510 part ID JM38510/12501SGA.

Typical Performance Characteristics

Aperture Time
(Note 9)



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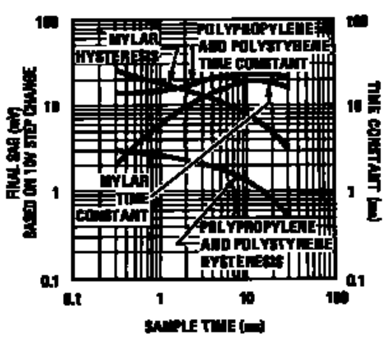
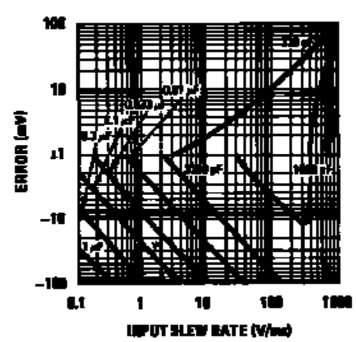
Dielectric Absorption Error in Hold Capacitor



DS005692-18

Dynamic Sampling Error

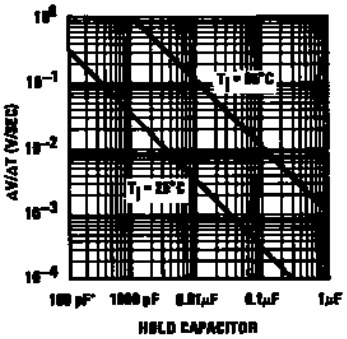


DS005692-19

Note 9: See Definition of Terms

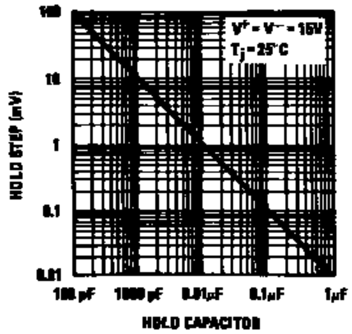
Typical Performance Characteristics (Continued)

Output Droop Rate



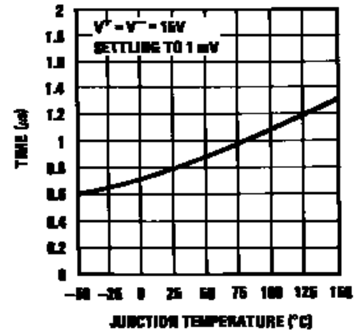
DS005692-20

Hold Step



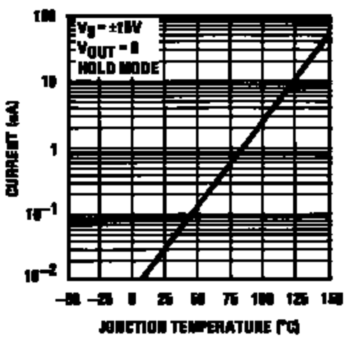
DS005692-21

"Hold" Settling Time
(Note 10)



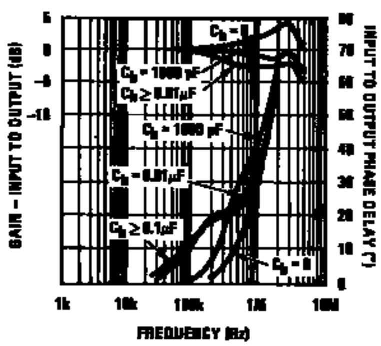
DS005692-22

Leakage Current into Hold Capacitor



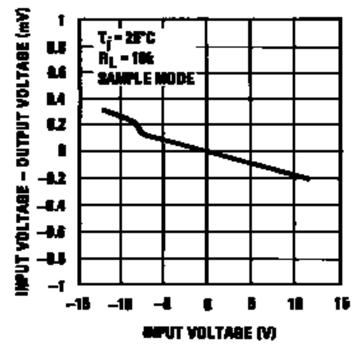
DS005692-23

Phase and Gain (Input to Output, Small Signal)



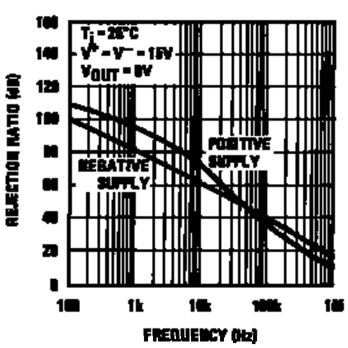
DS005692-24

Gain Error



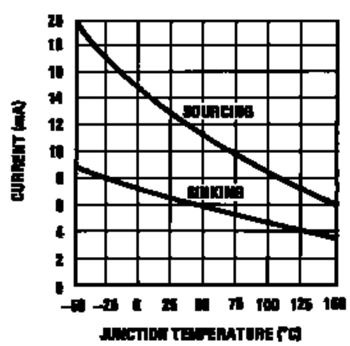
DS005692-25

Power Supply Rejection



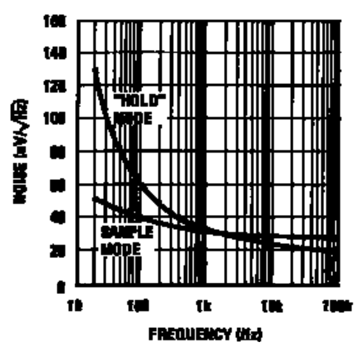
DS005692-26

Output Short Circuit Current



DS005692-27

Output Noise



DS005692-28

Note 10: See Definition