PRACTICAL WORKBOOK

FOR ACADEMIC SESSION 2014

ANALOG INTEGRATED CIRCUITS (EL-302)
THIRD YEAR ELECTRONICS

Name:

Roll Number:

Class:

Batch:

Department :

Department of Electronic Engineering
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LABORATORY WORKBOOK

FOR THE COURSE

EL-302 ANALOG INTEGRATED CIRCUITS

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ANALOG INTEGRATED CIRCUITS LABORATORY

CONTENTS

Lab No. 1

INTRODUCTION:

We will be working in three regions during AIC lab.

First of all you will be introduced to a new software i-e Mentor Graphics (IC Studio).

Secondly you people will have to implement labs on Orcad PSpice, which will the work done in pre-lab.

Thirdly you will be implementing circuits on bread board so as to get hands on experience.

Before coming to the introduction of Mentor Graphics let's have a look at the types of ICs:

TYPES OF IC:

1. Standard Product
2. Application Specific Integrated Circuit (ASIC)
    a) Full Custom
    b) Semi custom

1. STANDARD PRODUCT:

A standard product is produced by the manufacturer for sale to the general public. Standard products are readily available for use by anybody for a wider range of applications.

2. APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC)

The term '**ASIC**' stands for '**application-specific integrated circuit**'. An ASIC is basically an integrated circuit designed specifically for a special purpose or application. Strictly speaking, this also implies that an ASIC is built only for one and only one customer. An example of an ASIC is an IC designed for a specific line of cellular phones of a company, whereby no other products can use it except the cell phones belonging to that product line. The opposite of an ASIC is a standard product or general purpose IC, such as a logic gate or a general purpose microcontroller, both of which can be used in any electronic application by anybody.

Aside from the nature of its application, an ASIC differs from a standard product in the nature of its availability. The intellectual property, design database, and deployment of an

ASIC is usually controlled by just a single entity or company, which is generally the end-user of the ASIC too. Thus, an ASIC is proprietary by nature and not available to the general public.

a) FULL-CUSTOM

Full-custom ASIC's are those that are entirely tailor-fitted to a particular application from the very start. Since its ultimate design and functionality is pre-specified by the user, it is manufactured with all the photolithographic layers of the device already fully defined, just like most off-the-shelf general purpose IC's. The use of predefined masks for manufacturing leaves no option for circuit modification during fabrication, except perhaps for some minor fine-tuning or calibration. This means that a full-custom ASIC cannot be modified to suit different applications, and is generally produced as a single, specific product for a particular application only.

b) SEMI-CUSTOM ASIC:

Semi-custom ASIC's, on the other hand, can be partly customized to serve different functions within its general area of application. Unlike full-custom ASIC's, semi-custom ASIC's are designed to allow a certain degree of modification during the manufacturing process. A semi-custom ASIC is manufactured with the masks for the diffused layers already fully defined, so the transistors and other active components of the circuit are already fixed for that semi-custom ASIC design. The customization of the final ASIC product to the intended application is done by varying the masks of the interconnection layers, e.g., the metallization layers.

INTRODUCTION TO MENTOR GRAPHICS:

Mentor Graphics IC Studio is an EDA software .Electronic Design Automation (EDA or ECAD) is a category of software tools for designing electronic systems such as printed circuit boards and integrated circuits. The tools work together in a design flow that chip designers use to design and analyze entire semiconductor chips.

TOOLS IN MENTOR GRAPHICS:

1. Back end tools - IC Nanometer Design- Category 1
2. Front end tools-Design Verification & Test- Category 2
3. PCB Tools - PCB PADS- Category 3b

We will be using the Back end tools

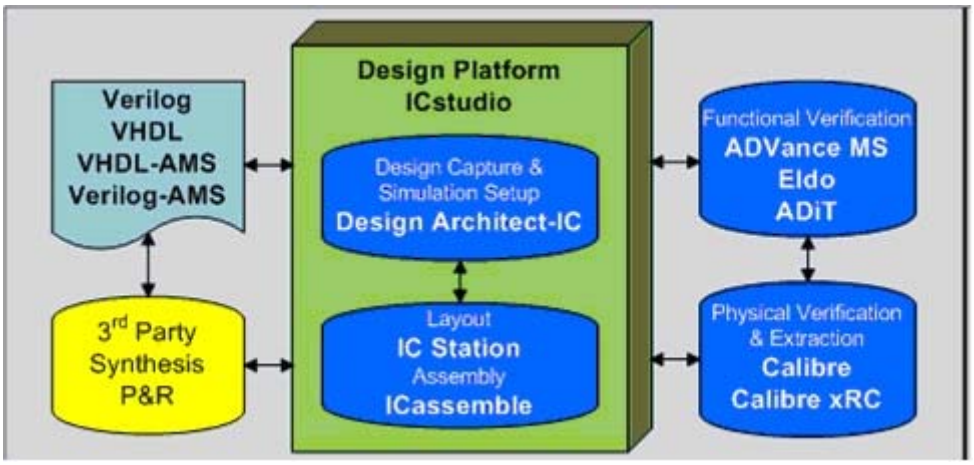


Fig 1.IC Nanometer Design

- **Design Architect-IC** - A powerful tool for schematic capture, netlisting, simulation setup and results viewing.
- **IC Station** - Provides the physical layout component of the Mentor Graphics full custom IC design flow. This suite includes application bundles for editing, schematic-driven layout, and top-level floor planning/routing.
- **IC assemble** - A robust set of features for floor planning, top-level assembly and interactive routing.
- **ADVance MS and ADVance MS RF** - A language-neutral, mixed-signal simulator that enables top-down design and bottom-up verification of multi-million gate analog/mixed-signal SoC designs.
- **Eldo and Eldo RF** - An analog simulator offering numerous simulation and modeling options that deliver high-performance and high-speed simulation with the accuracy required by the user.
- **Calibre** - The industry standard platform for physical verification, offering superior performance and capacity for both flat and hierarchical algorithms.
- **CalibrexRC** - Accurate transistor-level, gate-level and hierarchical parasitic extraction.

TECHNOLOGY FILE

The technology file contains process specific parameters such as layer thicknesses and the sheet resistance of the various layers.

Mentor's Technology Design Kit is a comprehensive and proven set of building blocks that enables semiconductor companies and electronics systems manufacturers to jump-start their design cycles using Mentor's analog/mixed-signal (AMS) IC Flow, thereby cutting time-to-market and ensuring manufacturing success of analog, RF and mixed-signal ICs and systems on chip (SoCs).

Mentor Graphics and GLOBALFOUNDRIES Semiconductor have teamed to develop TDKs for popular GLOBALFOUNDRIES manufacturing processes at multiple technology nodes, starting first with 0.18 micron. These AMS TDKs include all the foundry-specific data files and models for use with the Mentor Graphics integrated IC Flow comprised of the following tools: Design Architect-IC for schematic entry, Eldo and ADMS for analog and mixed-signal simulation, IC Station and IC assemble for schematic-driven layout and chip assembly, and Calibre for DRC/LVS verification and extraction.

Lab No. 2

OBJECTIVE:

To learn how to use IC Studio of Mentor Graphics for IC Designing

EQUIPMENT REQUIRED:

Linux and Mentor Graphics (IC Studio) installed PC

THEORY:

Mentor Graphics IC Studio is an EDA software .Electronic Design Automation (EDA or ECAD) is a category of software tools for designing electronic systems such as printed circuit boards and integrated circuits. The tools work together in a design flow that chip designers use to design and analyze entire semiconductor chips.

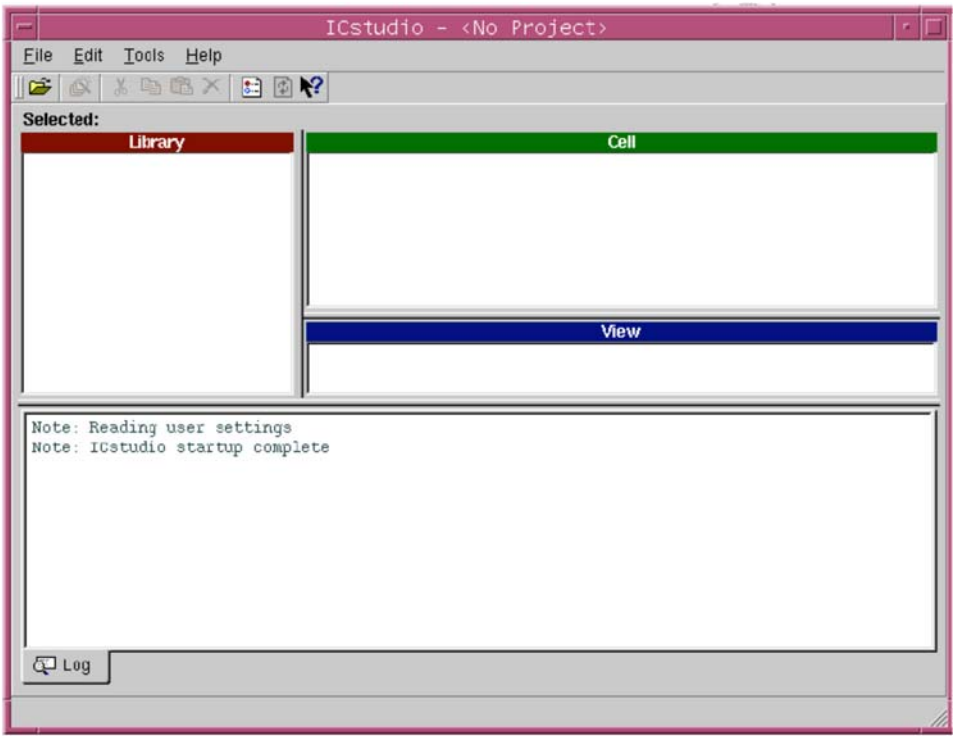
PROCEDURE:

Launching IC Studio:

Open a new terminal and type the following commands:

- **----------**
- **----------**
- **----------**

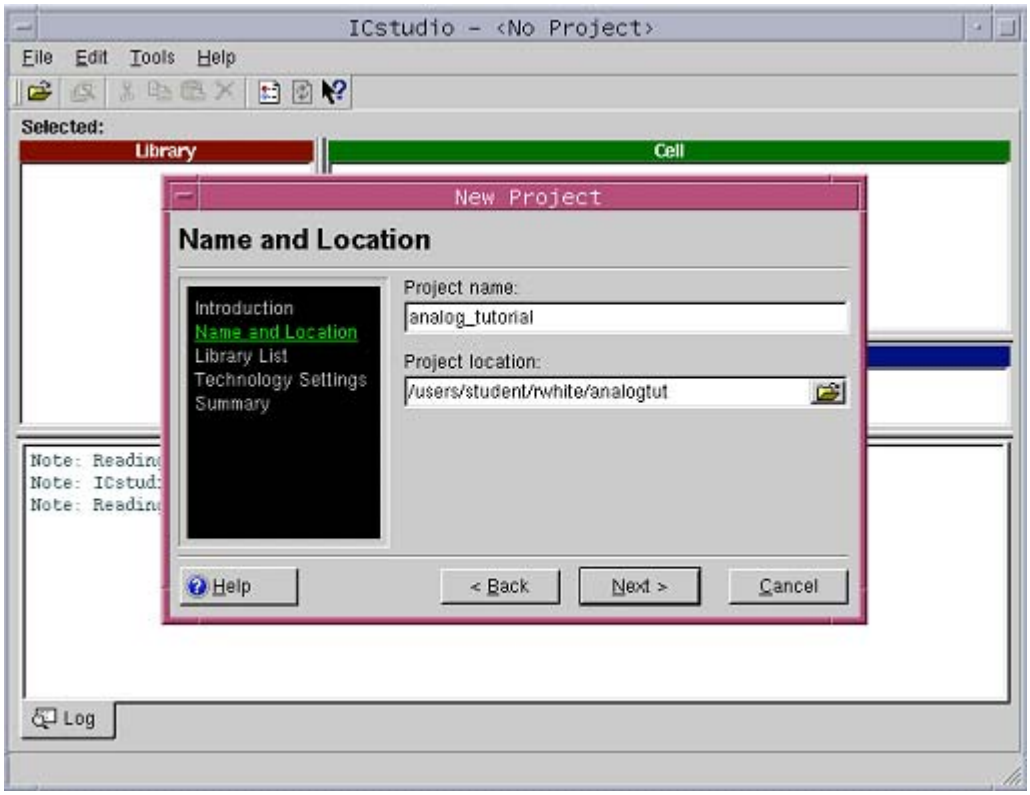
This will launch the window of ic_studio as shown below:



Creating a Project:

On the IC Studio window

- Click **File**>**New**>**Project** to create a new project.
- Click **Next** in the **New Project** pop-up window
- Enter the **Project name** (e.g project1) and the Project Location (**home/student**), click **Next** in the New Project popup window.



Specifying Location Map:

On the next window that appears

- Click the **Open Location Map Editor** button. The Location Map Editor appears.
- To add the design kit's standard cell libraries to the library list
  Click **Edit Menu > Add Standard MGC Libraries** pull down menu item
- Add the **MGC Design kit** to the location map
- Click **Edit Menu > Add MGC Design kit.**
- Specify MGC Design Kit Path as

- The Library List editor looks as in the figure below.
- Click **OK** on the Library List Editor
- Click **Next** on the New Project pop-up window.

Specifying Process files and other settings:

- Click **Open Settings Editor** button. The **Project** tab of the **Preference**s dialog box appears
- Load the process file and rule files.
  Process file and rule files are present in

  Process file:----------

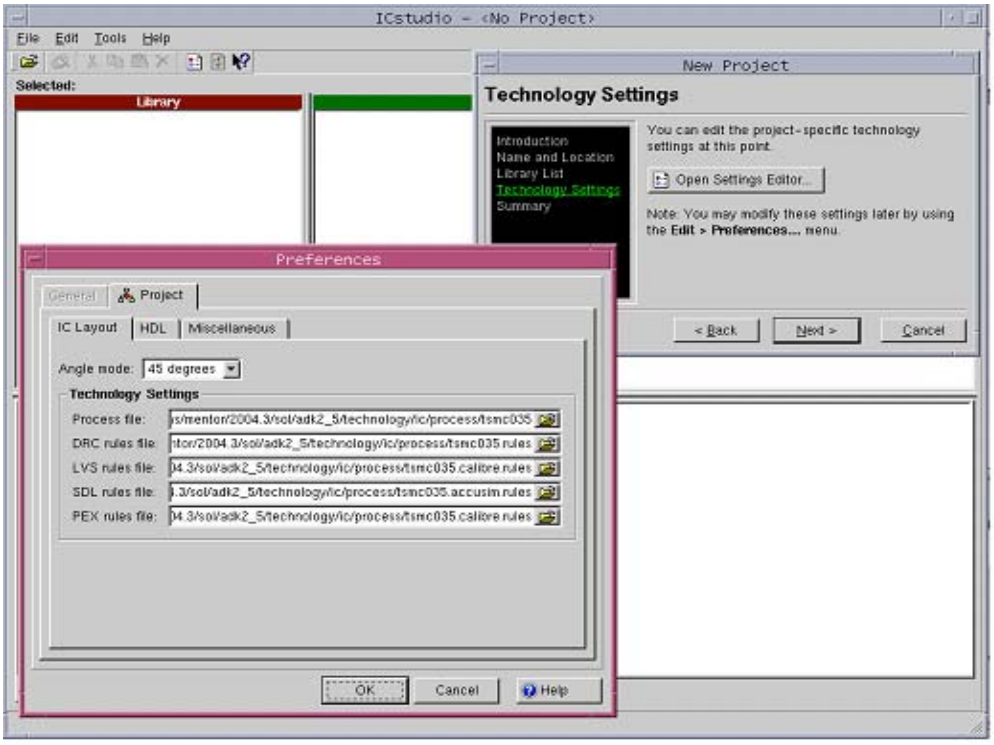
  DRC rules file:----------

  LVS rules file:----------

  SDL rules file:----------

  PEX rules file:----------

- Click **OK** on the Preferences dialog box.

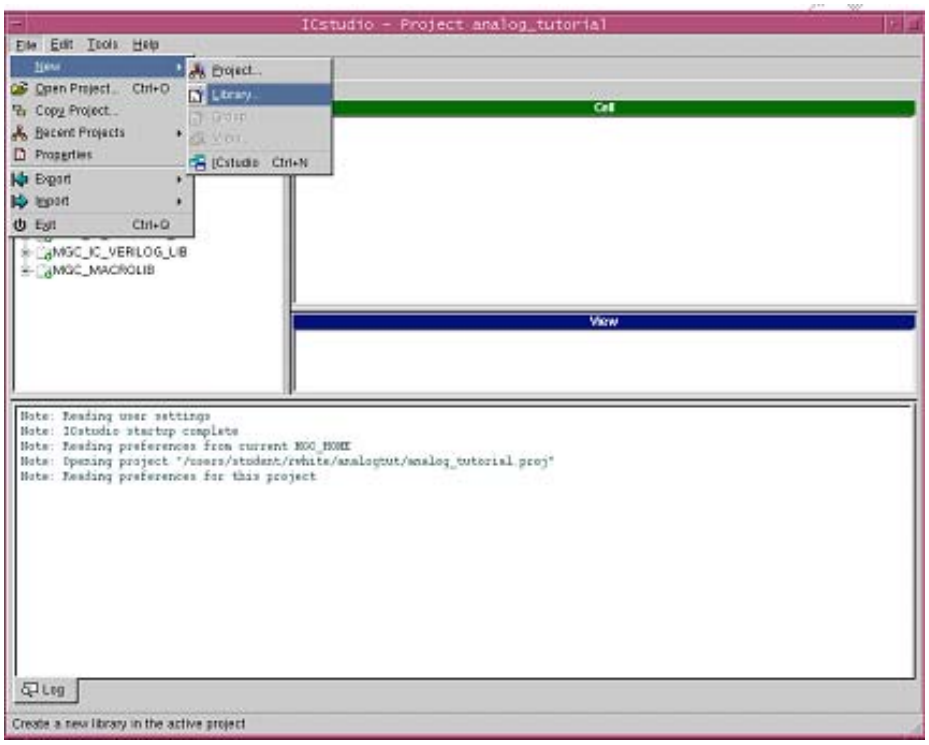


- Click **Next** on the New Project pop-up window
- View the **Summary** to make sure all the information is correct.
- Click **Finish**.

Creating a Library:

- Click **File >New > Library** .This opens the **Create Library** dialogue box.
- Enter the name of the library you want to create (e.g. lib)
- Click **OK**.

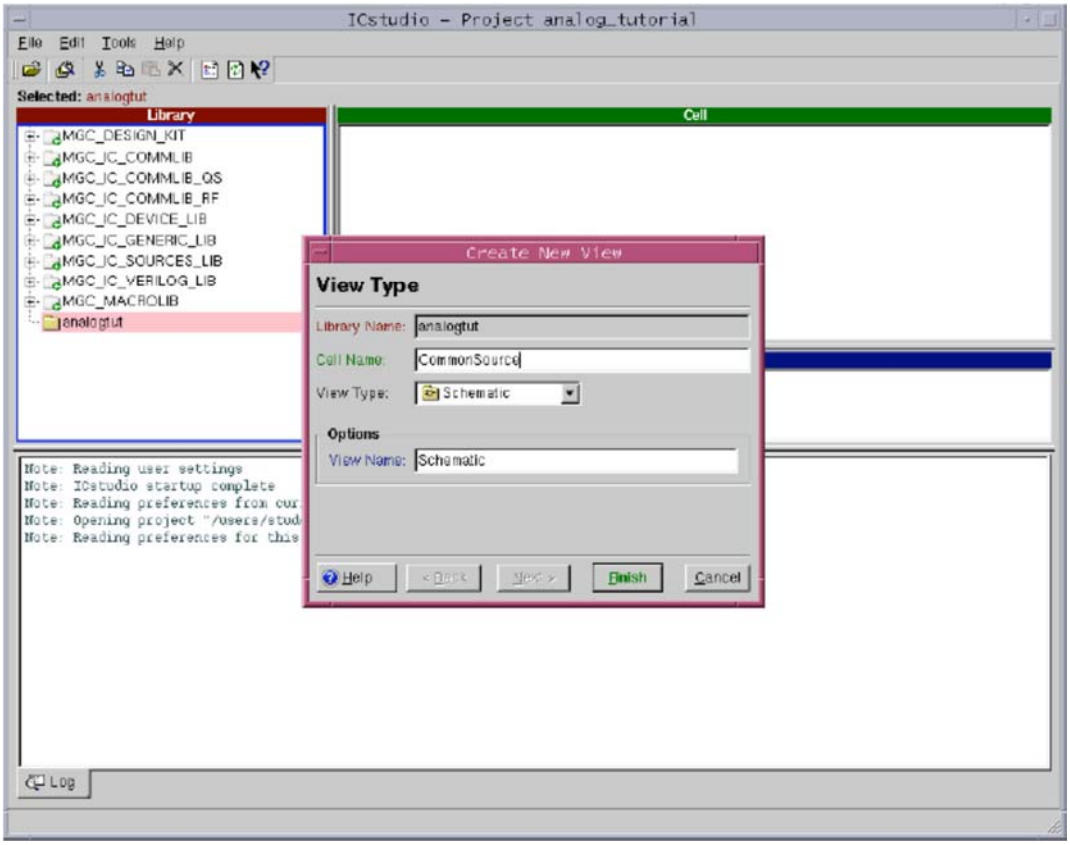
  The library appears in the IC Studio library pane as well as in the location map.



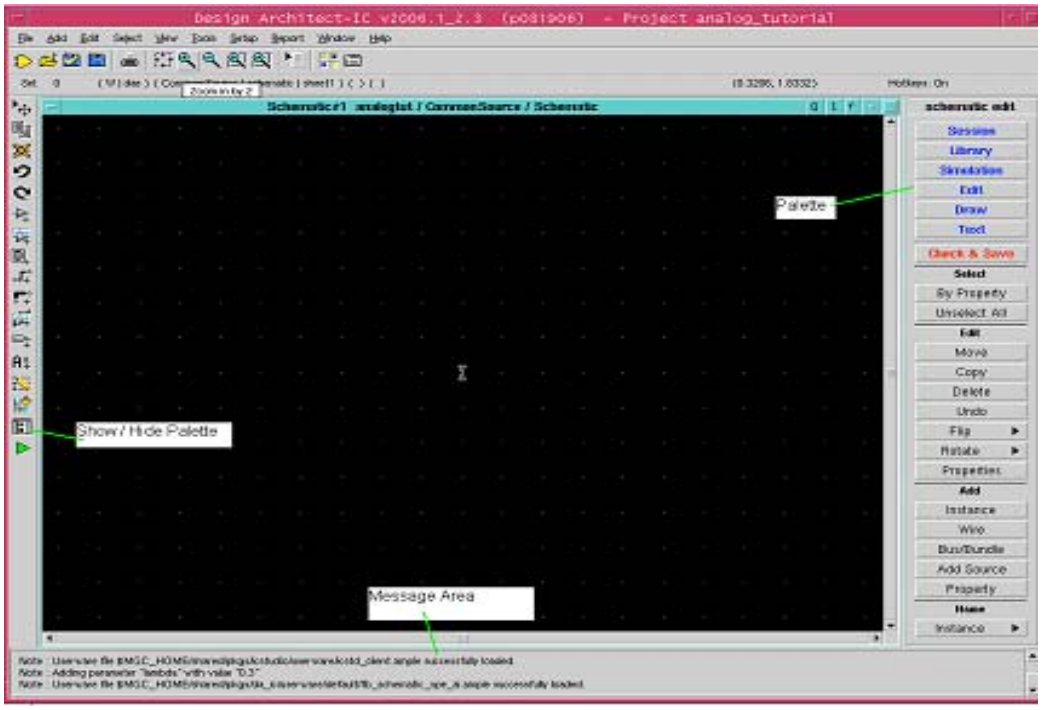
Capturing a Cell:

To create a new Schematic cell:

- Select a library (e.g lib) where you want a cell view to be created.
- Click **File > New >Cell View** .The **Create New View** dialogue box appears
- Enter the **Cell Name** (e.g current source).If the cell does not exist, it is created.
- Specify the **View Type** as **Schematic** and click **Finish**.



Design Architect (DA-IC) will open automatically where in you can capture the required cell design.


Palette
Show / Hide Palette
Message Area

Lab No. 3

OBJECTIVE:

To determine the dc operating points of MOSFET operating in saturation region.

EQUIPMENT REQUIRED:

Linux and Mentor Graphics (IC Studio) installed PC

THEORY:

Modes of operation of MOSFET:

MOSFET can be operated in three modes:

1) Cut off

2) Triode

3) Saturation

To operate the MOSFET as a current source it needs to be operated in saturation region. For an N-MOS to operate in saturation region the operating conditions must be such that

$$v_{DS} \geq v_{GS} - V_t$$

Ideally the current that flows through the MOSFET in saturation region is independent of drain voltage and is given by:

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)^2$$

But practically increasing v_{DS} beyond $v_{DS\,sat}$ causes the channel pinch off point to move slightly away from the drain towards the source which is as shown in figure 1:

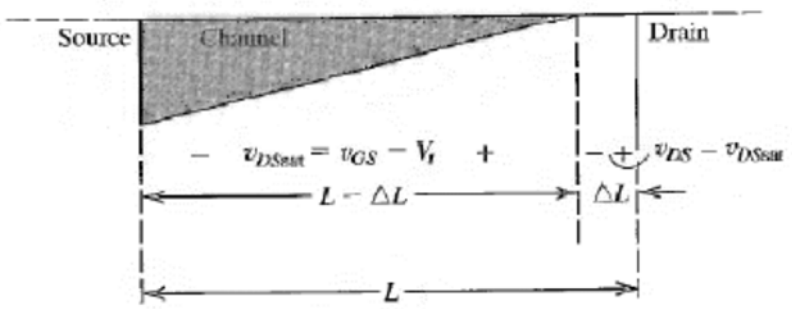


Figure 1: Increasing v_{DS} beyond $v_{DS\,sat}$ reduces the effective channel length.

Hence the voltage across the channel remains constant at $v_{GS} - V_t = v_{DS\,sat}$ and the additional applied voltage applied to the drain appears as a voltage drop across the narrow deplition region between the end of the channel and the drain region .This voltage accelerates the electrons that reach the drain end of the channel and sweeps them across the depletion region into the drain.Now since i_D is inversely propotional to the channel length , I_D increases with V_{DS} .

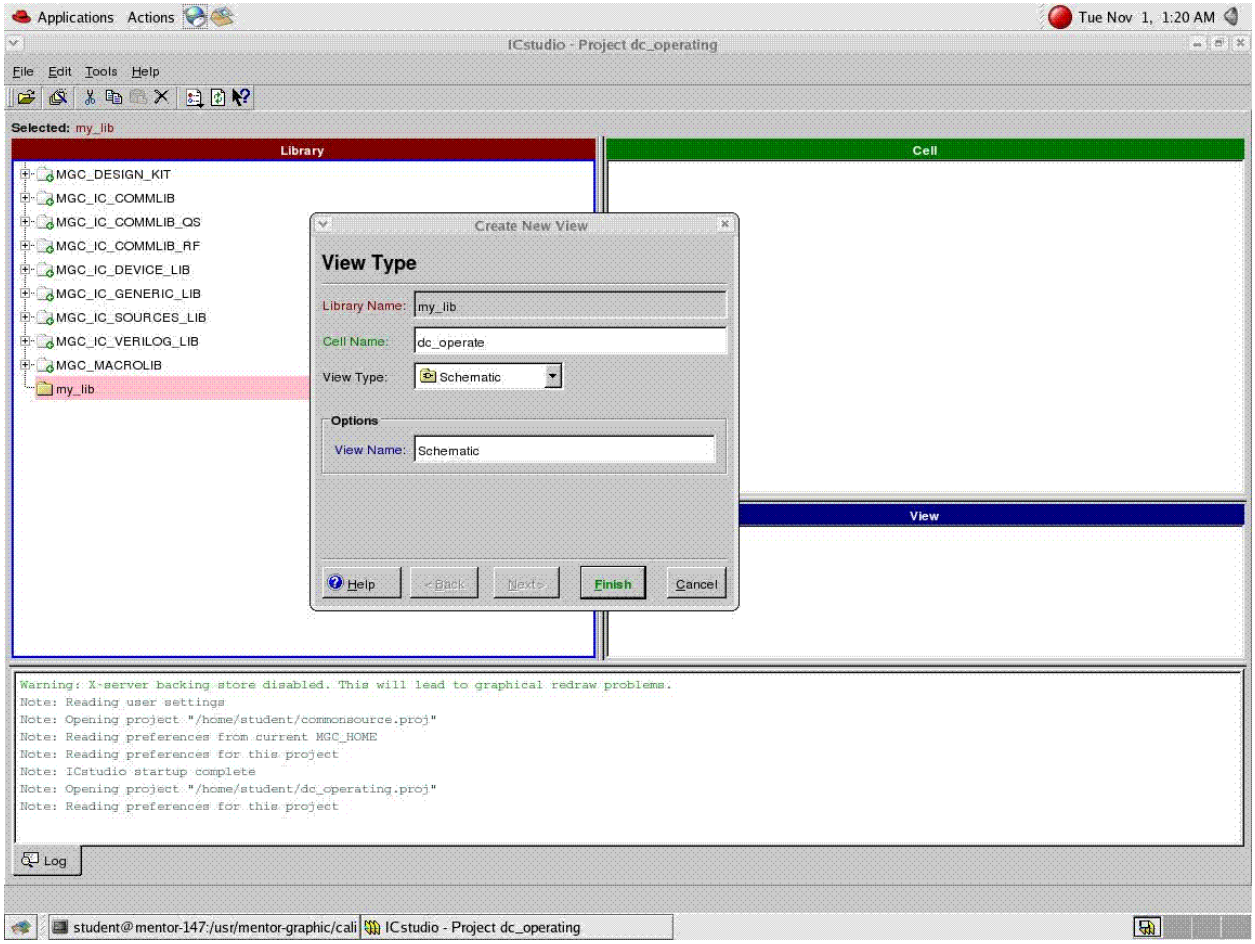
$$i_D = \frac{1}{2}\,\mu_n\, C_{ox}\frac{W}{L}\,(v_{GS} - V_t)^2\,(1 + \lambda v_{DS})$$

PROCEDURE:

Launch IC Studio on Linux as explained in Lab Session 1.

Capturing a Cell:

- Select a library (e.g lib) where you want a cell view to be created.
- Click **File > New > View**. The **Create New Vie**w dialog box appears.
- Enter the **Cell Name** (e.g current source) .If the cell does not exist, it is created.
- Specify the **View Type** as **Schematic** and click **Finish**.

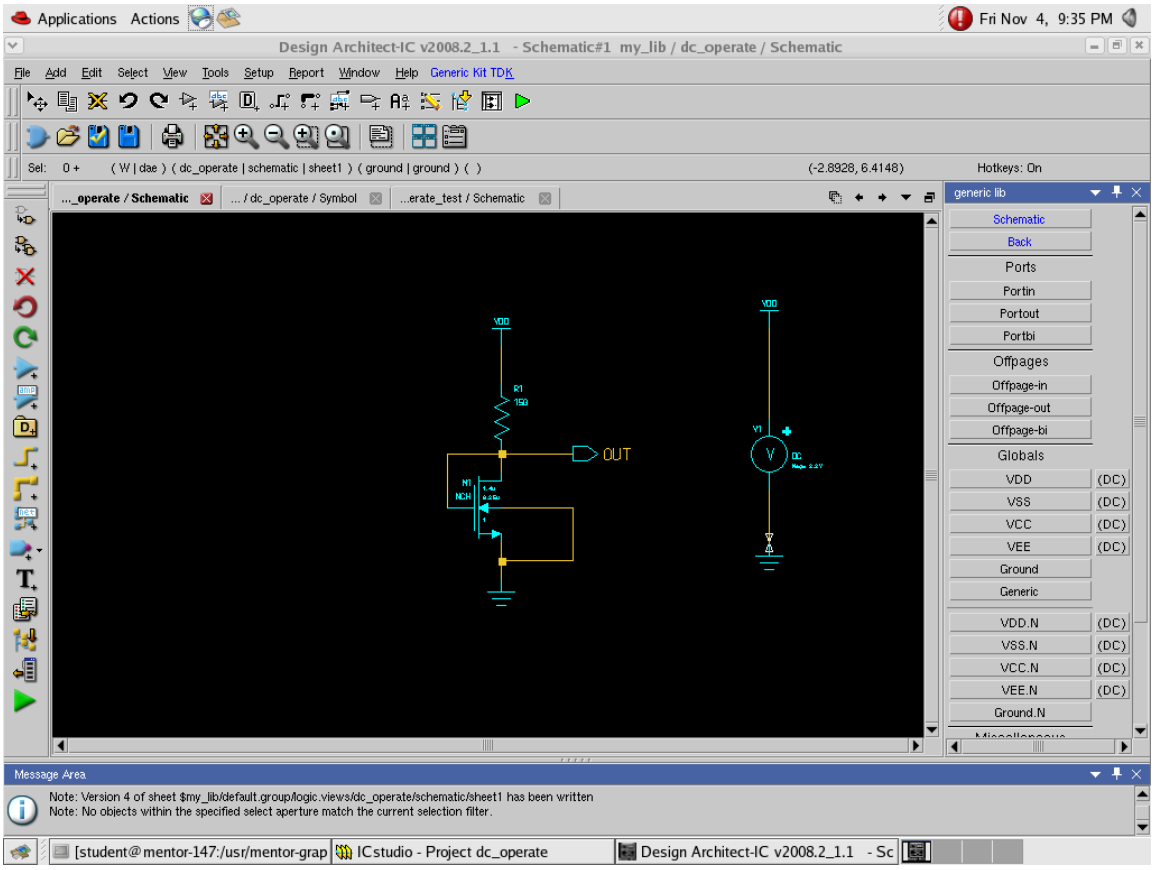


Design Architect (DA-IC) will open automatically where in you can capture the required cell design.

Schematic Entry:

- Select the parts for your schematic of the current source by choosing from a library of components.
  To place the transistor on the sheet:
- In the palette on RHS click on **Add Device** and in select **nmos**.
- In the palette menu shown alongside, click on **Library**
- In the subsequent palette menu click on **Device Lib.**
- Select **ideal resistor** and place it on the sheet by clicking on the position you wish to place it. Click **BACK** to go to the IC Library palette and click on **Generic Lib.** Place **VDD, PORTOUT and Ground** on the sheet.

- Add a DC source by selecting **IC Library >Sources Library > DC.** Highlight the DC Source, right click mouse, go to **Properties > Edit** to modify the voltage value of the source from 1V to 3.3V.
- From the **Schematic Edit Palette** select wire and wire the components as per the schematic shown below.
- Change the label **NET** of the **PORTOUT** symbol to **OUT**: Place cursor on **NET**, right click it then go to **Properties**. A display menu appears .Type **OUT** in the **Value** and click **OK**.
- To change the value of resistance place cursor on resistor, right click then go to P**roperties**. A display menu appears, in it change the **value** to 150 and click **OK**.
- Click **Check & Save** from the **Schematic Edit Palette** or in the **Menu Bar** to check and save your sheet.
- Now click the simulation button.



Setting up the Simulation Parameters:

Perform the simulation setup (all the ten steps) as explained in lab and view the dc operating points.

RESULT:

Attach the printout of the results i-e DC operating point of MOSFET operating in saturation region.

Lab No.4

OBJECTIVE:

To determine the behavior of MOS transistor using Mentor Graphics by analyzing its

- I_D v/s V_{DS} curve
- I_D v/s V_{GS} curve

EQUIPMENT REQUIRED:

Linux and Mentor Graphics (IC Studio) installed PC

THEORY:

The physical operation of a MOSFET can be divided into three regions of operation. For small value of V_G the transistor is switched off. For an NMOS transistoras V_{GS} increases from zero, holes in the p-substrate under the gate are repelled. Thus a depletion region is created from drain to source. For a sufficient value of interface potential, electron from source can actually travel through interface to drain terminal. The value of interface potential at this stage is called "Threshold Voltage" (V_t).

When $V_{GS}>V_t$ and $V_{DS}<(V_{GS}-V_t)$: Triode of Linear Region

In this region of operation MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages. The current from drain to source is modeled as:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_t)V_{DS} - \frac{V_{DS^2}}{2}\right]$$

whereμ_n is the charge-carrier effective mobility, W is the gate width, L is the gate length and C_{ox} is the gate oxide capacitance per unit area.

When $V_{GS}>V_t$ and $V_{DS}>(V_{GS}-V_t)$: Saturation Region

The switch is turned on, and a channel has been created, which allows current to flow between the drain and source. Since the drain voltage is higher than the gate voltage, the electrons spread out, and conduction is not through a narrow channel but through a broader, two- or three-dimensional current distribution extending away from the interface and deeper in the substrate. The onset of this region is also known as **pinch-off** to indicate the lack of channel region near the drain. The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate–source voltage, and modeled very approximately as:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$$

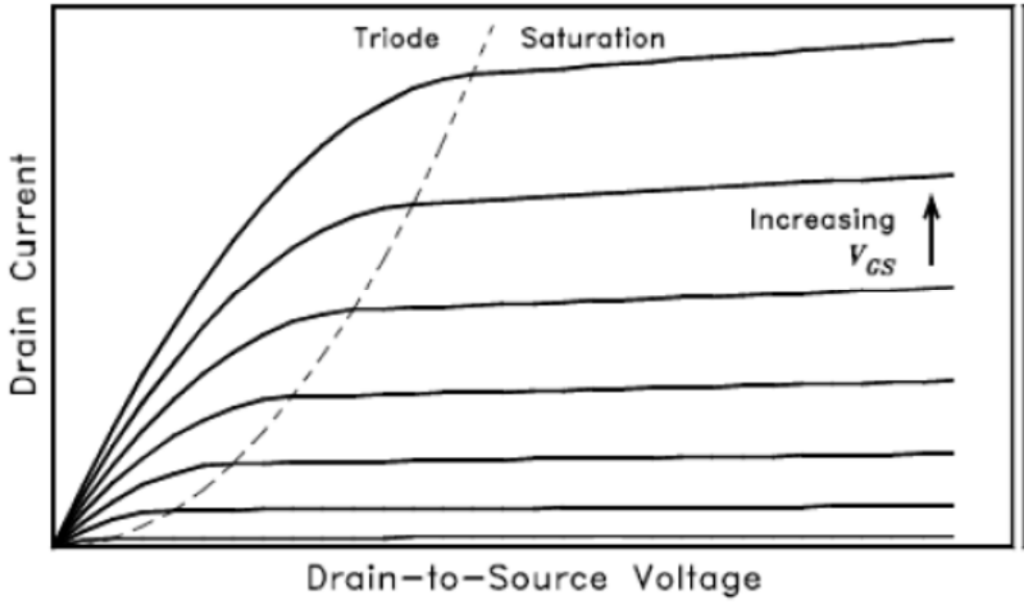


Figure 1:I_D v/s V_{DS} curve for different values of V_{GS}

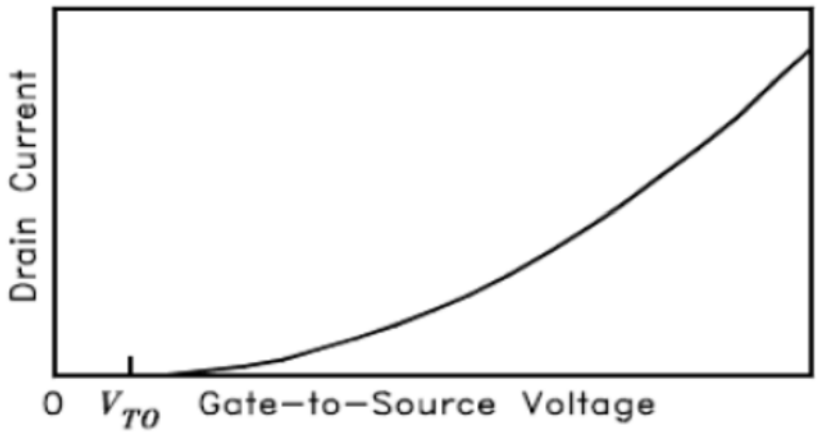


Figure 2:I_D v/s V_{GS}curve

The characteristic curve of Fig. 1 indicates three regions of operation. The cutoff region, the triode region and the saturation region. The device is cutoff when $V_{GS}<V_t$ whereas it follows a linear relationship in triode region. The MOS operation, therefore, can be modeled as a linear resistor in triode region. Saturation region on the other hand is used when MOS is employed as an amplifier. In saturation region MOS provides a drain current which is independent of V_{DS} and is determined by V_{GS} according to a square law relationship. Thus Fig. 2 shows MOSFET operation as an ideal current source whose value is controlled by V_{GS}.

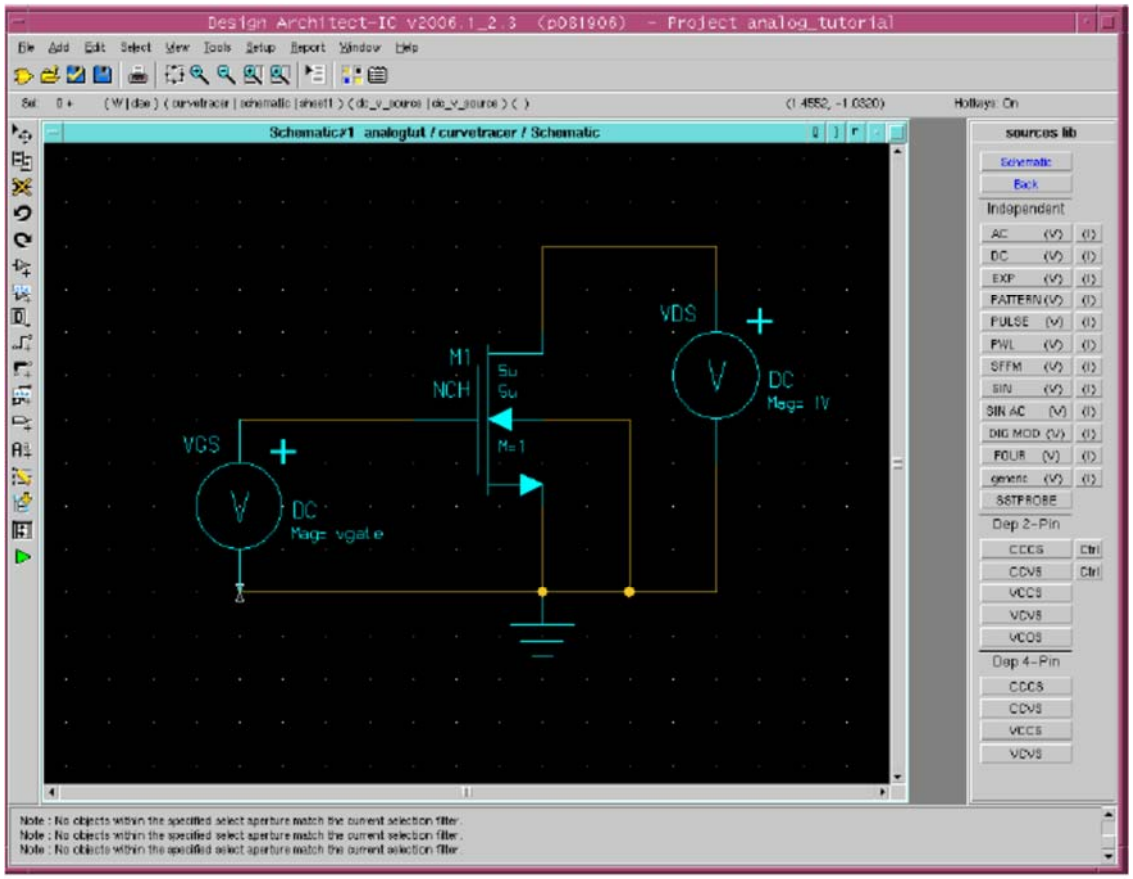
PROCEDURE:

Launch IC Studio on Linux as explained in Lab Session 1.

Capturing a Cell and Schematic Entry:

For I_D v/s V_{DS}curve:

Draw the following schematic by following the steps given in Lab Session 2.



- In the circuit set the Instantaneous Value of source connected between gate and source as vgs and its dc value as vgate.
- Similarly set the instantaneous value of dc source connected between drain and source as vds and its dc value will be by default 1V.

Setting up the Simulation Parameters:

- Now perform step 1 to 4 of lab 2.
- Set the **Setup Analysis** as **DC** and then sweep vds,

Defining Parameters:

- Select Setup Outputs and goto
  Parameter Sweeps
  In **Parameter Type** select **Global**
  Set **Parameter** as vgate and its value 0
  Select **Range** type as **linear** and specify the range of vgate.
  Add these parameters.
- Now perform steps 6, 7, 8 and 9 from lab 2.

Viewing the Results using EZWave Viewer:

- Under *(name of schematic)* open the List tab then drag the drain current to the waveform window.

I_D v/s V_{GS} curve:

Now implement changes in the schematic and simulation setup required. Also mention all the steps.

RESULT:

Attach the printout of the results i-e

- I_D v/s V_{DS} curve
- I_D v/s V_{GS} curve

Lab No.5

OBJECTIVE:

To determine the behavior of a Common Source Amplifier circuit using Mentor Graphics.

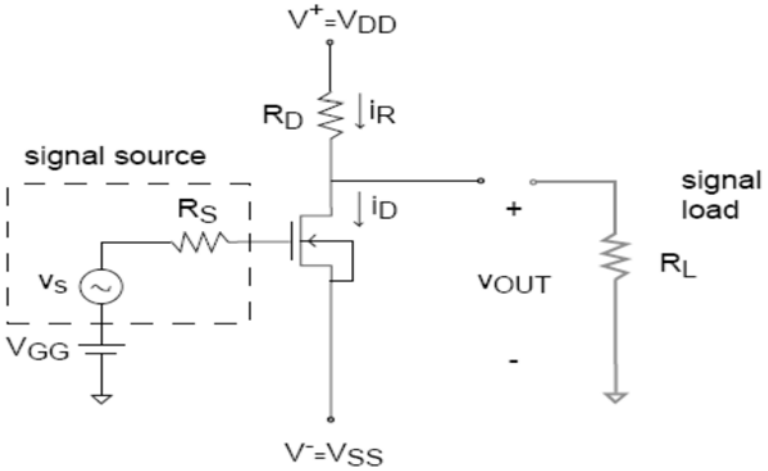
EQUIPMENT REQUIRED:

Linux and Mentor Graphics (IC Studio) installed PC

THEORY:

A common-source amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a voltage or transconductance amplifier. The easiest way to tell if a FET is common source, common drain, or common gate is to examine where the signal enters and leaves. The remaining terminal is what is known as "common". In this example, the signal enters the gate, and exits the drain. The only terminal remaining is the source. This is a common-source FET circuit. The analogous bipolar junction transistor circuit is the common-emitter amplifier.

The common-source (CS) amplifier may be viewed as a transconductance amplifier or as a voltage amplifier. As a transconductance amplifier, the input voltage is seen as modulating the current going to the load. As a voltage amplifier, input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance according to Ohm's law. However, the FET device's output resistance typically is not high enough for a reasonable transconductance amplifier (ideally infinite), nor low enough for a decent voltage amplifier (ideally zero). Another major drawback is the amplifier's limited high-frequency response. Therefore, in practice the output often is routed through either a voltage follower (common-drain or CD stage), or a current follower (common-gate or CG stage), to obtain more favorable output and frequency characteristics. The CS–CG combination is called a cascode amplifier.



PROCEDURE:

Launch IC Studio on Linux as explained in Lab Session 1.

Capturing a Cell and Schematic Entry:

Draw the schematic by following the steps given in Lab Session 2.

Select the drain current and gate to source voltage from the id-vds curve in lab 3, and then calculate the value of drain resistance.

Setting up the Simulation Parameters:

- Now perform step 1 to 4 of lab 2.
- Set the **Setup Analysis** as **Transient** and click on **setup** associated with it.
  In the **Setup** box that appears type **10m** in the **stop field** and **100n** in **Max time step** field .then click **OK.**
- Set the **Setup Outputs** as **Transient**.
- Perform steps 7, 8 and 9 as in lab 2.

Set up the simulation parameters as explained in lab and view waveform in EZ viewer.

CALCULATION:

The gain of the amplifier is:

RESULT:

Attach the printout of input and output waveform along with their peak-to-peak voltage measurement.

Lab No.6

OBJECTIVE:

Design and simulate simple MOS current mirror and current amplifier using Mentor Graphics.

EQUIPMENT REQUIRED:

Linux and Mentor Graphics (IC Studio) installed PC

THEORY:

Current Mirrors are fundamental building blocks of Analog Integrated Circuits. Operational amplifiers, operational transconductance amplifiers and biasing networks are examples of circuits that are composed of current mirrors. Analog integrated circuit implementation techniques such as current mode and switched current use current mirrors as the basic circuit element .Thedesign and layout of current mirrors is therefore an important aspect of successful analog circuit design.

In the simplest form a current mirror is composed of two transistors as shown in Fig.1. Transistor M1 is diode connected transistor and acts as a low impedance input of the current mirror .the drain of M2 is the output of current mirror.

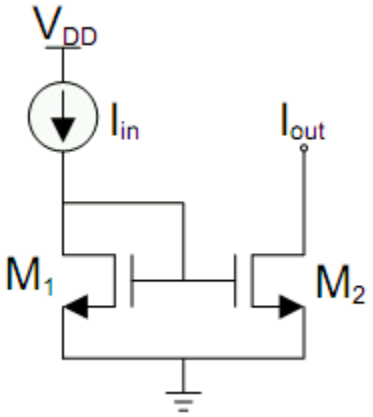


Figure 1: Simple current mirror

Since the gate to source voltage is the same for both the transistors then according to the first order MOSFET model, the drain currents will be equal .This assumes that the transistor sizes are equal as well as the process parameters.

A current mirror is used to mirror the input current into the output branch .A current (I_{in}) entering the diode connected the transistor establishes a gate voltage (V_{GS}).The gate voltage causes I_{out} to

low through the output transistor.

If the ratio of the transistors is changed, then the current mirror acts as a current amplifier. The gain of the amplifier is given by:

$$A_i = \frac{\left(W_2/L_2\right)}{\left(W_1/L_1\right)}$$

The above analysis assumed ideal operation of the current mirrors meaning that the drain currents are independent of V_{DS}; however, due to channel length we know this is not true. The following equation represents the dependence of drain current on V_{DS}.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$$

The excess current due to the differences in V_{DS1} and V_{DS2} will cause a difference in I_{D1} and I_{D2} . To reduce "lambda" effects, the drain to source voltages of the two transistors need to be kept equal.

PROCEDURE:

Launch IC Studio on Linux as explained in Lab Session 1.

Capturing a Cell and Schematic Entry:

Implement the circuit of MOS Current Mirror, MOS Amplifier and Cascode Current Mirror

Setting up the Simulation Parameters:

- Perform the steps given in lab 2 and determine the dc operating points of MOS Current Mirror, MOS Amplifier and Cascode Current Mirror.
- Also calculate the percentage difference in the output and input current in all the three cases.

Calculations:

Simple current mirror:

Iref	Io

% error:

Current Amplifier:

Iref	Io

% error:

RESULT:

Attach the printout of

1) Simple MOS current mirror
2) MOS Amplifier

Lab No.7

OBJECTIVE:

Design and simulate cascade current mirror using Mentor Graphics.

EQUIPMENT REQUIRED:

Linux and Mentor Graphics (IC Studio) installed PC.

]THEORY:

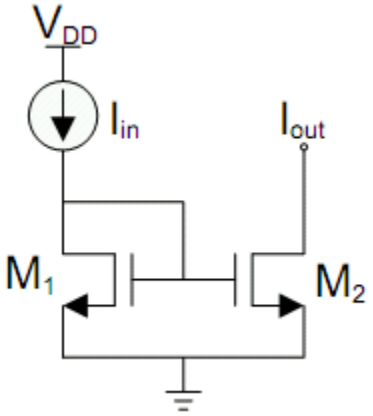


Figure 1: Simple current mirror

$$A_i = \frac{\left(W_2/L_2\right)}{\left(W_1/L_1\right)}$$

The above figure shows a simple current mirror .these current mirrors have non ideal effect that is having limited range of V_{DS2}.Since M1 remains in saturation for all input currents due to its diode connected configuration, M2 needs to be kept in saturation to assume proper operation .If V_{DS2} drops too low, M2 will enter the triode region, and the output current will be much less than what is wanted. The minimum output voltage for the current mirror is sometimes referred to as the compliance voltage .For the simple current mirror, the compliance voltage is $V_{DS\ sat2}$.

Hence to obtain good matching between input and output currents, the drain to source voltages of M1 and M2 must be kept equal .One way to achieve this is by using a cascode current mirror which is as given in figure 2.

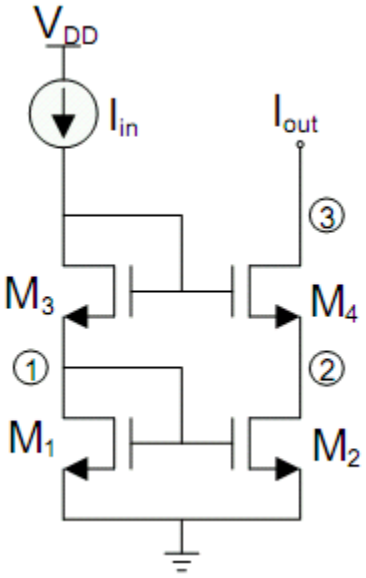


Figure 2: Cascode Current Mirror

Transistors M1 and M2 determine the ratio of the input and output currents. M3 biases M4 which is used to control the drain voltage of M2. If designed correctly ,V_{DS1} is approximately equal to V_{DS2} .The benefits of the cascade current mirror are better matching of output currents and larger output resistance .The disadvantage is that a larger compliance voltage is needed to keep both M3 and M4 in saturation. The compliance voltage of Figure 2 is given by:

Node 1: The voltage here is $V_{GS1} = V_T + V_{DSSat1}$.
Node 2: For good matching between input and output currents, we want V_{DS1} and V_{DS2} to be equal .thus, the voltage at node 2 is also $V_T + V_{DSsat1}$.
Node 3: The minimum compliant voltage will be the minimum voltage to keep M3 and M4 is saturation .This will be $V_T + V_{DSsat}1 + V_{DSsat2}$.

As you can see, adding the cascode transistor does not just increase the required compliance voltage by one V_{DSsat}, it also increases it by a threshold voltage

PROCEDURE:

Launch IC Studio on Linux as explained in Lab Session 1.

Capturing a Cell and Schematic Entry:

Implement the circuit of MOS Current Mirror, MOS Amplifier and Cascode Current Mirror

Setting up the Simulation Parameters:

- Perform the steps given in lab 2 and determine the dc operating points Cascode Current Mirror.
- Also calculate the percentage difference in the output and input current in all the three cases.

Calculations:

Cascode Current Mirror:

Iref	Io

% error:

RESULT:

Attach the printout of Cascode Current Mirror

Lab No. 8

OBJECTIVE:

To study different designs of constant current sources

This lab is designed to familiarize the student with the operation of two different designs of constant current sources. In particular, the operation of a simple BJT current source will be explored as well as the one of the so-called Wilson current mirror.TheWilson mirror is an improved current source circuit with a more stable output resistance.

The laboratory experiment is divided into TWO activities:

(A)The first activity involves the operation of a simple 2-BJT current-mirror constant current source.

(B)The second activity involves the operation of an improved 3-BJT constant current source (Wilson current mirror) that exhibits a more stable output resistance.

EQUIPMENT REQUIRED:

Protoboard
Function Generator
Digital Multimeter
Power Supply
Resistors:1 x 10 kΩ, 1 x 470 Ω, 2 x 1kΩ,
Transistors: 3 x 2N3904,

THEORY:

THE BASIC BJT CURRENT SOURCE:

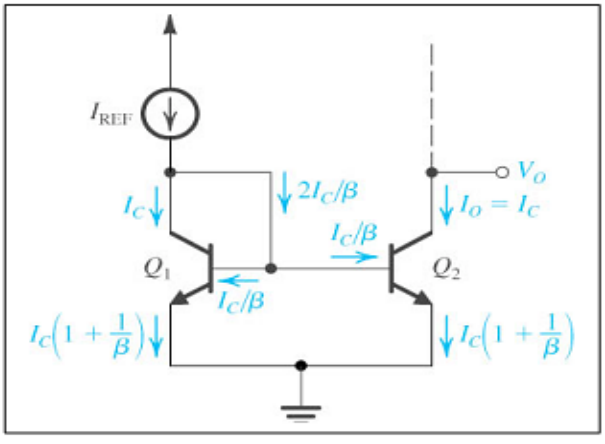


Fig 1: Analysis of the current mirror taking into account the effect of finite β

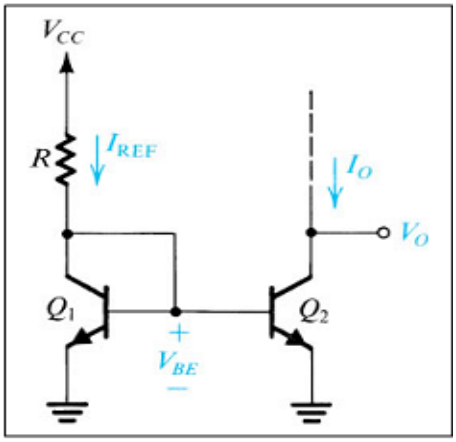


Fig 2: A Simple BJT current source

The basic BJT current mirror is shown in Fig.6.9.Let us consider the case when β is sufficiently high so that we can neglect the base currents. The reference current I_{REF} is passed through the diode-connected transistor Q_1 and thus establishes a corresponding voltage V_{BE}which in turn is applied between base and emitter of Q_2. Now, if Q_2 is matched to Q_1 or more specifically, if the EBJ area of Q_2 is the same as that of Q_1, and thus Q_2 has the same scale current I_S *as* Q_1, then the collector current of Q_2will be equal to that of Q_1, that is, $I_O=I_{REF}$.For this to happen, however, Q_2 must be operating in the active mode, which in turn is achieved so long as the collector voltage V_O is 0.3V higher than that of the emitter. To obtain a current transfer ratio other than unity, say m, we simply arrange that the area of the EBJ of Q_2 is m times that of Q_1.In this case, $I_O=mI_{REF}$.

Next we consider the effect of finite transistor β on the current transfer ratio. The analysis for the case in which the current transfer ratio is nominally unity -that is, for the case in which Q_2 is matched to Q_1-is illustrated in Fig. 1**.** The key point here is that since $Q_1$and Q_2 are matched and have the same V_{BE} their collector currents will be equal. The rest of the analysis is straight forward. A node equation at the collector of Q_1 yields

$$I_{REF} = I_C + \frac{2I_C}{\beta} = I_C\left(1+\frac{2}{\beta}\right)$$

Finally, since $I_O=I_C$ the current transfer ratio can be found as

$$\frac{I_O}{I_{REF}} = \frac{I_C}{I_C\left(1+\frac{2}{\beta}\right)} = \frac{1}{1+\frac{2}{\beta}}$$

Note that as β approaches ∞, I_o/I_{REF} approaches the nominal value of unity. For typical values of β, however, the error in the current transfer ratio can be significant. For instance, β= 100 results in a 2% error in the current transfer ratio.

The BJT mirror his a finite output resistance R_O

$$R_O = \frac{\Delta V_O}{\Delta I_O} = r_{O2} = \frac{V_A}{I_O}$$

Where V_A, and r_{O2} are the Early voltage and the output resistance, respectively. of Q_2Thus, even if we neglect the error due to finite β, the output current I_O will be at its nominal value only when Q_2 has the same V_{CE} as $_{Q1}$,namely at $V_O = V_{BE}$.As V_O is increased, I_O will correspondingly increase. Taking both the finite β and the finite R_O into account we can express the output current of a BJT mirror (with m=1) as

$$I_O = \frac{I_{REF}}{1+\frac{2}{\beta}}\left(1+\frac{V_O - V_{BE}}{V_A}\right)$$

Finally, if the current I_{REF} is taken in a simple manner as in Fig. 2 above, then

$$I_{REF} = \frac{V_{CC} - V_{BE}}{R}$$

THE WILSON CURRENT MIRROR :

At the cost of adding one more transistor an improved current mirror results, which exhibits both reduced dependence of the transfer ratio on β as well as increased output resistance. The drawback, in addition to the cost of an extra device, is that an additional V_{BE} drop is required for its operation so that one must allow for about 1 V across the Wilson-mirror output. The analysis is shown below right on the figure (Fig. 3) and results in an output resistance of $R_o = \beta r_o/2$ (for β=100, 50 times as much as with the simple mirror) and a transfer ratio

$$\frac{I_O}{I_{REF}} = \frac{1}{1+\frac{2}{\beta(\beta+2)}} \approx \frac{1}{1+\frac{2}{\beta^2}}$$

So that with β=100 the ratio is 0.9998 or the error is 0.02% instead of 2%

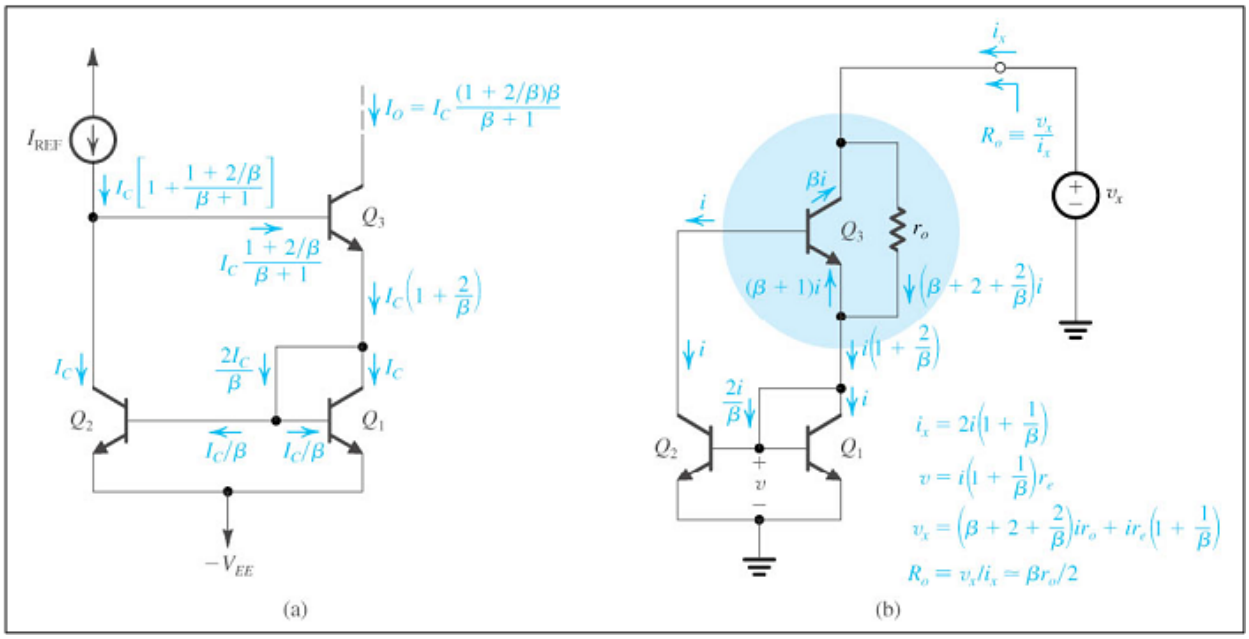


Fig 3: The Wilson bipolar current mirror :(a)circuit showing analysis to determine the current transfer ratio; and (b)determining the output resistance. Note that the current i_X that enters $Q3$ must equal the sum of the currents that leave it, $2i$.

PRELAB ASSIGNMENT:

Use the computer software tool OrCAD PSPICE to simulate the two lab activities. Make sure to bring the PSPICE results to the laboratory .In addition to being an aid in immediately verifying measured results ,**they will be the basis of your Prelab grade for this lab.**

- Specifically, the Circuit drawings with the nodes labeled and with DC node voltages **and all branch currents**

  Fill in all entries in the tables provided below that are labeled "calculated".

PROCEDURE:

LABORATORY ACTIVITIES:

ACTIVITY 6.A: SIMPLE CURRENT SOURCE

There will be two parts to this activity, each with a different resistance value for R_L.

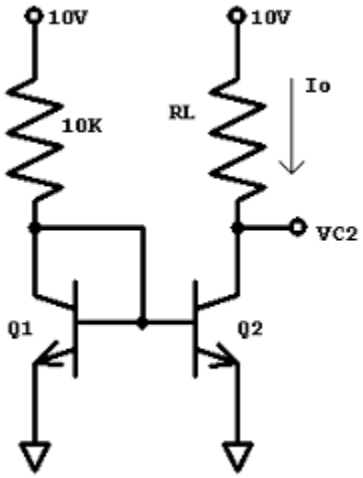


Fig 4: Simple current source .The transistors are 2N3904

- **6.A.a** Build the circuit given in figure 4 with R_L=0 Ω.

(i) Using a DC ammeter, measure and record the DC branch currents for each resistor. Note: Due to self heating, the circuit will take around 30 seconds to settle.

Activity A. Part a: R_L = 0 Ω DC Currents

	I_{calc} mA	I_{meas} mA	% error
I_i (10K)			
I_o (RL)			

(ii) Calculate the output resistance, R_O,of the current source using the equation

$$R_o = r_o = \frac{V_A}{I_{CQ}} \quad \text{where } V_A = 100 \text{ V}.$$

$R_o = r_o =$

- **6.A.b** Build the circuit given in the above figure with R_L= 1kΩ.

(i) Using a DC ammeter, measure and record the DC branch currents for each resistor. Note: Due to self heating, the circuit will take around 30 seconds to settle.

Activity A. Part b:R_L=1kΩ DC Currents

	I_{calc} mA	I_{meas} mA	% error
I_i (10K)			
I_o (RL)			

(ii) Calculate the output resistance, R_O,of the current source using the equation

$$R_o = r_o = \frac{V_A}{I_{CQ}} \quad \text{where } V_A = 100 \text{ V}.$$

$R_o = r_o =$

(iii) Using the two operating points, one with R_L =0Ω and one with R_L =1kΩ, determine the *actual* value of the output resistance and *actual* value of V_A.

Activity 6.B: WILSON CURRENT MIRROR CIRCUIT:

In this activity, a Wilson current mirror will be studied. There will be two parts of this activity with different resistance values for R_L in each part , similar to Activity A. However, the values are not the same as in Activity A.

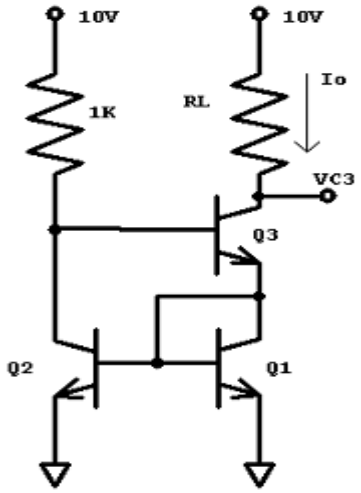


Fig 5: Wilson Current Mirror, The transistors are 2N3904

- **6.B.a** Build the circuit given in figure 5 with R_L=0 Ω.

(i) Using a DC ammeter, measure and record the DC branch currents for each resistor.
Note: Due to self heating, the circuit will take around 30 seconds to settle.

Activity B. Part a : R_L= 0 Ω

	I_{calc} mA	I_{meas} mA	% error
I_i (1K)			
I_o (RL)			

(ii) Calculate the output resistance, R_O,of the current source using the equation

$$R_o = r_o\left(\frac{\beta}{2}\right) \text{ where } V_A = 100 \text{ V}, \beta = 150, \text{ and } r_o = \frac{V_A}{I_{CQ}}.$$

- **6.B. b** Build the circuit given in the above figure with R_L=470 Ω.

(i) Using a DC ammeter, measure and record the DC branch currents for each resistor.
Note: Due to self heating, the circuit will take around 30 seconds to settle.

Activity B . Part b : R_L= 470 Ω

	I_{calc} mA	I_{meas} mA	% error
I_i (1K)			
I_o (RL)			

(ii) Calculate the output resistance, R_O,of the current source using the equation

$$R_o = r_o\left(\frac{\beta}{2}\right) \text{ where } V_A = 100 \text{ V}, \beta = 150, \text{ and } r_o = \frac{V_A}{I_{CQ}}.$$

(iii) Using the two operating points, one with R_L =0Ω and one with R_L =470Ω, determine the *actual* value of the output resistance and *actual* value of V_A.

CALCULATOIONS:

Show all the calculations

RESULTS:

BASIC BJT CURRENT SOURCE:

$R_o = r_o$(for R_L =0) =

$R_o = r_o$ (for R_L =1k Ω) =

Actual Value of R_o =

Actual Value of V_A =

WILSON CURRENT MIRROR:

$R_o = r_o$ (for R_L =0) =

$R_o = r_o$ (for R_L =470 Ω) =

Actual Value of R_o =

Actual Value of V_A =

Lab No. 9

OBJECTIVE:

To analyze the frequency response of Common Emitter Amplifier.

EQUIPMENT REQUIRED:

Protoboard
Function Generator
Digital Multimeter
Power Supply
Resistors
Transistors: 1 x 2N3904

THEORY:

COMMON EMITTER AMPLIFIER:

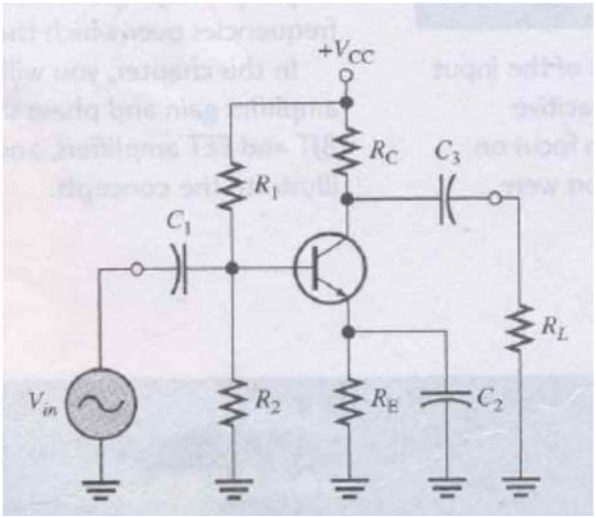


Fig1: Common Emitter Amplifier

A Common-Emitter amplifier is one of three basic single-stage bipolar-junction-transistor (BJT) amplifier topologies, typically used as a voltage amplifier. In this circuit the base terminal of the transistor serves as the input, the collector is the output, and the emitter is common to both (for example, it may be tied to ground reference or a power supply rail), hence its name. The analogous field-effect transistor circuit is the common-source amplifier.

EMITTER DEGENERATION RESISTANCE RE:

R_E introduces negative feedback in the amplifier circuit. If for instance the collector current increases, the emitter current will also increase resulting in an increased voltage drop across R_E. Thus the emitter voltage rises and the base-emitter voltage decreases .The latter effect causes the collector current to decrease, counteracting the initially assumed change, an indication of the presence of negative feedback.

TRANSISTOR CAPACITANCES:

C1 and C_3 are coupling capacitors while C_2 is bypass capacitor. There also exists internal capacitance between base and collector and base and base and emitter i-e C_{bc} and C_{be} respectively.

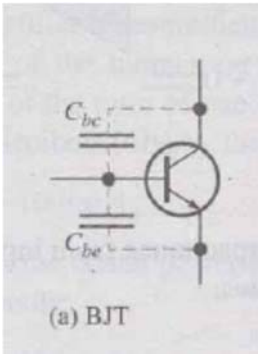


Fig 2: BJT Internal Capacitances C_{bc} and C_{be}

EFFECT OF COUPLING , BYPASS AND INTERNAL CAPACITANCES AT DC AND AT LOW FREQUENCIES:

Since $X_C=1/2\pi fC$,hence at low frequencies the reactance is greater and it decreases as the frequency increases. At low frequencies the reactance of coupling capacitance is high (The coupling and bypass capacitances are usually in microfarads) , hence they act as almost open circuit .Therefore at low frequencies the coupling capacitances act as nearly as open circuit

The bypass capacitance also acts as nearly open circuit at low frequency.

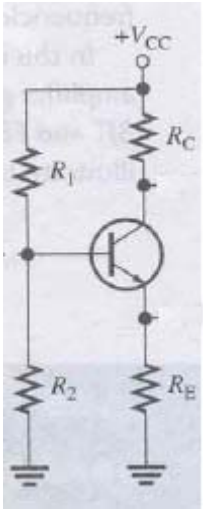


Fig 3: Common Emitter amplifier at DC

At lower frequencies, the internal capacitances C_{bc} and C_{be} have a very high reactance because of their low capacitance value (usually a few picofarads) and the low frequency value .Therefore they look like opens and have no effect on transistor's performance

AT MID RANGE FREQUENCY:

In mid range frequency the coupling and by-pass capacitance act as nearly short circuit. As the midrange frequency is also not much high and the internal transistor capacitances are also very small hence the internal transistor capacitances do not effect the transistor performance. Hence during mid range frequency the gain of the amplifier is maximum.

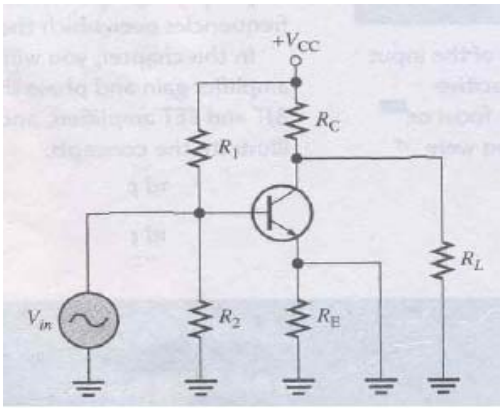


Fig 4: Common Emitter Amplifier at Mid-Range frequency

AT HIGH FREQUENCIES:

At high frequencies, the coupling and bypass capacitors become effective ac shorts and do not effect amplifier's response .The reactance of internal transistor junction capacitances, (C_{bc} and C_{be}) become small enough and a significant amount of signal voltage is lost due to the voltage divider effect of signal source resistance and the reactance of C_{be} as shown in figure .When the reactance of C_{bc} becomes small enough , a significant amount of output signal is fed back out of phase with the input (negative feedback) thus effectively reducing the voltage gain which is as illustrated in figure :

The effect of C_{bc} can be explained much clearly using Miller's theorem.

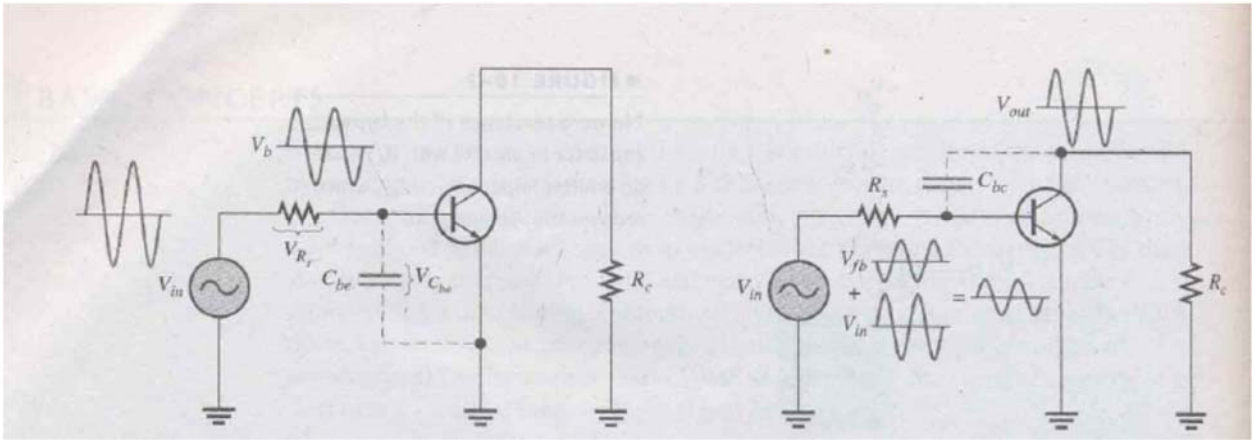


Fig 5a : Effect of C_{bc} where V_b is reduced by the voltage-divider action of R_3 and X_{Cbe}

Fig 5 b: Effect of C_{bc} , where part of V_{out} (V_{fb}) goes back through C_{bc} to the base and reduces the input signal because it is approximately 180^o out of phase with V_{in}

MILLER'S THEOREM IN HIGH-FREQUENCY ANALYSIS:

The capacitance C_{bc} in BJT between the input and output is shown in a generalized form in Fig 6 .A_V is the absolute voltage gain of the amplifier at midrange frequencies and C represents C_{bc}

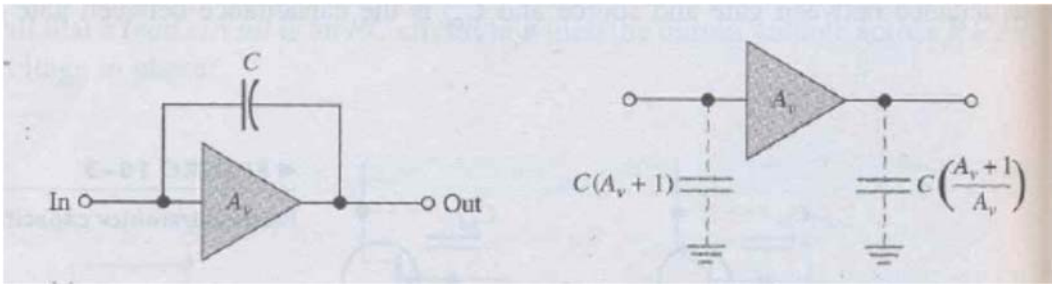


Fig 6: General case of Miller input and output capacitances.

Miller's theorem states that C effectively appears as a capacitance from input to ground

$$C_{\text{in (Miller)}} = C_{bc}\,(A_v + 1)$$

C_{bc} appears as a capacitance to ac ground, in parallel with $C_{\text{in (Miller)}}$

For e.g if C_{bc} = 6pF and the amplifier gain is 50 then $C_{\text{in (Miller)}}$= 306pF.

Miller's theorem also states that C effectively appears as a capacitance from output to ground

$$C_{out(Miller)} = C_{bc}\left(\frac{A_v + 1}{A_v}\right)$$

These two Miller capacitances create a high frequency input RC circuit and a high frequency output RC circuit which is as shown in figure:

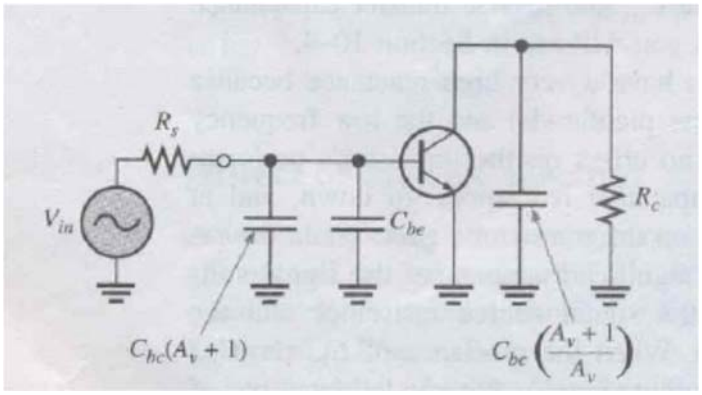
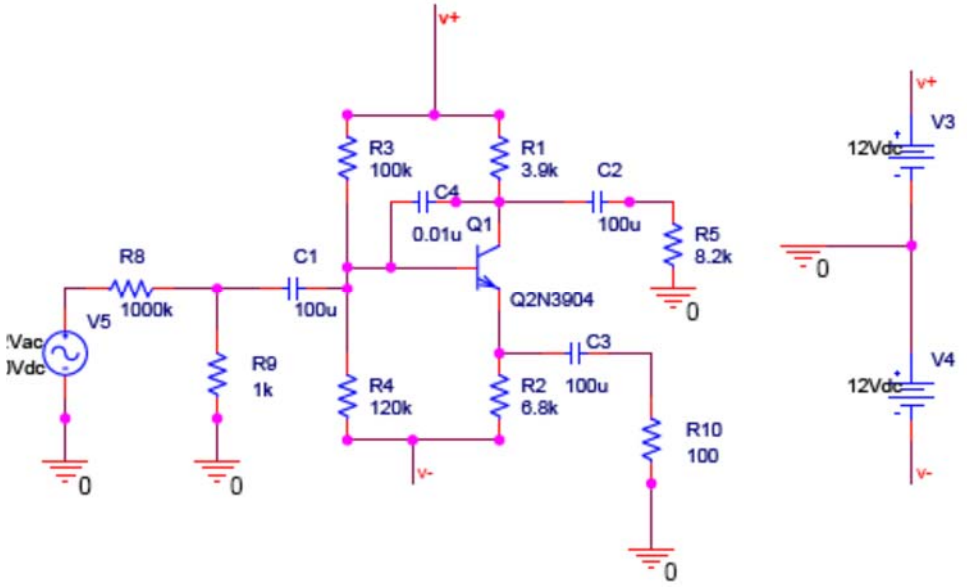


Fig 7: Amplifier ac equivalent circuits showing internal capacitances and effective Miller capacitances

PRELAB ASSIGNMENT:

The Common Emitter amplifier circuit that is to be simulated and implemented on bread board is as shown below:



Use the computer software tool OrCAD PSPICE to simulate the circuit. Make sure to bring the PSPICE results to the laboratory. In addition to being an aid in immediately verifying measured results, **they will be the basis of your Prelab grade for this lab**.

Specifically, the following items must be addressed using OrCAD PSPICE as part of the prelab assignment:

- Circuit drawings with the nodes labeled and with DC node voltages.
- Transient response (time-domain) with V_{in} = 2V, showing plots of Base voltage (input voltage) and voltage across load (output voltage) waveforms separately. Also mark label to the maximum output voltage (using pspice)
- AC Sweep/Noise response, showing waveform of output voltage Vs Frequency.

Fill in all entries in the tables provided below that are labeled "simulated".

DC PARAMETERS:

	Simulated	Measured	% error
V_B (Volts)			
V_C (Volts)			
V_E (Volts)			

TRANSIENT RESPONSE:

V_{in} (at base) :

Simulated	Measured	% error

V_{out} (across load)

Simulated	Measured	% error

Gain Calculated:

Simulated	Measured	% error

FREQUENCY RESPONSE:

Frequency	V_{out} (Simulated)	V_{out} (Measured)

Draw a plot of the output voltage Vs Frequency using semi log graph paper.

RESULT:

Phase Shift between input and output signal ----------.

The upper critical frequency as determined from the graph is ----------.

Lab No. 10

OBJECTIVE:

To analyze the frequency response of Cascode Amplifier and compare it with Common Emitter Amplifier.

EQUIPMENT REQUIRED:

Protoboard
Function Generator
Digital Multimeter
Power Supply
Resistors
Transistors: 2 x 2N3904

THEORY:

Cascode amplifier is about a compound structure that consists of a common emitter and a common base amplifier.

While the C-B (common-base) amplifier is known for wider bandwidth than the C-E (common-emitter) configuration, the low input impedance (10s of Ω) of C-B is a limitation for many applications. The solution is to precede the C-B stage by a low gain C-E stage which has moderately high input impedance (kΩs). The stages are in a cascode configuration, stacked in series, as opposed to cascaded for a standard amplifier chain. The cascode amplifier configuration has both wide bandwidth and moderately high input impedance.

The cascode amplifier preserves all the features of a common emitter amplifier as far as the voltage and current gains, the equivalent input resistance and the output resistance are concerned. Cascode amplifiers are designed to extent the frequency range of operation of common emitter amplifiers to higher frequencies. This performance is due to the presence of the common base amplifier.

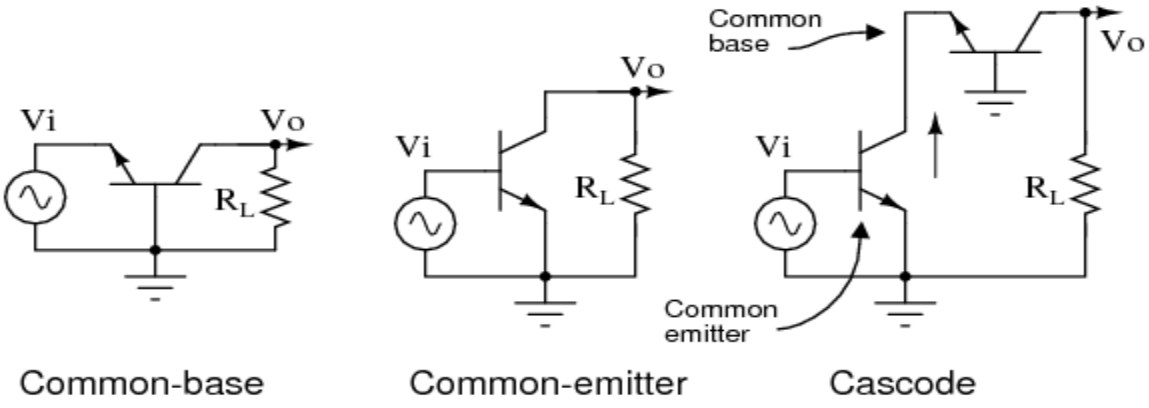


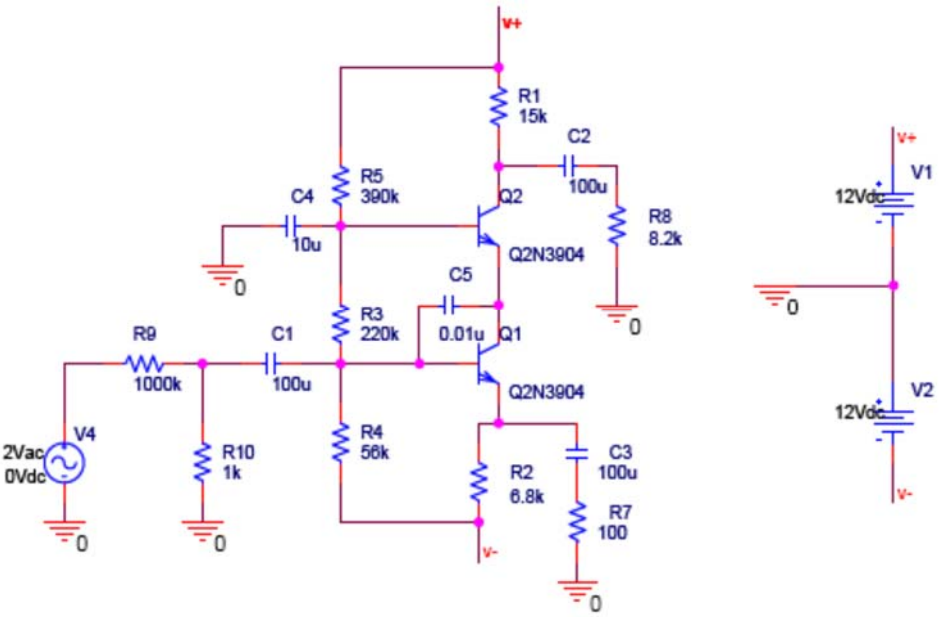
Fig 1: This is an AC circuit equivalent with batteries and capacitors replaced by short circuits.

A common-base configuration is not subject to the Miller effect because the grounded base shields the collector signal from being fed back to the emitter input. Thus, a C-B amplifier has better high frequency response.

To have moderately high input impedance, the C-E stage is still desirable.

PRELAB ASSIGNMENT:

The Cascode amplifier circuit that is to be simulated and implemented on bread board is as shown below:



Use the computer software tool OrCAD PSPICE to simulate the circuit. Make sure to bring the PSPICE results to the laboratory. In addition to being an aid in immediately verifying measured results, **they will be the basis of your Prelab grade for this lab**.

Specifically, the following items must be addressed using OrCAD PSPICE as part of the prelab assignment:

- Transient response (time-domain) with V_{in} = 2V, showing plots of Base voltage (input voltage) and voltage across load (output voltage) waveforms separately. Also mark label to the maximum output voltage (using pspice)
- AC Sweep/Noise response, showing waveform of output voltage Vs Frequency.

Fill in all entries in the tables provided below that are labeled "simulated".

TRANSIENT RESPONSE:

V_{in} (at base):

Simulated	Measured	% error

V_{out} (across load)

Simulated	Measured	% error

Gain Calculated:

Simulated	Measured	% error

FREQUENCY RESPONSE:

Frequency	V_{out} (Simulated)	V_{out} (Measured)

Draw a plot of the output voltage Vs Frequency using semi log graph paper.

Result:

Phase Shift between input and output signal ----------.

The upper critical frequency as determined from the graph is ----------.

As compared to CE amplifier the upper critical frequency of Cascode Amplifier is increased by ----------.

Lab No. 11

OBJECTIVE:

Design and analyze a Common Gate Amplifier circuit.

EQUIPMENT REQUIRED:

Protoboard
Function Generator
Digital Multimeter
Power Supply
Resistors
Transistors: 1 x 2N7000

THEORY:

BACKGROUND:

MOS transistor is a voltage controlled device, where gate voltage modulates the channel resistance and voltage between drain and source determines current flow between the drain and source terminals. Like BJT, MOS transistor can perform as amplifier and as electronic switch. MOS comes in two different flavors, as NMOS and as PMOS.

MOS AMPLIFIERS:

Three common MOS amplifiers are common source, common drain and common gate.

COMMON GATE AMPLIFIER:

As shown in figure 1 the common gate amplifier has a grounded gate terminal , a signal input at the source terminal and the output taken at the drain.

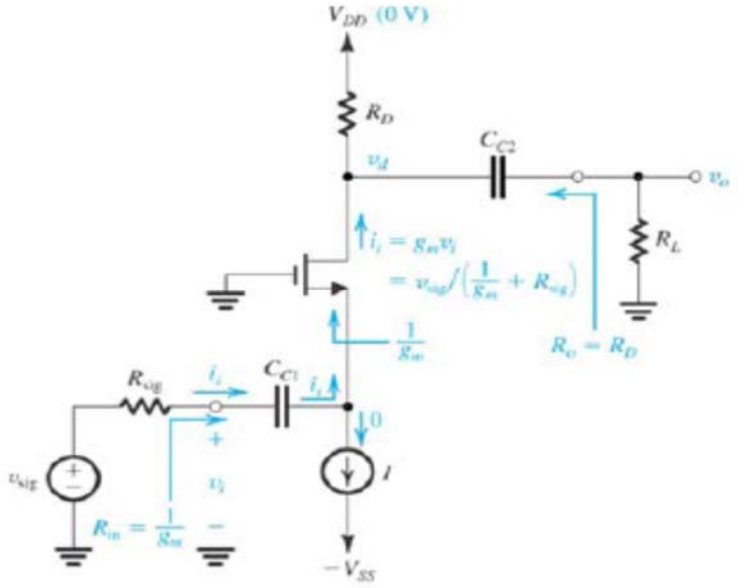


Fig 1: Common Gate Amplifier

Its input resistance is

$$R_{in} = \frac{1}{g_m}$$

And voltage gain is:

$$G_v = \frac{g_m R_D \| R_L}{1 + g_m R_{sig}}$$

Small Signal current gain:

$$G_i = \frac{R_D}{R_D + R_L}$$

Output Resistance:

$$R_{out} = R_D$$

Hence Common Gate amplifiers have

- Non-Inverting output
- Moderate input resistance
- Moderately large small signal voltage gain but smaller than common source amplifier.
- Small signal current gain less than one
- Potentially large output resistance (Dependent on R_D)

Design a common gate amplifier using 2N7000 transistor that meets the following specifications:
I_D= 10mA
V_{CC} =12V

PRELAB ASSIGNMENT:

Step1:
Determine the values of V_{GS} and g_m.
Use **OrCAD PSPICE** simulation to find V_{GS} required to yield the current . Plot I_DVs V_{GS} curve . Make sure to bring the PSPICE results to the laboratory. Take two points in the region near 10mA and determine gm in the small linear region.

Step 2:
Determine the value of R_D and R_S
Maximum and minimum voltage at the drain node of the amplifier can vary from V_{CC} (when I_D=0) to almost zero when voltage drop between drain and ground is very small.We want the AC signal to swing symetrically around the mid-point of the power supply (1/2 V_{CC})

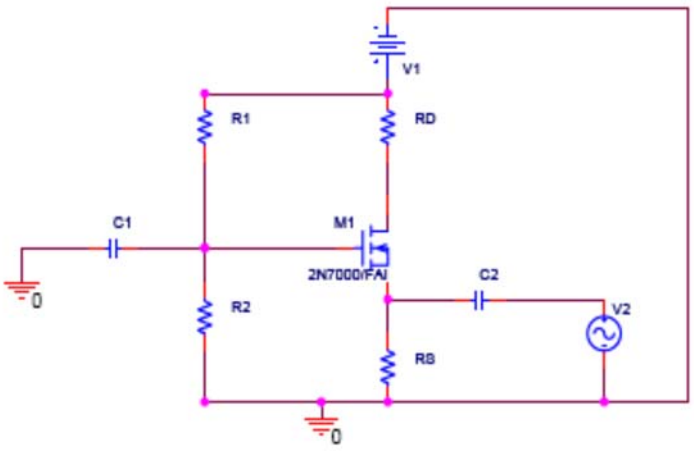
R_D= (V_{CC}-V_C)/I_D

Let R_S be 10% of R_D

Step 3:
With $V_G = V_S + V_{GS}$ (where V_{GS} is to be used at I_D = 10mA) .Select the value of R_1 and R_2 such that the voltage at the gate is as desired and the current through the resistance R_D is nearly 10mA and the drain current remains stable at the value calculated.

Step 4:
Use a 1u capacitor between gate and ground terminal and a 10u capacitor between the sin source and Rs.

The Common Gate amplifier circuit that is to be simulated and implemented on bread board is as shown below:



Use the computer software tool OrCAD PSPICE to simulate the circuit.
Make sure to bring the PSPICE results to the laboratory .In addition to being an aid in immediately verifying measured results,**they will be the basis of your Prelab grade for this lab**.

Specifically, the following items must be addressed using OrCAD PSPICE as part of the prelab assignment:

- Circuit drawings with the nodes labeled and with DC node voltages, and DC currents through all branches.
- Transient response (time-domain) with V_{in} = 10mV, showing plots of source voltage (input voltage) and drain voltage (output voltage) waveforms separately. Also mark label to the maximum output voltage (using pspice)

CALCULATIONS:

Show all the calculations for determining R_D, R_S, V_S, V_G, R_1 and R_2.

RESULT:

The gain of the common gate amplifier as determined by the circuit is: ----------

Lab No. 12

OBJECTIVE:

To demonstrate the properties of differential amplifiers in both common mode and differential mode.

EQUIPMENT REQUIRED:

Protoboard
Function Generator
Digital Multimeter
Power Supply
Resistors
Capacitors
Transistors: 4 x Q2N3904

THEORY:

BASIC OPERATION OF THE BJT DIFFERENTIAL PAIR

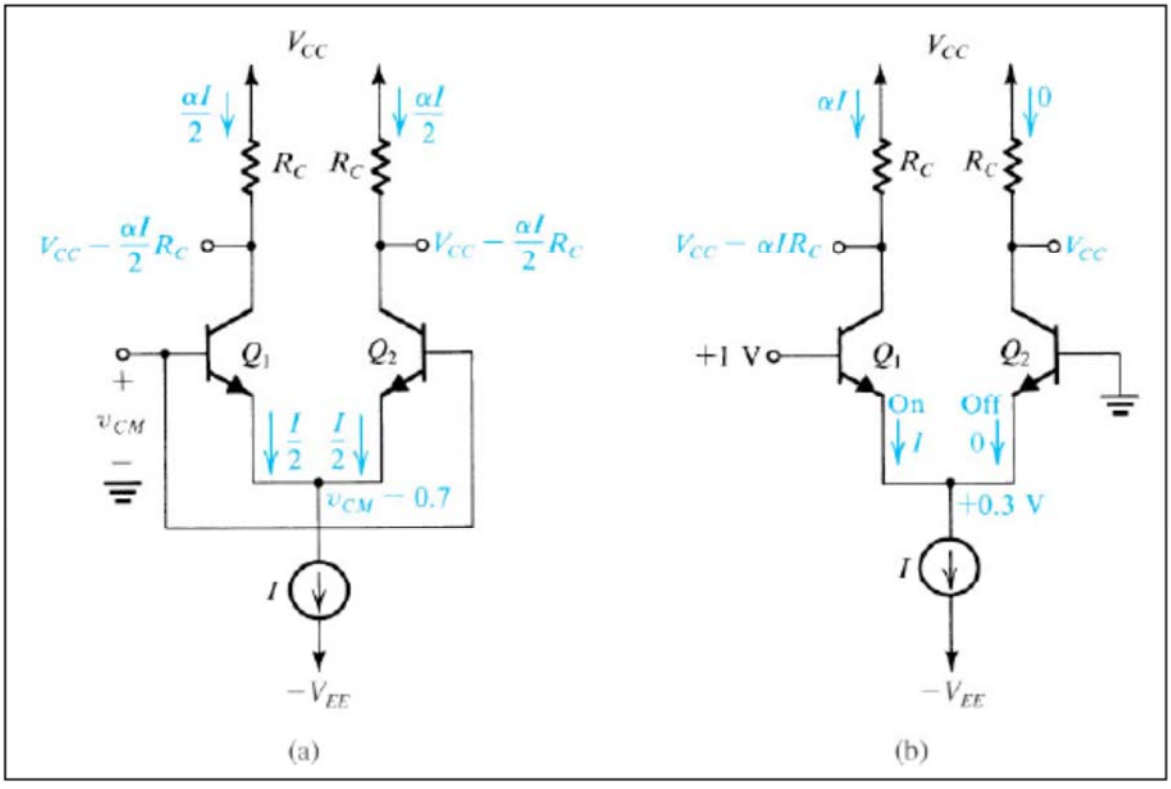


Fig 1 : Different modes of operation of the BJT differential pair: (a) The differential pair with a common-mode input signal v_{CM}. (b) The differential pair with a large differential input signal.

First consider the case of Figure 1a where the two bases are tied together. Then $v_{B1} = v_{B2} = v_{CM}$. If Q_1 and Q_2 are matched, and assuming an ideal bias current source I with infinite output resistance, it follows that the current *I* will remain constant and from symmetry that *I* will divide equally between Q_1 and Q_2. Thus $i_{E1} = i_{E2} = I/2$, and the voltage at the emitters will be v_{CM} -V_{BE} where V_{BE} is the base-emitter voltage (assumed to be approximately 0.7 V) corresponding to an emitter current of *I/2*. The voltage at each collector will be V_{CC}-1/2 αIR_C, and the difference in voltage between the two collectors will be zero.

Now let us vary the value of the common-mode input signal v_{CM}. Obviously, as long as Q_1 and Q_2 remain in the active region the current *I* will still divide equally between Q_1 and Q_2, and the voltages at the collectors will not change. Thus the ideal differential pair does not respond to (i.e., it rejects) common-mode input signals.

As another experiment, let the voltage v_{B2_2} be set to a constant value, say, zero (by grounding B_2), and let $v_{B2} = +1$ V (see Fig.1b). With a bit of reasoning, it can be seen that Q_1 will be on and conducting all of the current *I* and that Q_2 will be off. For Q_1 to be on (with $V_{BE1} = 0.7$ V) the emitter has to be at approximately +0.3 V, which keeps the EBJ of Q_2 reverse-biased. The collector voltages will be, $v_{C1} = V_{CC}$-αIR_C and $v_{C2} = V_{CC}$.

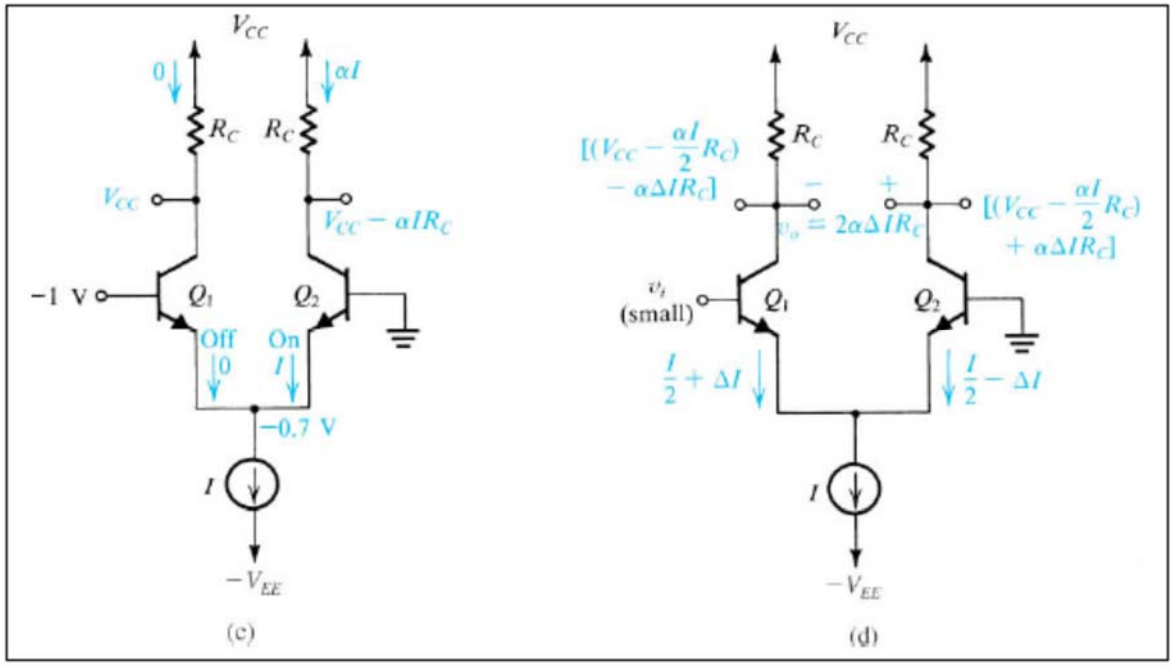


Fig 1 (Continued) (c) The differential pair with a large differential input signal of polarity opposite to that in (b) .(d) The differential pair with a small differential input signal v_i . Note that we have assumed the bias current source I to be ideal (i.e., it has an infinite output resistance) and thus I remains constant with the change in v_{CM}

Let us now change v_{B1} to -1 V (Fig.1c). Again with some reasoning it can be seen that Q_1 will turn off and Q_2 will carry all the current I. The common emitter will be at -0.7 V, which means that the EBJ of Q_1 will be reverse-biased by 0.3 V. The collector voltages will be $v_{C2} = V_{CC}-\alpha IR_C$ and $v_{C1} = V_{CC}$.

From the foregoing, we see that the differential pair certainly responds to large difference-mode (or differential) signals. In fact, with relatively small difference voltages we are able to steer the entire bias current from one side of the pair to the other.

To use the BJT differential pair as a linear amplifier we apply a very small differential signal (a few millivolts), which will result in one of the transistors conducting a current of $I/2 + \Delta I$: the current in the other transistor will be $I/2 + \Delta I$, with ΔI being proportional to the difference input voltage (see Fig. 1d). The output voltage taken between the two collectors will be $2\alpha\Delta IR_C$, which is proportional to the differential input signal v_i.

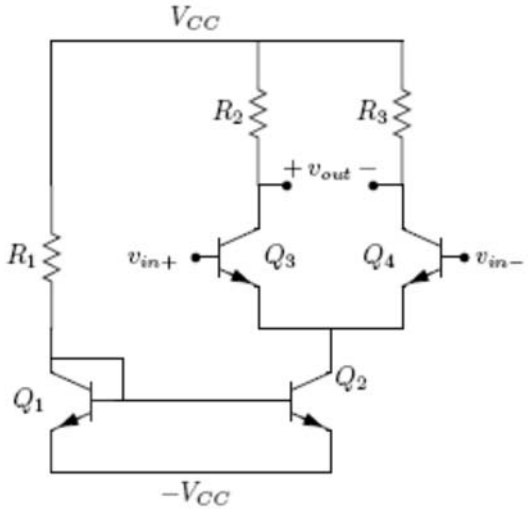
PROCEDURE:

LABORATORY ACTIVITIES:

Plot the i_c_v_{be} curve, and i_b_v_{be} curve. Let I_C = 1mA . At that point measure V_{BE} . Next simulate the i_b_v_{be} curve at V_{BE} and measure I_B . From here determine the β of the transistor at I_C = 1mA.

DIFFERNTIAL PAIR WITH RESISTIVE LOAD

With the inputs being grounded design a Differential amplifier circuit which is biased by a current source which has the collector voltage at Q_3 and Q_4 to be 5V. The collector currents of Q_3 and Q_4 to be 1mA. Calculate R_3 and R_2 for the two transistors .Determine the emitter current of Q_3 and Q_4. Determine the value of R_1 for the circuit so that the collector currents of Q_3 and Q_4 remain constant at nearly 1mA.



Fill the table below:

	V_{sim}	V_{meas}
V_{E1}, V_{E2}		
V_{B1}, V_{C1}, V_{B2}		
V_{C2}, V_{E3}, V_{E4}		
V_{B3}		
V_{B4}		
V_{C3}		
V_{C4}		

Transient response:

1) Apply a 30 mV amplitude,1kHz sine wave to v_{in+} and ground v_{in-} . Fill in the table below:

	V_{sim}	V_{meas}
v_{b3}		
v_{c3}		
v_{b4}		
v_{c4}		
Δv_{out}		

2) Apply a 100 mV amplitude,1kHz sine wave to v_{in+} and 90mV signal to v_{in-} . Fill in the table below:

	V_{sim}	V_{meas}
v_{b3}		
v_{c3}		
v_{b4}		
v_{c4}		
Δv_{out}		

RESULTS:

a) With the base of Q_3 and Q_4 grounded;
The differential gain of the circuit from simulation comes out to be: ----------
The differential gain of the circuit as measured comes out to be: ----------

b) By applying a 30 mV amplitude,1kHz sine wave to v_{in+} and ground v_{in-};
The differential gain of the circuit from simulation comes out to be: ----------
The differential gain of the circuit as measured comes out to be: ----------

c) By applying a 100 mV amplitude,1kHz sine wave to v_{in+} and 90mV signal to v_{in-};
The differential gain of the circuit from simulation comes out to be: ----------
The differential gain of the circuit as measured comes out to be: ----------

Lab No. 13

OBJECTIVE:
To measure the open loop gain and offset voltage of an op amp.

EQUIPMENT REQUIRED:
Protoboard
Function Generator
Digital Multimeter
Power Supply
Resistors
741 op-amp

THEORY:

Introduction
An operational amplifier, (or "op amp" as commonly known), has two inputs as shown in Figure

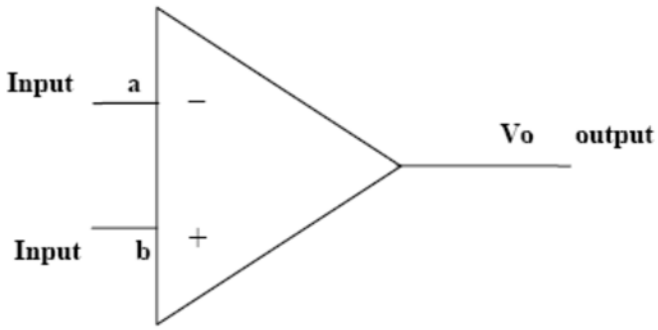


Fig.1

The output voltage Vo is proportional to the difference in voltage between the two inputs, and is given by:

$$V_o = G_v . (V_b - V_a)$$

where G_v is a large number, possibly as high as 1,000,000. Ideally, op amps should have: infinite input impedance zero currents flowing into the inputs zero output impedance.

However the characteristics of real op amps differ from the ideal. The key characteristics are:

The ***offset voltage*** -this is the voltage which when applied across the two inputs produces a zero voltage on the output

The ***bias and offset*** *currents* are currents flowing into the inputs I

The ***input impedance*** (usually high, but not infinite), and the *output impedance* (low but not zero).

The way in which the characteristics *change with frequency.*

OFFSET VOLTAGE :

This is the voltage which must be applied across the inputs to produce a zero voltage output. Generally with no input voltage the output is not zero, as expected with a perfect amplifier. This is because of slight differences, or asymmetries in the circuit. In other words the offset voltage is the voltage needed to counterbalance the small voltage normally present at the input.

The circuit used to measure the offset is shown in fig. . Vo is the unwanted output voltage, caused by Vi at the input.

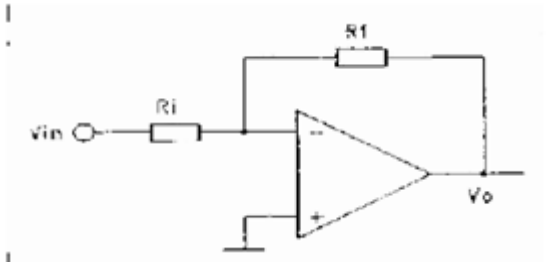


Fig. 2

Open Loop Gain Measurement

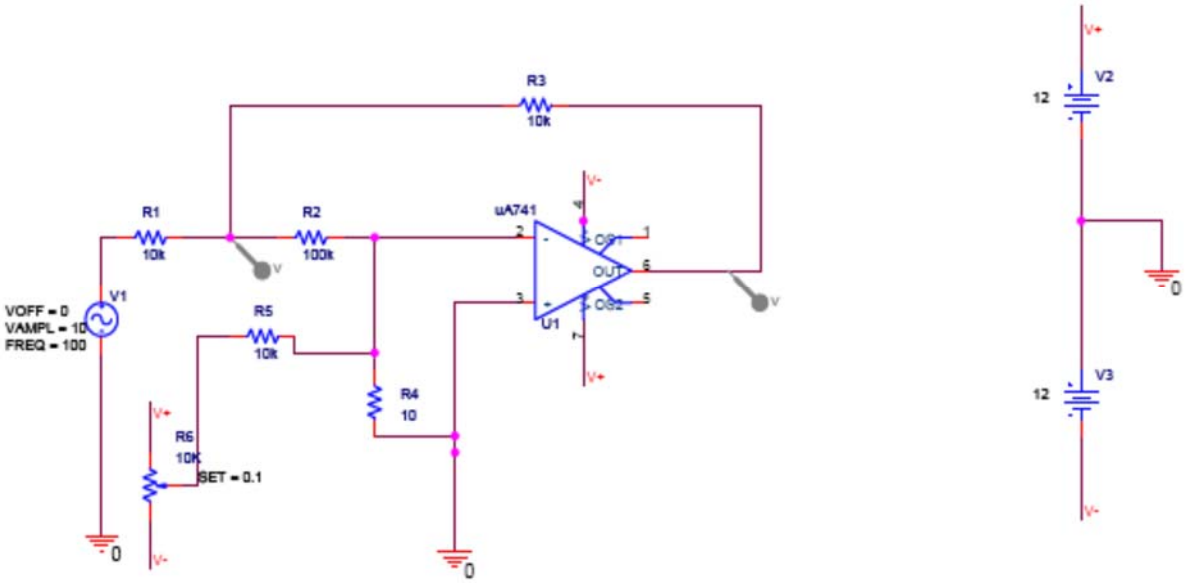


Fig. 3

- Implement the circuit of fig.3
- Connect Function Generator at resistance R1.
- Set the Function Generator to 100 Hz frequency, and 10 V_{pp}.
- Connect the oscilloscope probe to the output of the amplifier.
- If it shows saturation, reduce input until it shows normal waveform.
- Using potentiometer R6 adjust the average value of the output voltage to be zero, by applying a bias voltage to the inverting input (OFFSET voltage compensation).
- Measure the peak-to-peak Voltage V1 present at the negative pin of LM741.
- Measure the output voltage of the op amp .
- Measure the values of the resistors used in this experiment.
- Using formula calculate the gain of operational amplifier.

$$G_v = V_o (R_{in} + R_2) / (V_1 * R_{in})$$
Where $R_{in} = R_4$ // to ($R_5 + R_6$)

OFFSET VOLTAGE MEASUREMENT:

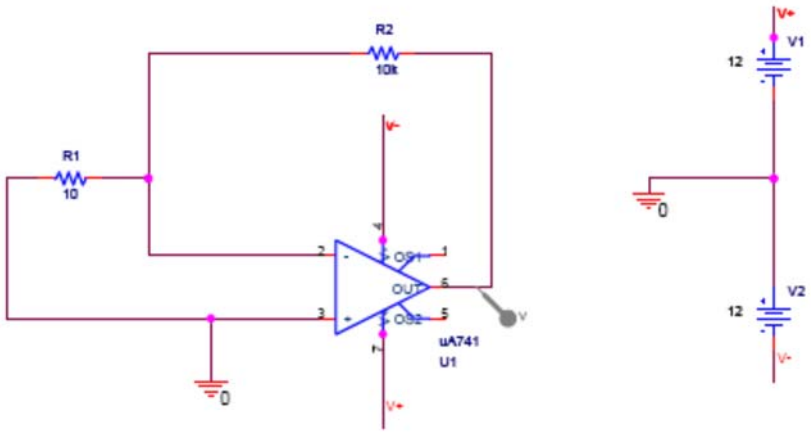


Fig.4

- Implement the circuit of fig.4
- With the multimeter (function VDC) measure the output voltage of the operational amplifier.

OUTCOME:
The open loop gain comes out to be:
The offset voltage comes out to be:

Lab No. 14

OBJECTIVE:

To measure the slew rate and bandwidth of an op amp.

EQUIPMENT REQUIRED:

Protoboard
Function Generator
Digital Multimeter
Power Supply
Resistors
741 op-amp

THEORY:

The slew rate is defined as the speed with which the amplifier can change its output voltage. This parameter is measured in volts/second (or volts/μs) and can be measured with the circuit shown in Fig. 1.

$$SR = (dVo(t)/dt)_{max}$$

To measure this parameter, apply a square wave signal to the amplifier input and measure the change in output voltage during a short time interval (e.g. in one μs)

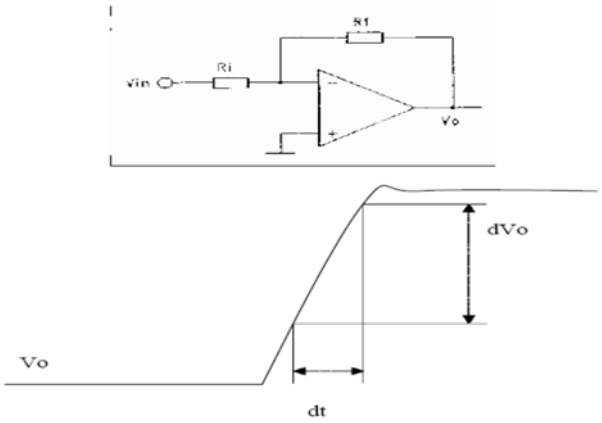


Fig. 1

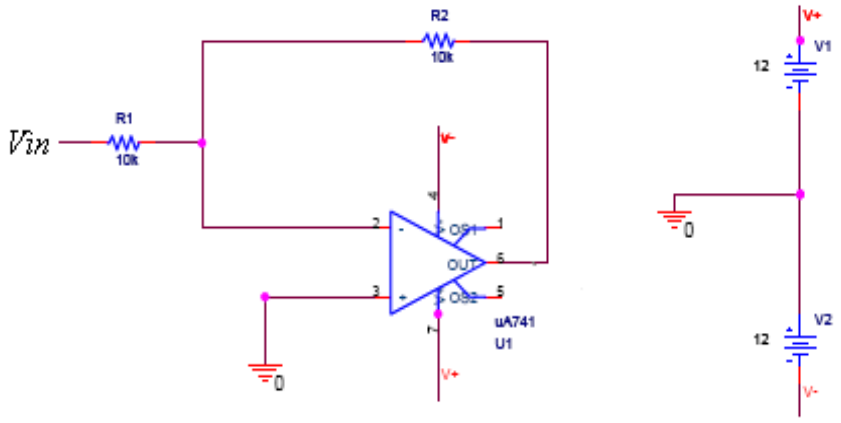


Fig. 2

SLEW RATE MEASUREMENT

- Implement the circuit in fig.2
- Apply a square-wave signal, 10 KHz, 3Vpp and zero average voltage value between terminal 2 and ground.
- Connect the first probe of the oscilloscope to the input of the circuit (terminal 2) and the second to the output of the amplifier.
- Measure the time taken for the output to raise from -1 V to + 1 V.

BANDWIDTH:

- Keep the previous circuit as shown in fig.2
- Apply a Sine wave, 100Hz, $1V_{pp}$ between input terminals.
- Note down the output voltage.
- Increase the frequency to all values shown in table and record the output voltage at each frequency.
- Plot the graph of output voltage w.r.t frequency.
- Determine the frequency at which the output voltage drops to 0.707 of its maximum value.
- Measure the frequency for which the amplification is equal to 1.

OBSERVATION:

SLEW RATE

Quantity	Observed Value
dVo	
D	
SR	

BANDWIDTH:

Input Frequency	**Output Voltage**
100Hz	
500Hz	
1KHz	
10KHz	
20KHz	
50KHz	
100KHz	
200KHz	
500KHz	

OUTCOME:

- The slew rate of the op-amp comes out to be…
- The bandwidth of the op-amp comes out to be…