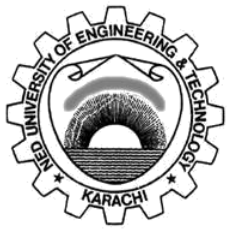


Department of Electronic Engineering

N.E.D. University of Engineering & Technology,

PRACTICAL WORK BOOK

For the course

ANALOG INTEGRATED CIRCUITS

(EL-239) For S.E (EL & TC)

Instructors name: _____

Student Name: _____

Roll no.: _____ **Batch:** _____

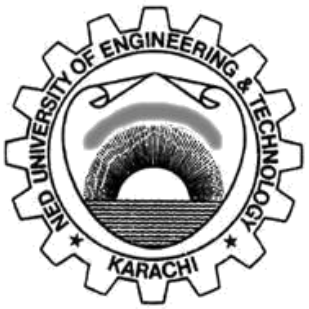
Semester: _____ **Year:** _____

Department: _____

LABORATORY WORK BOOK
FOR THE COURSE

EL - 239 ANALOG INTEGRATED CIRCUITS

Prepared By:
Ayesha Akhtar (Lecturer)



Approved By:
The Board of Studies of Department of Electronic Engineering

Analog Integrated Circuit Laboratory Manual
CONTENTS

LAB SESSION 01

To learn how to use Cadence Virtuoso for IC Designing

Student Name: _____
Roll no.:_____ Batch: _____
Semester:_____ Year:_____

Total Marks	Marks Obtained

Remarks (if any) :_____

Instructor Name:_____

Instructor Signature:_____Date:_____

NED University of Engineering and Technology, Karachi

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Cognitive Domain Assessment Rubric				
Skill Sets	**Extent of Achievement**			
	0	**1**	**2**	**3**
Software Identification Sensual ability to **identify Software** and/or its component for a lab work	Unable to identify the **Software**	-	-	Able to identify **Software** as well as its components
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Weighted CLO (Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 01

OBJECTIVE:

To learn how to use Cadence Virtuoso for IC Designing

EQUIPMENT REQUIRED:

Linux and Cadence Virtuoso installed PC

INTRODUCTION:

We will be working in three regions during AIC lab.

First of all you will be introduced to a new software i-e Cadence Virtuoso.

Secondly you people will have to implement labs on Orcad PSpice, which will the work done in pre-lab.

Thirdly you will be implementing circuits on bread board so as to get hands on experience.

Before coming to the introduction of Cadence Virtuoso let‟s have a look at the types of ICs

THEORY:

TYPES OF IC:

1. Standard Product
2. Application Specific Integrated Circuit (ASIC)
   a) Full Custom
   b) Semi-Custom

1. STANDARD PRODUCT:

A standard product is produced by the manufacturer for sale to the general public. Standard products are readily available for use by anybody for a wider range of applications.

2. APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC)

The term '**ASIC**' stands for '**application-specific integrated circuit**'. An ASIC is basically an integrated circuit designed specifically for a special purpose or application. Strictly speaking, this also implies that an ASIC is built only for one and only one customer. An example of an ASIC is an IC designed for a specific line of cellular phones of a company, whereby no other products can use it except the cell phones belonging to that product line. The opposite of an ASIC is a standard product or general purpose IC, such as a logic gate or a general purpose microcontroller, both of which can be used in any electronic application by anybody. Aside from the nature of its application, an ASIC differs from a standard product in the nature of its availability. The intellectual property, design database, and deployment of an ASIC are usually controlled by just a single entity or company, which is generally the end-user of the ASIC too.

Thus, an ASIC is proprietary by nature and not available to the general public.

a) FULL-CUSTOM

Full-custom ASIC's are those that are entirely tailor-fitted to a particular application from the very start. Since its ultimate design and functionality is pre-specified by the user, it is manufactured with all the photolithographic layers of the device already fully defined, just like most off-the-shelf general purpose IC's. The use of predefined masks for manufacturing leaves no option for circuit modification during fabrication, except perhaps for some minor fine-tuning or calibration. This means that a full-custom ASIC cannot be modified to suit different applications, and is generally produced as a single, specific product for a particular application only.

b) SEMI-CUSTOM ASIC:

Semi-custom ASIC's, on the other hand, can be partly customized to serve different functions within its general area of application. Unlike full-custom ASIC's, semi-custom ASIC's are designed to allow a certain degree of modification during the manufacturing process. A semi-custom ASIC is manufactured with the masks for the diffused layers already fully defined, so the transistors and other active components of the circuit are already fixed for that semi-custom ASIC design. The customization of the final ASIC product to the intended application is done by varying the masks of the interconnection layers, e.g., the metallization layers.

CADENCE VIRTUOSO:

Cadence Virtuoso is an EDA software .Electronic Design Automation (EDA or ECAD) is a category of software tools for designing electronic systems such as printed circuit boards and integrated circuits. The tools work together in a design flow that chip designers use to design and analyze entire semiconductor chips.

PROCEDURE:

Launching ic_fb log:

Open a new terminal and type the following commands:

- ---
- ---
- ---
- ---

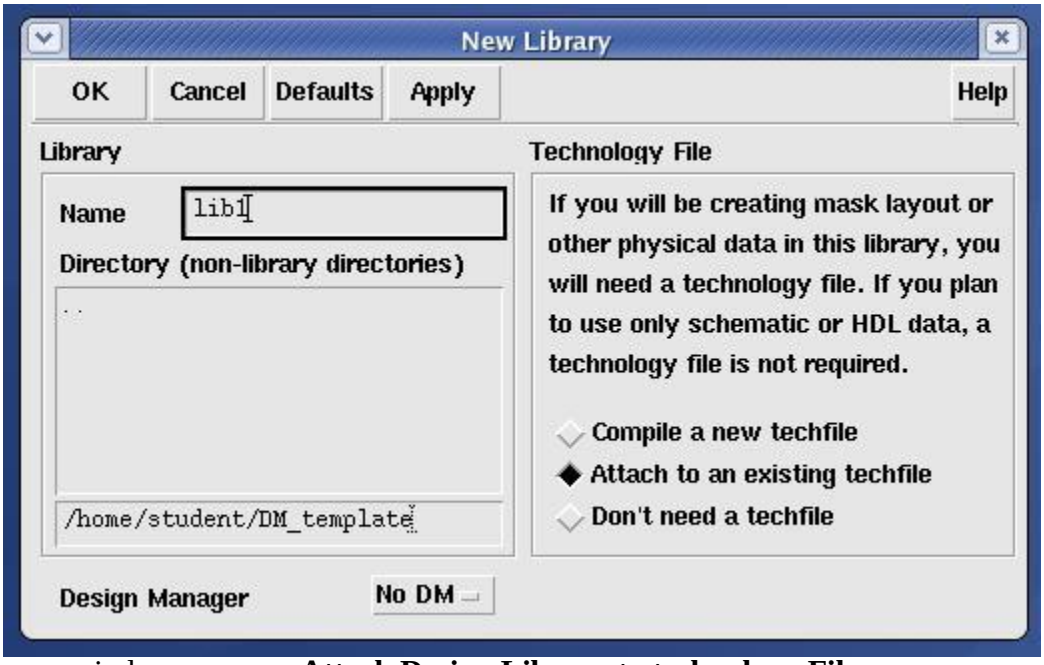
This will launch the window of icfb_log

Creating a Library:

On the icfb_log window

- Click **File**>**New**>**Library to** create a new library. A new window opens

- Assign **Name** to the library as „lib1“
- Select **Attach to an existing technology file**
- Click **Ok**
- The library has been created ,the window will look as follows:

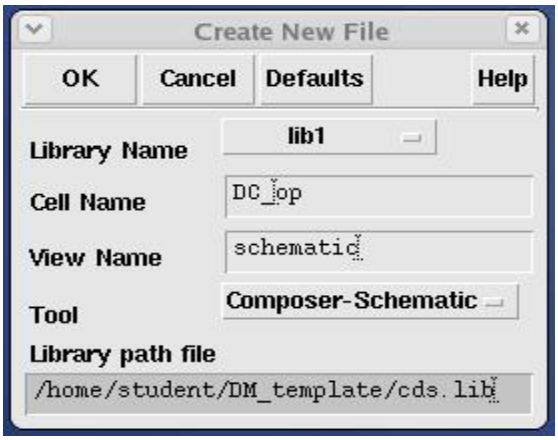


- A new window opens as **Attach Design Library to technology File**
- Select **New Design Library** as „lib 1“
- Select **Technology Library** as **cmrf8sf**
- Click **Ok**
- The window will look like this

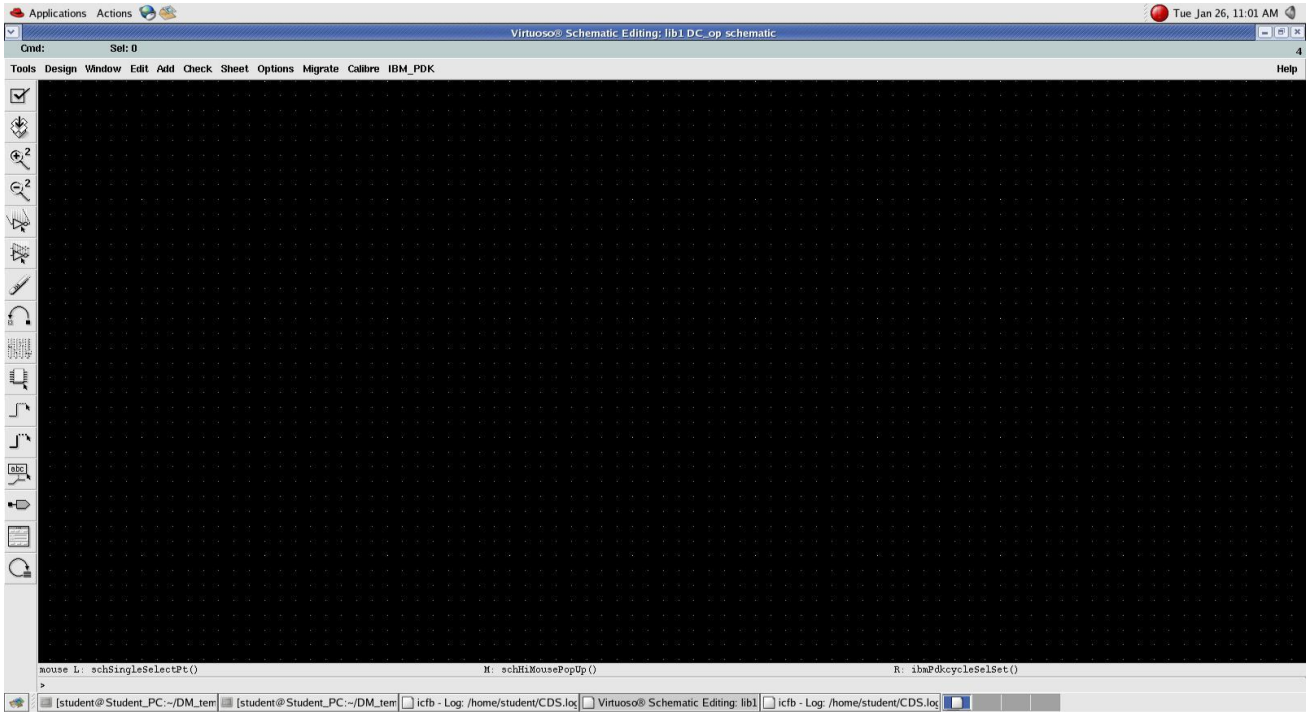
Creating a Cell for Schematic:

In the **icfb_log**

- **Click File>New>Cell View**
  A new window opens by the name **Create New File**
- Provide **Library Name** as „lib1“**, Cell Name** as „DC_op“ **,View Name** as „Schematic“ and **Tool** as „Composer Schematic“
- The window will look like this



Now a schematic window will open .



LAB SESSION 02

To analyze the behavior of MOS transistor using Cadence Virtuoso by simulating its

- I_D v/s V_{GS} curve
- I_D v/s V_{DS} curve

Student Name: _____
Roll no.:_____ Batch: _____
Semester:_____ Year:_____

Total Marks	Marks Obtained

Remarks (if any) :_____

Instructor Name:_____

Instructor Signature:_____Date:_____

NED University of Engineering and Technology, Karachi

Course Code: _____ Course Name: _____

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Weighted CLO (Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 02

OBJECTIVE:

To analyze the behavior of MOS transistor using Cadence Virtuoso by simulating its

- I_D v/s V_{GS} curve
- I_D v/s V_{DS} curve

EQUIPMENT REQUIRED:

Linux and Cadence Virtuoso installed PC

THEORY:

The physical operation of a MOSFET can be divided into three regions of operation. For small value of V_G the transistor is switched off. For an NMOS transistor V_{GS} increases from zero, holes in the p-substrate under the gate are repelled. Thus a depletion region is created from drain to source. For a sufficient value of interface potential, electron from source can actually travel through interface to drain terminal. The value of interface potential at this stage is called "Threshold Voltage" (V_t).

When $V_{GS} > V_t$ and $V_{DS} < (V_{GS} - V_t)$: Triode of Linear Region

In this region of operation MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages. The current from drain to source is modeled as:

Where μ_n is the charge-carrier effective mobility, W is the gate width, L is the gate length and C_{ox} is the gate oxide capacitance per unit area.

When $V_{GS} > V_t$ and $V_{DS} > (V_{GS} - V_t)$: Saturation Region

The switch is turned on, and a channel has been created, which allows current to flow between the drain and source. Since the drain voltage is higher than the gate voltage, the electrons spread out, and conduction is not through a narrow channel but through a broader, two- or three-dimensional current distribution extending away from the interface and deeper in the substrate. The onset of this region is also known as **pinch-off** to indicate the lack of channel region near the drain. The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate–source voltage, and modeled very approximately as:

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$$

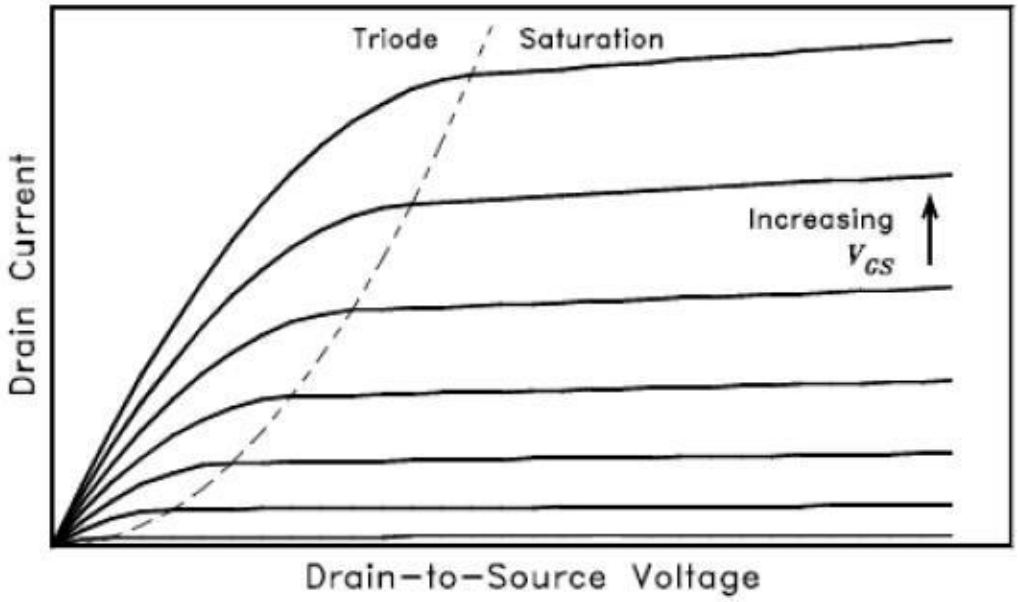


Figure 1:I_D v/s V_{DS} curve for different values of V_{GS}

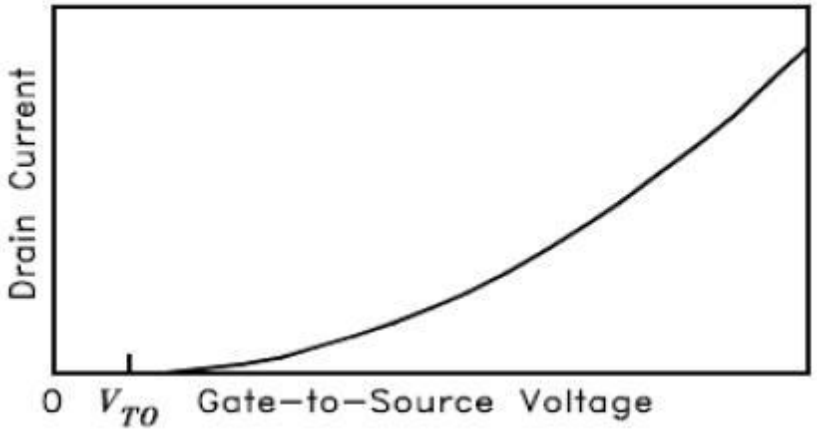


Figure 2: I_D v/s V_{GS} Curve

The characteristic curve of Fig. 1 indicates three regions of operation. The cutoff region, the triode region and the saturation region. The device is cutoff when VGS < Vt whereas it follows a linear relationship in triode region. The MOS operation, therefore, can be modeled as a linear resistor in triode region. Saturation region on the other hand is used when MOS is employed as an amplifier. In saturation region MOS provides a drain current which is independent of VDS and is determined by VGS according to a square law relationship. Thus Fig. 2 shows MOSFET operation as an ideal current source whose value is controlled by VGS.

PROCEDURE:

Launch icfb_log on Linux as explained in Lab Session 1.

Capturing a Cell and Schematic Entry:

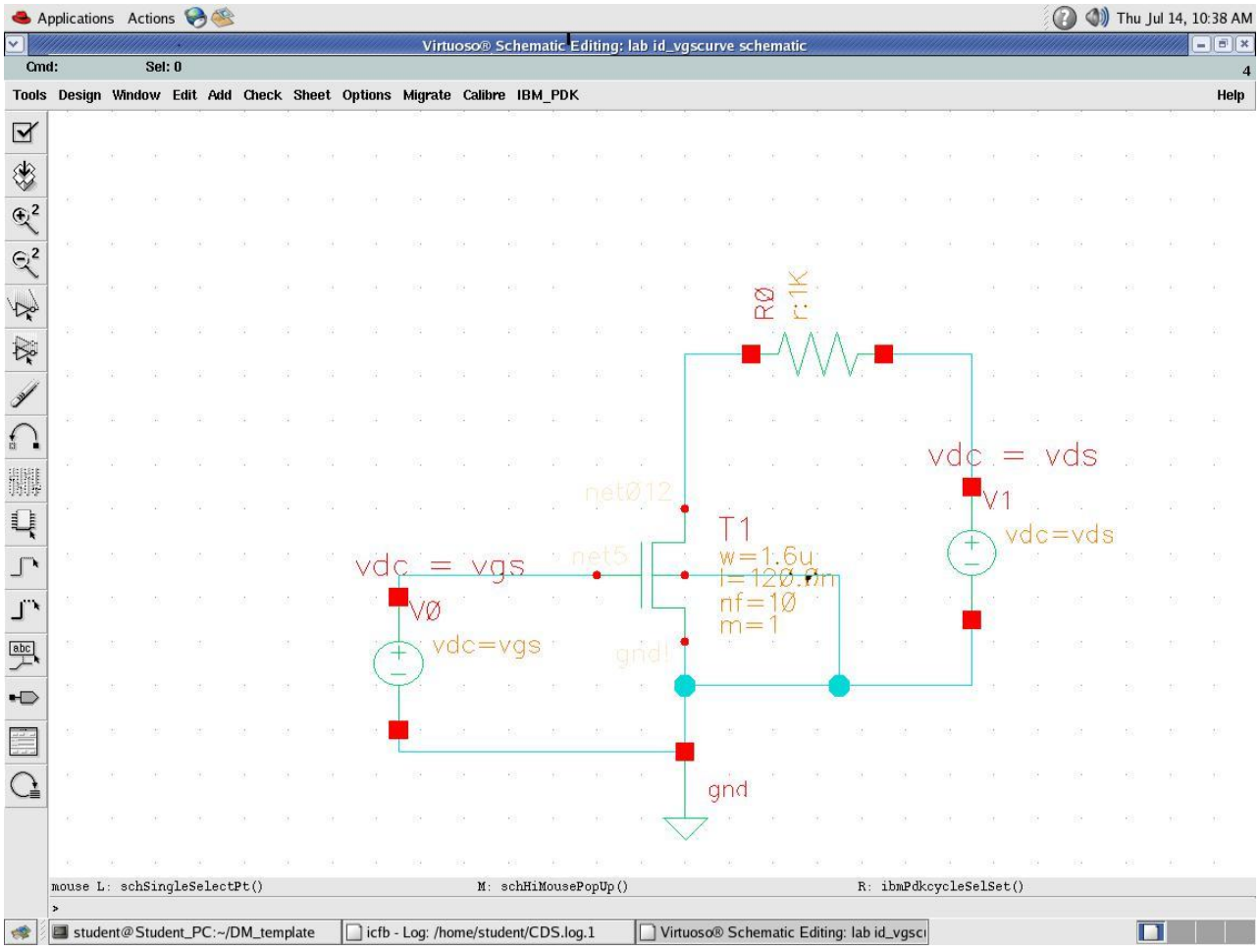
Launch icfb_log on Linux as explained in Lab Session 1.

For I_D v/s V_{DS} Curve:

Draw the following schematic below using these steps

Schematic Entry:

- Use **Add instance** to add components
- Browse **Analog Library** and add the following components:
  - Ideal resistor
  - Vdc (DC Volatge source)
  - Gnd (Ground)
- Browse **cmrf8sf** and add „ nfet“



Simulation:

Perform the steps as explained in lab to determine the id_vgs curve and id_vds curve.

RESULT:

Attach the printout of the results i-e

- I_D v/s V_{GS} curve
- I_D v/s V_{DS} curve

Maximum Marks	Performance = 05
Marks Obtained :	
Remarks (if any) :	

Experiment Evaluated by: _____

Instructor Name: _____

Sign. And Date : _____

LAB SESSION 03

To analyze the behavior of a Common Source Amplifier circuit using Cadence Virtuoso.

Student Name: _____
Roll no.:_____ Batch: _____
Semester:_____ Year:_____

Total Marks	Marks Obtained

Remarks (if any) :_____

Instructor Name:_____

Instructor Signature:_____Date:_____

NED University of Engineering and Technology, Karachi

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

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Group Work Contributes in a group based lab work	Never participates	Rarely participates	Occasionally participates and contributes	Regularly participates and contributes

Weighted CLO (Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 03

OBJECTIVE:

To analyze the behavior of a Common Source Amplifier circuit using Cadence Virtuoso.

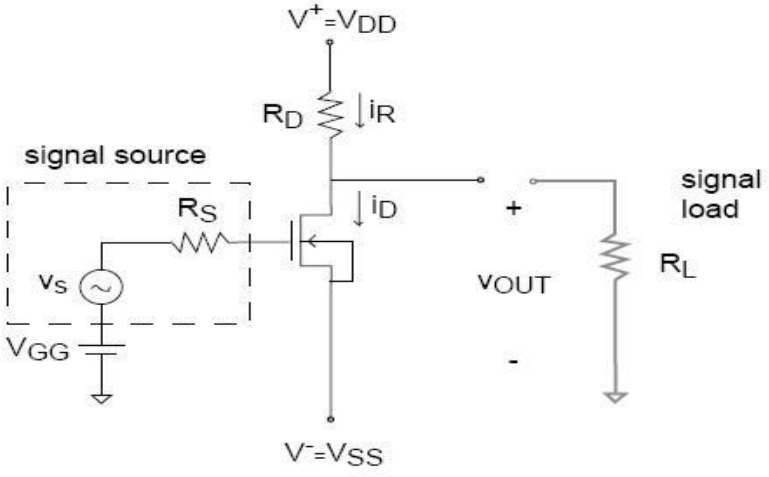
EQUIPMENT REQUIRED:

Linux and Cadence Virtuoso installed PC

THEORY:

A common-source amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a voltage or trans-conductance amplifier. The easiest way to tell if a FET is common source, common drain, or common gate is to examine where the signal enters and leaves. The remaining terminal is what is known as "common". In this example, the signal enters the gate, and exits the drain. The only terminal remaining is the source. This is a common-source FET circuit. The analogous bipolar junction transistor circuit is the common-emitter amplifier.

The common-source (CS) amplifier may be viewed as a trans-conductance amplifier or as a voltage amplifier. As a trans-conductance amplifier, the input voltage is seen as modulating the current going to the load. As a voltage amplifier, input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance according to Ohm's law. However, the FET device's output resistance typically is not high enough for a reasonable trans-conductance amplifier (ideally infinite), nor low enough for a decent voltage amplifier (ideally zero). Another major drawback is the amplifier's limited high-frequency response. Therefore, in practice the output often is routed through either a voltage follower (common-drain or CD stage), or a current follower (common-gate or CG stage), to obtain more favorable output and frequency characteristics. The CS–CG combination is called a cascode amplifier.



PROCEDURE:

Launch icfb_log on Linux as explained in Lab Session 1.

Capturing a Cell and Schematic Entry:

Draw the schematic by following the steps given in Lab Session 2.

Setting up the Simulation Parameters:

Set up the simulation parameters as explained in lab and view the transient response.

CALCULATION:

The gain of the amplifier is:

RESULT:

Attach the printout of input and output waveform along with their peak-to-peak voltage measurement.

Maximum Marks	Performance = 05
Marks Obtained :	
Remarks (if any) :	

Experiment Evaluated by: _____

Instructor Name: _____

Sign. And Date : _____

LAB SESSION 04

To design and simulate simple MOS current mirror and current amplifier using Cadence Virtuoso

Student Name: _____
Roll no.:_____ Batch: _____
Semester:_____ Year:_____

Total Marks	Marks Obtained

Remarks (if any) :_____

Instructor Name:_____

Instructor Signature:_____Date:_____

NED University of Engineering and Technology, Karachi

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Weighted CLO (Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 04

OBJECTIVE:

To design and simulate simple MOS current mirror and current amplifier using Cadence Virtuoso

EQUIPMENT REQUIRED:

Linux and Cadence Virtuoso installed PC

THEORY:

Current Mirrors are fundamental building blocks of Analog Integrated Circuits. Operational amplifiers, operational trans-conductance amplifiers and biasing networks are examples of circuits that are composed of current mirrors. Analog integrated circuit implementation techniques such as current mode and switched current use current mirrors as the basic circuit element .The design and layout of current mirrors is therefore an important aspect of successful analog circuit design.

In the simplest form a current mirror is composed of two transistors as shown in Fig.1. Transistor M1 is diode connected transistor and acts as a low impedance input of the current mirror .the drain of M2 is the output of current mirror.

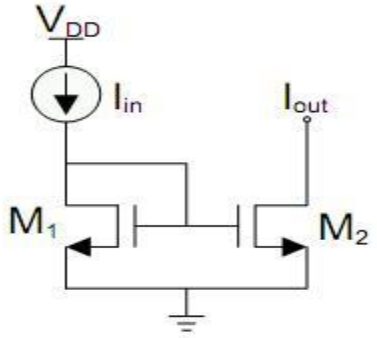

Figure 1: Simple current mirror

Since the gate to source voltage is the same for both the transistors then according to the first order MOSFET model, the drain currents will be equal .This assumes that the transistor sizes are equal as well as the process parameters.

A current mirror is used to mirror the input current into the output branch .A current (I_{in}) entering the diode connected the transistor establishes a gate voltage (V_{GS}).The gate voltage causes I_{out} to low through the output transistor.

If the ratio of the transistors is changed, then the current mirror acts as a current amplifier. The gain of the amplifier is given by:

$$A_i = \frac{\left(W_2/L_2\right)}{\left(W_1/L_1\right)}$$

The above analysis assumed ideal operation of the current mirrors meaning that the drain currents are independent of V_{DS}; however, due to channel length we know this is not true.
The following equation represents the dependence of drain current on V_{DS}.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$$

The excess current due to the differences in V_{DS1} and V_{DS2} will cause a difference in I_{D1} and I_{D2}.To reduce "lambda" effects, the drain to source voltages of the two transistors need to be kept equal.

PROCEDURE:

Launch icfb_log on Linux as explained in Lab Session 1.

Simulating the circuit:

- Perform the simulation steps as explained in lab and determine the dc operating points of MOS Current Mirror and MOS Amplifier.
- Also calculate the percentage difference in the output and input current in the two cases.

CALCULATIONS:

Simple current mirror:

Iref	Io

% error:

Current Amplifier:

Iref	Io

% Error:

RESULT:

Attach the printout of

1) Simple MOS current mirror
2) MOS Amplifier

LAB SESSION 05

To design and simulate cascode current mirror using Cadence Virtuoso.

Student Name: _____
Roll no.: _____ Batch: _____
Semester: _____ Year: _____

Total Marks	Marks Obtained

Remarks (if any) : _____

Instructor Name: _____

Instructor Signature: _____ Date: _____

NED University of Engineering and Technology, Karachi

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

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Weighted CLO (Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 05

OBJECTIVE:

To design and simulate cascode current mirror using Cadence Virtuoso.

EQUIPMENT REQUIRED:

Linux and Cadence Virtuoso installed PC

THEORY:

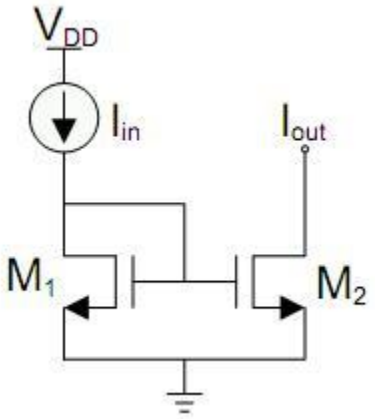

Figure 1: Simple current mirror

$$A_i = \frac{\left(W_2/L_2\right)}{\left(W_1/L_1\right)}$$

The above figure shows a simple current mirror .these current mirrors have non ideal effect that is having limited range of V_{DS2}.Since M1 remains in saturation for all input currents due to its diode connected configuration, M2 needs to be kept in saturation to assume proper operation .If V_{DS2} drops too low, M2 will enter the triode region, and the output current will be much less than what is wanted. The minimum output voltage for the current mirror is sometimes referred to as the compliance voltage .For the simple current mirror, the compliance voltage is $V_{DS\ sat2}$.

Hence to obtain good matching between input and output currents, the drain to source voltages of M1 and M2 must be kept equal .One way to achieve this is by using a cascade current mirror which is as given in figure 2.

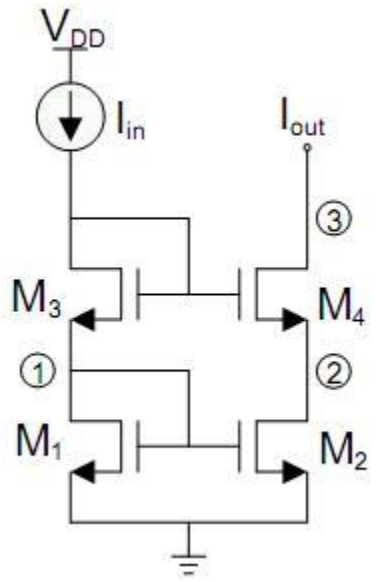

Figure 2: Cascode Current Mirror

Transistors M1 and M2 determine the ratio of the input and output currents. M3 biases M4 which is used to control the drain voltage of M2. If designed correctly, V_{DS1} is approximately equal to V_{DS2} .The benefits of the cascade current mirror are better matching of output currents and larger output resistance .The disadvantage is that a larger compliance voltage is needed to keep both M3 and M4 in saturation. The compliance voltage of Figure 2 is given by:

Node 1: The voltage here is $V_{GS1} = V_T + V_{DSSat1}$.
Node 2: For good matching between input and output currents, we want V_{DS1} and V_{DS2} to be equal .thus, the voltage at node 2 is also $V_T + V_{DSsat1}$.
Node 3: The minimum compliant voltage will be the minimum voltage to keep M3 and M4 is saturation .This will be $V_T + V_{DSsat}1 + V_{DSsat2}$.

As you can see, adding the cascode transistor does not just increase the required compliance voltage by one V_{DSsat}, it also increases it by a threshold voltage.

PROCEDURE:

Launch icfb_log on Linux as explained in Lab Session 1.

Capturing a Cell and Schematic Entry:

Implement the circuit of Cascode Current Mirror as explained in lab 2.

Setting up the Simulation Parameters:

- Perform the simulation steps explained in lab and determine the dc operating points Cascode Current Mirror.
- Also calculate the percentage difference in the output and input current in all the three cases.

CALCULATIONS:

Cascode Current Mirror:

Iref	Io

% Error:

RESULT:

Attach the printout of Cascode Current Mirror

LAB SESSION 06

To analyze Common Gate Amplifier circuit

Student Name: _____
Roll no.:_____ Batch: _____
Semester:_____ Year:_____

Total Marks	Marks Obtained

Remarks (if any) :_____

Instructor Name:_____

Instructor Signature:_____ Date:_____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	**Extent of Achievement**				
	0	**1**	**2**	**3**	**4**
Equipment Identification Sensual ability to **identify** equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
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Observation's Use Displays skills to perform related mathematical calculations using the observations from lab work	Unable to use lab work observations for mathematical calculations	Able to slightly use lab work observations for mathematical calculations	Able to somewhat use lab work Observations for mathematical calculations	Able to moderately use lab work Observations for mathematical calculations	Fully use lab work observations for mathematical calculations
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Equipment Handling equipment care during the use	Doesn't handle Equipment with required care	Rarely handles equipment with required care	Occasionally handles Equipment with required care	Often handles Equipment with required care	Handles equipment with required care
Ability to troubleshoot errors and try to resolve with/without the supervision or guidance	Unable to troubleshoot experimentation errors and resolve them	Able to troubleshoot experimentation errors but cannot resolve them	Able to troubleshoot experimentation errors and resolve them under supervision	Able to troubleshoot experimentation errors independently but need guidance in resolving them	Able to troubleshoot experimentation errors and resolve them without supervision or guidance

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 06

OBJECTIVE:

To analyze Common Gate Amplifier circuit

EQUIPMENT REQUIRED:

- Protoboard
- Function Generator
- Digital Multimeter
- Power Supply
- Resistors
- Transistors: 1 x 2N7000
- Capacitors

THEORY:

BACKGROUND:

MOS transistor is a voltage controlled device, where gate voltage modulates the channel resistance and voltage between drain and source determines current flow between the drain and source terminals. Like BJT, MOS transistor can perform as amplifier and as electronic switch. MOS comes in two different flavors, as NMOS and as PMOS.

Small-Signal Amplifier Design and Biasing

If a small time-varying signal is superimposed on the DC bias at the input (gate or base terminal), then under the right circumstances the transistor circuit can act as a linear amplifier. Figure 1 illustrates the situation appropriate to a MOSFET common-source amplifier. The transistor is first biased at a certain DC gate bias to establish a desired drain current, shown as the "Q"-point (quiescent point) Figure 1a. A small AC signal of amplitude ΔV_{gs} is then superimposed on the gate bias, causing the drain current to fluctuate synchronously. If ΔV_{gs} is small enough, then we can approximate the I_d vs. V_{gs} curve by a straight line with a slope given by

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \qquad (1)$$

and then the drain current amplitude is $\Delta I_d = g_m \Delta V_{gs}$. With a drain resistor R_d as shown, the drain current is related to the output voltage by $V_{dc} = V_{dd} - I_d R_d$, so the AC output signal will be given by

$$\Delta V_{dc} = -\Delta I_d R_d = -g_m R_d \Delta V_{gs} \qquad (2)$$

The voltage gain is therefore $A_v = -g_m R_d$. This can be appreciated graphically using a load-line approach as in Figure 1b.

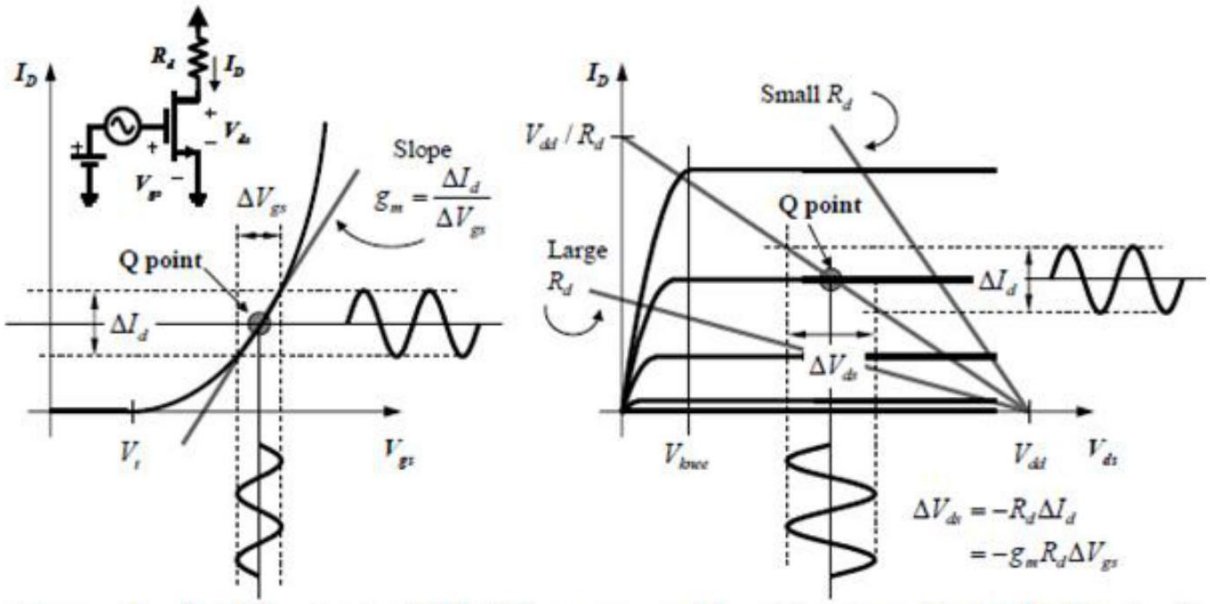

Figure 1 – Amplification in a MOSFET common-source configuration. (a) A small AC signal is superimposed on the DC gate bias, creating an AC drain current. (b) Same situation with a load-line superimposed on the output characteristic, showing how the AC drain current leads to an AC drain voltage and gain of $-g_m R_d$.

Figure 1 also illustrates the importance of the bias point selection in the operation of transistor amplifiers. Figure 1a shows that the transconductance (and hence the gain) will depend on the gate bias; this can be quantified using the I_d vs. V_{gs} characteristic

$$I_m = K_n \left(V_{gs} - V_t \right)^2 \qquad (3)$$

Substituting (3) into (1) gives

$$g_m = 2K_n (V_{gs} - V_t) = 2\sqrt{K_n I_d} = \frac{2I_d}{(V_{gs} - V_t)} \qquad (4)$$

To establish a large transconductance we must bias the device well above threshold. This is also important to insure that the transistor stays in saturation over the full AC cycle. However, there is a limit on gate bias and drain current imposed by the output characteristic and load resistor as shown in Figure 1b. To allow for maximum output voltage swing the Q-point should lie approximately halfway between V_{dd} and the edge of the ohmic region, shown in the figure as V_{knee}. If the drain current or load resistor is too large, the device will swing into the ohmic region during operation leading to significant waveform distortion.

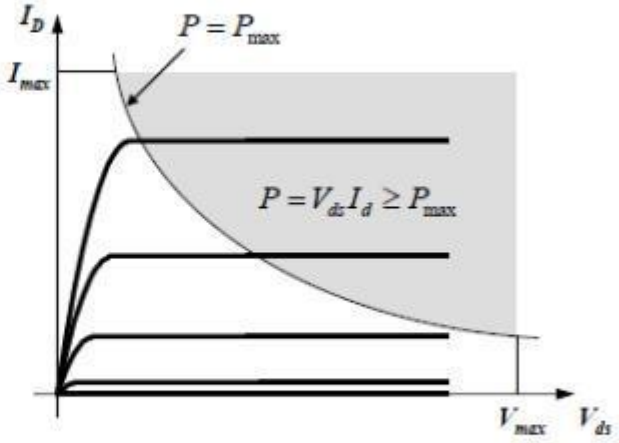

Figure 2 – Limitations on biasing imposed by maximum power considerations.

Another important consideration is the DC power dissipation in the device given by $P = V_{ds} I_d$. This power is dissipated as heat within the device so there is always a thermal limit on the dissipated power for every device and package. The datasheet will specify the maximum DC power P_{max}, maximum DC current $I_{d\,max}$, and maximum DC voltage $V_{ds\,max}$, to avoid destroying the device. These limits are superimposed on the output characteristic in Figure 2. The Q-point must be selected to lie below the shaded region in the figure.

Although the focus has been on MOSFETs in this discussion, it is important to recognize that the key conclusions above are largely independent of the choice of device. All transistors can be described by an output-current versus input-voltage characteristic like that in Figure 2-1a, and hence by a bias-dependent transconductance. Only the details of the voltage dependence will be different. For example, BJTs follow a diode-like exponential model; state-of-the-art short-channel MOSFETs have a nearly linear I_d vs. V_{gs} characteristic and hence a constant g_m.

Lastly, note that the supply voltage is also an important variable. Generally a larger supply voltage is desirable for maximum voltage gain and maximum output voltage swing. This can be seen as follows: for a given drain current I_d, the drain resistor that is required for a drain bias of $V_{ds} \approx V_{dd}/2$ is

$$R_d = \frac{V_{dd} - V_{ds}}{I_d} \approx \frac{V_{dd}}{2I_d} \qquad (5)$$

and thus the gain is given by

$$|A_v| = g_m R_d \approx \frac{g_m}{I_d}\frac{V_{dd}}{2} = V_{dd}\sqrt{\frac{K_n}{I_d}} \qquad (6)$$

The maximum gain scales with supply voltage for a specified device and current level.

MOSFET Design Parameters and Subthreshold Currents

For amplifier designs using any transistor (MOSFETs or BJTs) we need to know the transconductance g_m. For MOSFETs, a knowledge of the threshold voltage V_t and the current parameter K_n can be used to estimate g_m using (4), ***assuming the square-law device model (3) holds***. A common method to estimate these parameters is to measure and plot the square-root of I_d versus V_{gs}, which theoretically should yield a linear dependence,

$$\sqrt{I_d} = \sqrt{K_n}\left(V_{gs} - V_t\right) \qquad (7)$$

Thus the x-intercept if such a plot should yield the threshold voltage, and the slope should yield the current parameter.

The 2N7000, also in your parts kit, is at the other extreme: it is intended for larger currents and has an inherently larger transconductance. Consequently we need to operate this device closer to threshold in order to keep the DC currents low, an imperative from a DC power-dissipation standpoint. The data sheet specifies a maximum DC power dissipation of 400mW; for drain voltages in the range of 2.5-5V (appropriate to supply voltages in the range of 5-10V) we would need to keep the currents below ~100mA.

Figure 3 shows a measured plot of *Id* vs. *Vgs* for a 2N7000 for currents in this range; on this scale we can see a significant departure from the square-law characteristic. This device has gate lengths of around 2.5um.

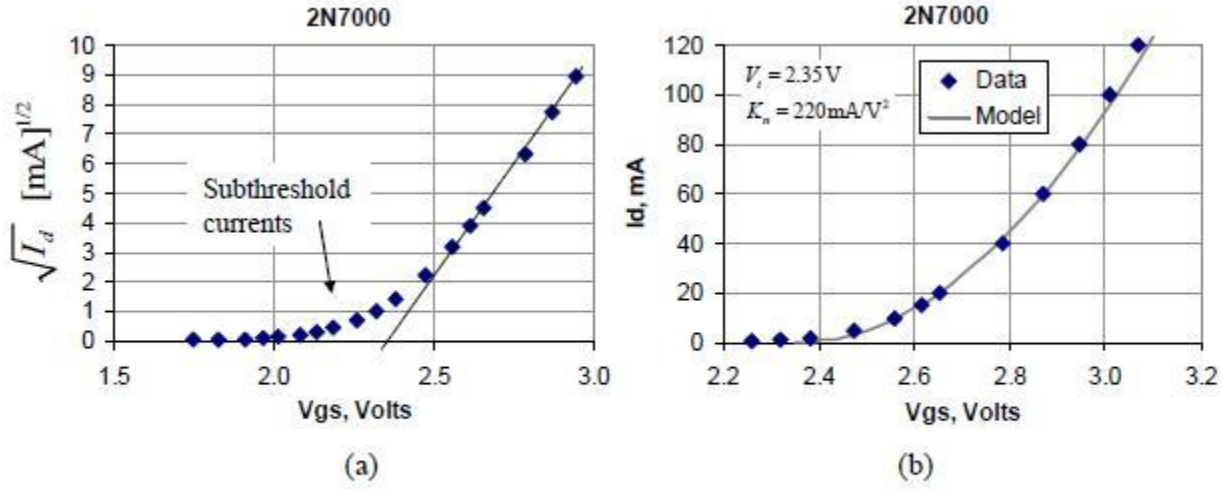

Figure 3 – (a) Data for a 2N7000 device plotted as $\sqrt{I_d}$ vs. V_{gs}, showing sub-threshold currents. (b) Same data set plotted as I_d vs. V_{gs}, with comparison to the ideal model using given parameters (dashed line)

Is this a problem? No, it just means that we can't expect (3) to work well below currents of around 10mA. Above 10mA, the model seems to work reasonably well, and for the particular device shown in Figure 3 we find $V_t \approx 2.35\,\text{V}$ and $K_n \approx 220\,\text{mA/V}^2$.

Remember, these parameters vary from device to device, and also may vary considerably from manufacturer to manufacturer. Figure 4 shows a comparison of characteristic from four different 2N7000 devices, two from one manufacturer, and two from another manufacturer, selected randomly. Not only does the threshold voltage vary, but it is apparent that the current parameter K_n also varies between manufacturers.

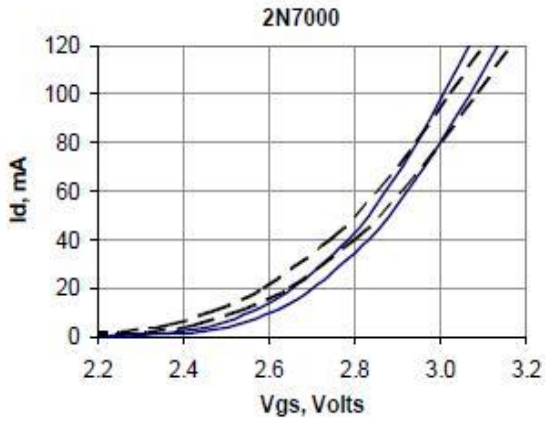

Figure 4 – Comparison of four different 2N7000 devices. Dashed lines and solid lines represent different manufacturers.

Frankly the 2N7000 isn't a great choice for small-signal linear amplifier designs, it is really intended for use in power switching circuits. You might wonder why we chose the 2N7000 for this experiment. The simple answer: it is cheap and ubiquitous, a common theme for components used in AIC labs!

COMMON GATE AMPLIFIER:

As shown in figure 5 the common gate amplifier has a grounded gate terminal , a signal input at the source terminal and the output taken at the drain.

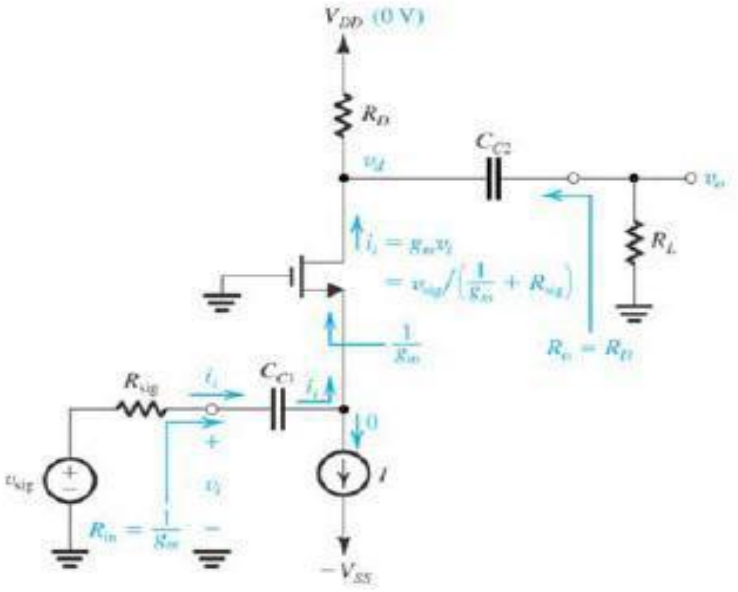

Fig 5: Common Gate Amplifier

Hence Common Gate amplifiers have

- Non-Inverting output
- Moderate input resistance
- Moderately large small signal voltage gain but smaller than common source amplifier.
- Small signal current gain less than one
- Potentially large output resistance (Dependent on R_D)

PRELAB ASSIGNMENT:

Implement a common-gate amplifier, as shown in Figure 6 . Note the 100µF AC coupling capacitor at the input, and the 100µF bypass capacitor on the gate; the latter makes the gate an AC ground, appropriate to the common-gate configuration.

□ Construct the circuit in circuit Figure 6. Be sure to use the correct polarity for the coupling capacitors, or the circuit may not function properly.

□ With the power supply on, the function generator connected to the input port, and the oscilloscope set to observe the input voltage *Vin* , adjust the amplitude of the function generator such that *Vin* is a 10mV sinusoid at 1kHz. Then measure and record the AC voltage gain *Vout / Vin*

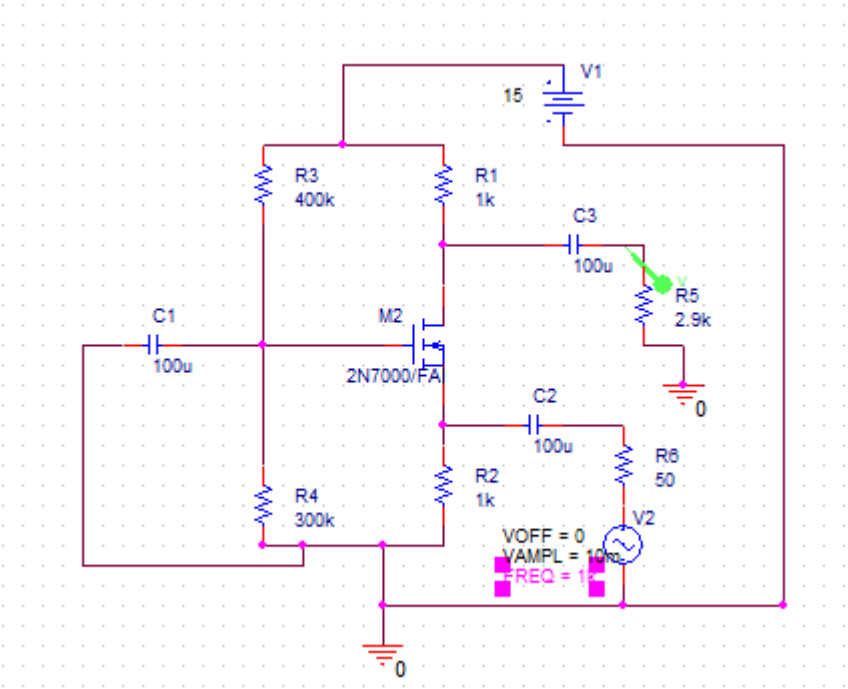

Fig 6: common gate amplifier (practical circuit)

Use the computer software tool OrCAD PSPICE to simulate the circuit.
Make sure to bring the PSPICE results to the laboratory .In addition to being an aid in immediately verifying measured results, **they will be the basis of your Prelab grade for this lab**.

Specifically, the following items must be addressed using OrCAD PSPICE as part of the prelab assignment:

- Circuit drawings with the nodes labeled and with DC node voltages, and DC currents through all branches.
- Transient response (time-domain) with V_{in} = 10mV, showing plots of source voltage (input voltage) and drain voltage (output voltage) waveforms separately. Also mark label to the maximum output voltage (using pspice)

Fill in all entries in the tables provided below that are labeled "simulated"

ANALYSIS:

You are required to analyze a common gate amplifier with drain current is 5mA. Determine the gate , drain and source voltage . perform all necessary calculations .Let Vt= 1V . justify that the circuit can be used as an amplifier

OBSERVATIONS:

DC PARAMETERS:

	Simulated	Measured	% error
V_G (Volts)			
V_S (Volts)			
V_D (Volts)			

TRANSIENT RESPONSE:

V_{in} (at Source):

Simulated	Measured	% error

V_{out} (at Drain)

Simulated	Measured	% error

Gain Calculated:

Simulated	Measured	% error

CALCULATIONS:

RESULT:

Phase Shift between input and output signal ----------

The gain of Common Gate Amplifier is found to be: _____

LAB SESSION 07

To analyze the frequency response of Common gate Amplifier

Student Name: _____
Roll no.:_____ Batch: _____
Semester:_____ Year:_____

Total Marks	Marks Obtained

Remarks (if any) :_____

Instructor Name:_____

Instructor Signature:_____Date:_____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	**Extent of Achievement**				
	0	**1**	**2**	**3**	**4**
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 07

OBJECTIVE:

To analyze the frequency response of Common gate Amplifier

EQUIPMENT REQUIRED:

- Protoboard
- Function Generator
- Digital Multimeter
- Power Supply
- Resistors
- Transistors: 1 x 2N7000

THEORY:

The current-voltage relationships for the MOSFET capture the behavior at low and moderate frequencies. However, similar to the diode, at high frequencies, there are a number of capacitive effects that come into play. These effects can be modeled by adding various capacitors to the MOSFET large and small signal models we have used thus far. For now, lets consider generic signals (could be large or small). First, there is some overlap between the gate and S/D. This overlap capacitance is given by

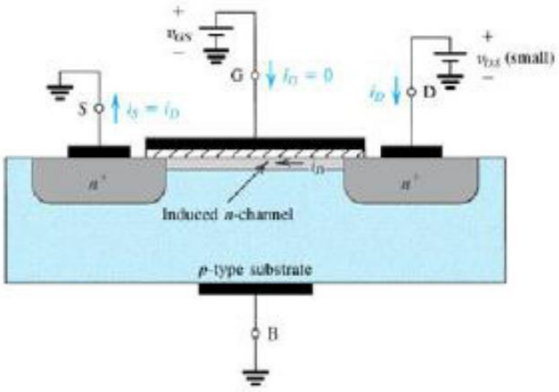
$$C_{ov} = W \cdot L_{ov} \cdot C_{ox}$$

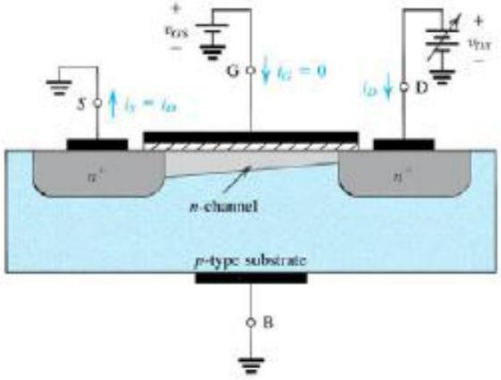
With a self-aligned process, these overlap capacitances can be made very small (Lov ≈ 0.05 .. 0.1 L). The reason is that the gate itself serves as the mask when implanting the S and D regions.

In addition, there is a capacitance between the gate and the induced channel. The value of this gate capacitance is gate

$$C_{gate} = W \cdot L \cdot C_{ox}$$

How this gate capacitive effect manifests itself depends on the operation mode of the transistor.





triode

$$\begin{cases} C_{gs} = \dfrac{1}{2} \cdot C_{gate} + C_{ov} \\ C_{gd} = \dfrac{1}{2} \cdot C_{gate} + C_{ov} \end{cases}$$

saturation

$$\begin{cases} C_{gs} = \dfrac{2}{3} \cdot C_{gate} + C_{ov} \\ C_{gd} = C_{ov} \end{cases}$$

(due to tapered channel)

cutoff

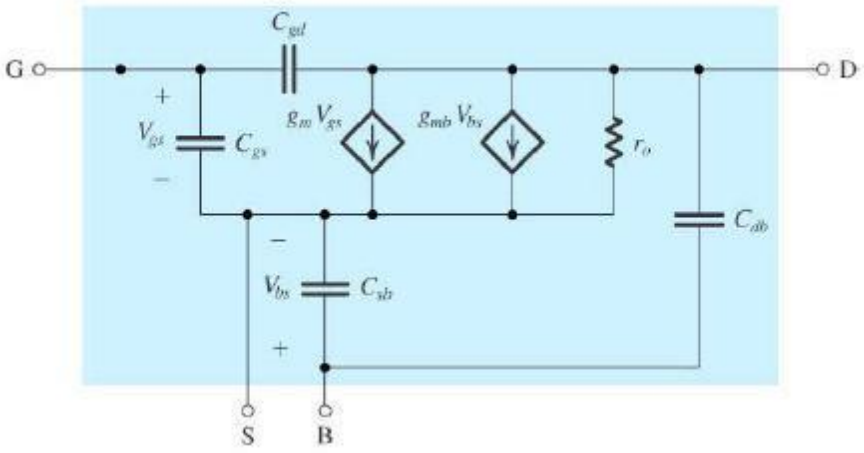
$$\begin{cases} C_{gs} = C_{gd} = C_{ov} \\ C_{gb} = C_{gate} \end{cases}$$

(there is no channel)

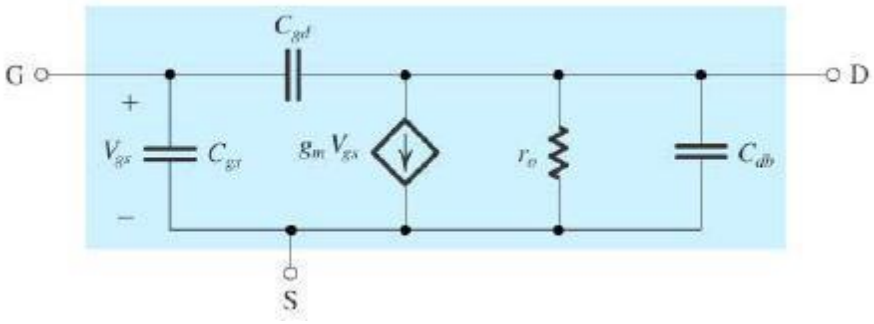
Finally, there is also the junction capacitance associated with the S-B and D-B diodes. These diodes are reverse biased. From our discussion of diodes, we know:

$$C_{sb} = C_j(V_{SB}) \qquad C_{db} = C_j(V_{DB})$$

The equations above capture the capacitive effects for a MOSFET for a generic signal, large or small. In this course, we are mainly interested in the small signal behavior. For small signals, the capacitive effects manifest themselves as small signal capacitors that are added to the small signal model. Remember, for small signals, we will assume the MOSFET is biased in saturation. The resulting high-frequency small-signal model for the MOSFET in saturation now looks as follows:



If S is connected to B (which is typically the case in this course), this simplifies to:



$$C_{gs} = \frac{2}{3} \cdot C_{gate} + C_{ov}$$

$$C_{gd} = C_{ov}$$

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{DB}}{V_0}}}$$

FREQUENCY RESPONSE OF CG AMPLIFIERS.

Miller effect amplifies the role of C_{GD} and it is often the C_M rather than C_{GS} that limits the BW of CS amplifier. Common Gate (CG) amplifier does not suffer from Miller effect since no capacitive coupling (well, almost no) is present between input and output.

Figure shows CG circuit topology for signals only, i.e. power supplies are omitted but assumed.

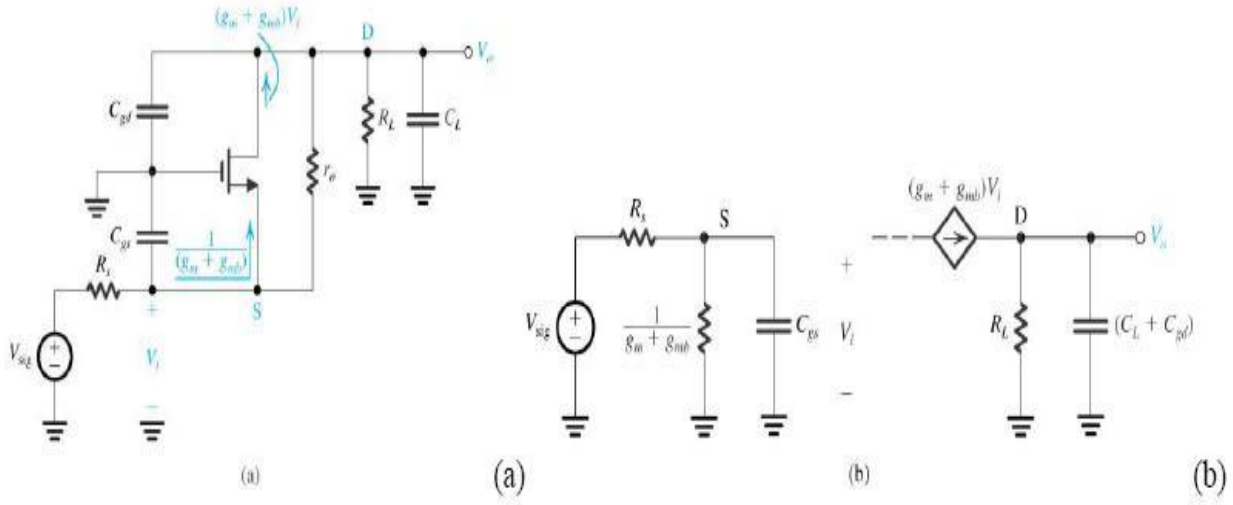


Figure 2b shows an equivalent circuit with r0 ignored and gmb, i.e. “back-gate” transconductance, shown. In integrated circuit (IC) CG amplifiers, gate and back-gate transconductances act together since source-to-gate and source-to-bulk signal voltages are equal to each other (bulk is connected to power supply voltage, i.e. ground for signal). In our lab experiments we should not care about gmb since we often connect bulk to source for simplicity. Effective low-pass-filter at the input of CG amplifier has 3dB cut-off:

$$f_{H\,input} \approx \frac{1}{2 \cdot \pi \cdot \left(R_S \parallel \frac{1}{g_m + g_{mb}} \right) \cdot C_{GS}}.$$

The low-pass-filter at the output will have 3dB cut-off at (often dominant pole in many applications):

$$f_{H\,output} \approx \frac{1}{2 \cdot \pi \cdot (C_{GD} + C_L) \cdot R_L'}.$$

Here RL‟ is an equivalent load, i.e. including RD. Both poles due to input and output low-pass-filters are often higher then f_H for CS amplifier. Hence, BW of CG amplifier is extended as compared to CS one. However, low input impedance of CG amplifier can reduce midband voltage gain especially for signal sources with large internal resistance (observe voltage divider made of RS and 1/(gm + gmb)). Hence we can expect (in our experiments for CG amplifier) wider BW but lower midband gain as compared to CS one.

.

PRELAB ASSIGNMENT:

For the circuit of common gate amplifier implemented in last lab add a capacitor of 1nF between gate and drain use the computer software tool OrCAD PSPICE to simulate it. Make sure to bring the PSPICE results to the laboratory. In addition to being an aid in immediately verifying measured results, **they will be the basis of your Prelab grade for this lab**.

Specifically, the following items must be addressed using OrCAD PSPICE as part of the prelab assignment:

AC Sweep/Noise response with V_{in} = 10mV, showing, showing waveform of Output voltage Vs. Frequency, with frequency range from 1Hz to 10GHz

FREQUENCY RESPONSE:

Frequency	V_{out} (Measured)

Draw a plot of the output voltage Vs Frequency using semi log graph paper.

RESULT:

The Bandwidth of common gate amplifier as determined from the graph is ----------

LAB SESSION 08

To analyze the slew rate of an op-amp

Student Name:_____
Roll no.:_____Batch:_____
Semester:_____Year:_____

Total Marks	Marks Obtained

Remarks (if any) :_____

Instructor Name:_____

Instructor Signature:_____Date:_____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Psychomotor Domain Assessment Rubric-Level P2					
Skill Sets	**Extent of Achievement**				
	0	**1**	**2**	**3**	**4**
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Equipment Use Sensory skills to **describe** the use of the equipment for the lab work	Unable to describe the use of equipment	Rarely able to describe the use of equipment	Occasionally describe the use of equipment	Often able to describe the use of equipment	Regularly able to describe the use of equipment
Safety Adherence Following of **safety** procedures	Doesn't follow Safety procedures	Rarely follow safety Procedures	Occasionally follow Safety procedures	Often follow safety procedures	Fully follow safety procedures
Equipment Handling equipment care during the use	Doesn't handle Equipment with required care	Rarely handles equipment with required care	Occasionally handles Equipment with required care	Often handles Equipment with required care	Handles equipment with required care

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 08

OBJECTIVE:

To analyze the slew rate of an op-amp

EQUIPMENT REQUIRED:

Proto board
Function Generator
Digital Multi meter
Power Supply
Resistors
741op-amp

THEORY:

The slew rate is defined as the speed with which the amplifier can change its output voltage. This parameter is measured in volts/second (or volts/µs) and can be measured with the circuit shown in Fig. 1.

$$SR = (dVo(t)/dt)_{max}$$

To measure this parameter, apply a square wave signal to the amplifier input and measure the change in output voltage during a short time interval (e.g. in one µs)

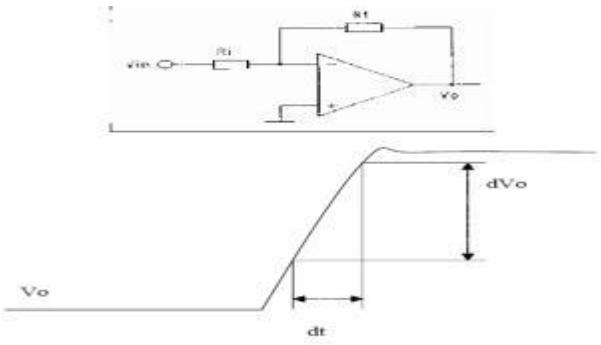

Fig. 1

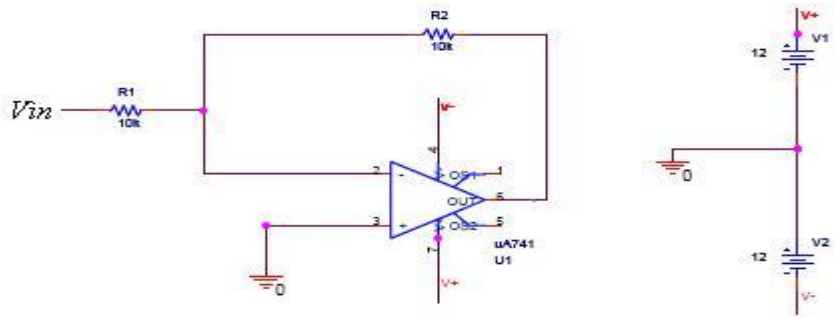

Fig. 2

SLEW RATE MEASUREMENT

- Implement the circuit in Fig. 2
- Apply a square-wave signal, 10 KHz, 3Vpp and zero average voltage value between terminal 2 and ground.
- Connect the first probe of the oscilloscope to the input of the circuit (terminal 2) and the second to the output of the amplifier.
- Measure the time taken for the output to raise from -1 V to + 1 V.

OBSERVATION:

Quantity	Observed Value
dVo	
D	
SR	

RESULT:

- The slew rate of the op-amp comes out to be……..

LAB SESSION 09

To analyze the bandwidth of an op-amp

Student Name: _____
Roll no.:_____Batch: _____
Semester:_____Year:_____

Total Marks	Marks Obtained

Remarks (if any) :_____

Instructor Name:_____

Instructor Signature:_____Date:_____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Psychomotor Domain Assessment Rubric-Level P2					
Skill Sets	**Extent of Achievement**				
	0	**1**	**2**	**3**	**4**
Equipment Identification Sensual ability to **identify** equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
Procedural Skills Displays skills to act upon sequence of steps in lab work	Unable to either learn or perform lab work procedure	Able to slightly understand lab work procedure and perform lab work	Able to somewhat understand lab work procedure and perform lab work	Able to moderately understand lab work procedure and perform lab work	Fully understands lab work procedure and perform lab work
Equipment Use Sensory skills to **describe** the use of the equipment for the lab work	Unable to describe the use of equipment	Rarely able to describe the use of equipment	Occasionally describe the use of equipment	Often able to describe the use of equipment	Regularly able to describe the use of equipment
Safety Adherence Following of **safety** procedures	Doesn't follow Safety procedures	Rarely follow safety Procedures	Occasionally follow Safety procedures	Often follow safety procedures	Fully follow safety procedures
Equipment Handling equipment care during the use	Doesn't handle Equipment with required care	Rarely handles equipment with required care	Occasionally handles Equipment with required care	Often handles Equipment with required care	Handles equipment with required care

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 09

OBJECTIVE:

To analyze the bandwidth of an op-amp

EQUIPMENT REQUIRED:

- Proto board
- Function Generator
- Digital Multi meter
- Power Supply
- Resistors
- 741 op-amp

THEORY:

The bandwidth is defined as the difference between the upper and lower frequencies in a continuous set of frequencies. It is typically measured in hertz.

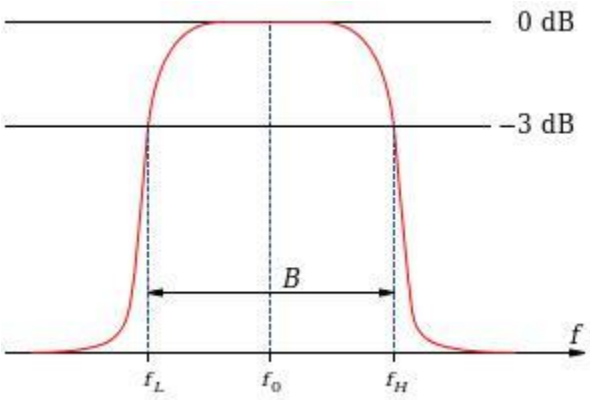

Fig. 1

FORMULA:

$$BW = \frac{f_0}{Q}$$

or

$$BW = f_2 - f_1$$

Where:

BW = bandwidth of a circuit in units of frequency

f_0 = center frequency

f_2 = the upper cutoff frequency

f_1 = the lower cutoff frequency

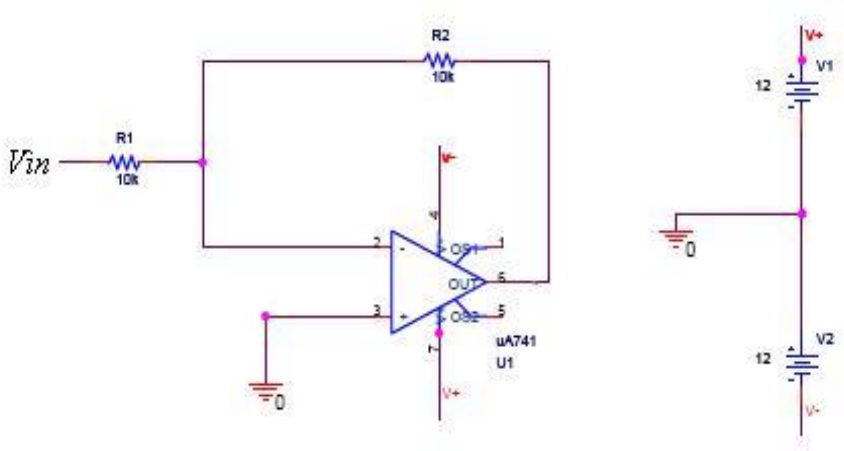

Fig. 2

PROCEDURE :

- Implement the circuit as shown in fig.2
- Apply a Sine wave, 100Hz, $1V_{pp}$ between input terminals.
- Note down the output voltage.
- Increase the frequency to all values shown in table and record the output voltage at each frequency.
- Plot the graph of output voltage w.r.t frequency.
- Determine the frequency at which the output voltage drops to 0.707 of its maximum value.
- Measure the frequency for which the amplification is equal to 1.

OBSERVATION:

Input Frequency	Output Voltage
10Hz	
50 Hz	
100Hz	
500Hz	
1KHz	
10KHz	
20KHz	
50KHz	
100KHz	
200KHz	
500KHz	

RESULT:

- The bandwidth of the op-amp comes out to be……

LAB SESSION 10

To analyze and implement a class B push-pull power amplifier.

Student Name: _____
Roll no.:_____ Batch: _____
Semester:_____ Year:_____

Total Marks	Marks Obtained

Remarks (if any) :_____

Instructor Name:_____

Instructor Signature:_____ Date:_____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Psychomotor Domain Assessment Rubric-Level P2					
Skill Sets	**Extent of Achievement**				
	0	**1**	**2**	**3**	**4**
Equipment Identification Sensual ability to **identify** equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
Procedural Skills Displays skills to act upon sequence of steps in lab work	Unable to either learn or perform lab work procedure	Able to slightly understand lab work procedure and perform lab work	Able to somewhat understand lab work procedure and perform lab work	Able to moderately understand lab work procedure and perform lab work	Fully understands lab work procedure and perform lab work
Equipment Use Sensory skills to **describe** the use of the equipment for the lab work	Unable to describe the use of equipment	Rarely able to describe the use of equipment	Occasionally describe the use of equipment	Often able to describe the use of equipment	Regularly able to describe the use of equipment
Safety Adherence Following of **safety** procedures	Doesn't follow Safety procedures	Rarely follow safety Procedures	Occasionally follow Safety procedures	Often follow safety procedures	Fully follow safety procedures
Equipment Handling equipment care during the use	Doesn't handle Equipment with required care	Rarely handles equipment with required care	Occasionally handles Equipment with required care	Often handles Equipment with required care	Handles equipment with required care

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 10

OBJECTIVE:

To analyze and implement a class B push-pull power amplifier.

EQUIPMENT REQUIRED:

- Proto board
- Function Generator
- Digital Multi meter
- Power Supply
- Resistors
- Capacitors 2x10µF, 220uF
- Diodes: 2x 1N914 or 1N4148
- Transistors: 1xQ2N3904, 1xQ2N3906

INTRODUCTION:

POWER AMPLIFIER:

Power Amplifiers are large signal amplifiers .This generally means that a much larger portion of the load line is used during signal operation than in a small signal amplifier.

Power amplifiers are normally used as the final stage of a communications receiver or transmitter to provide signal power to speakers or to transmitting antenna.

CLASS B PUSH-PULL AMPLIFIERS:

When an amplifier is biased at cut-off so that it operates in the linear region for 180^{o} of the input cycle and is in cutoff for 180^{o}, it is a class B amplifier. The primary advantage of a class B amplifier over a class A amplifier is that either one is more efficient than a class A amplifier; you can get more output power for a given amount of input power. A disadvantage of class B is that it is more difficult to implement the circuit in order to get a linear reproduction of the input waveform.

CLASS B OPERATION:

The class B operation is illustrated in fig.1. Where the output is shown relative to the input in terms of time (t)

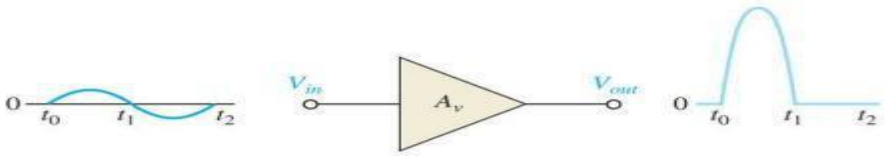

Fig. 1: Basic Class B Amplifier operation

THE Q-POINT IS AT CUTOFF:

The class B amplifier is biased at the cutoff point so that $I_{CQ} = 0$ and $V_{CEQ} = V_{CE\ (cutoff)}$. It is brought out of cutoff and operates in its linear region when the input signal drives the transistor into conduction. This is illustrated in fig.2 with an emitter-follower circuit where, the output is not

replica of the input.

CLASS B PUSH-PULL OPERATION:

The circuit in fig.2 only conducts for the positive half cycle of the cycle. To amplify the entire cycle, it is necessary to add a second class B amplifier that operates on the negative half of the cycle. The combination of two class B amplifiers working together is called push-pull operation.

There are two common approaches for using for using push-pull amplifiers to reproduce the entire waveform. The first approach uses transformer coupling. The second uses two complementary symmetry transistors; these are a matching pair of npn/pnp BJTs or a matching pair of n-channel/p-channel FETs.

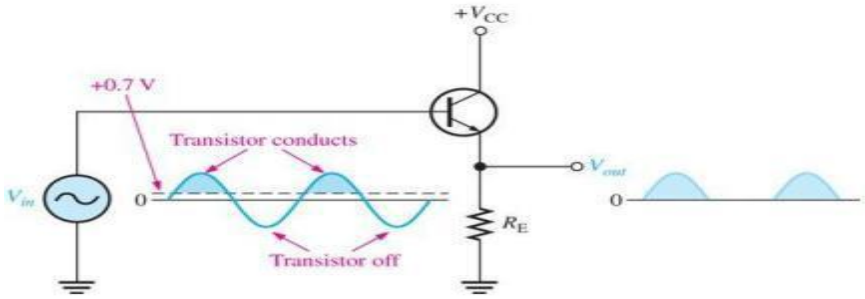

Fig.2: Common collector class B amplifier

TRANSFORMER COUPLING:

Transformer coupling is illustrated in fig.3.The input transformer is center-tapped secondary that is connected to ground, producing phase inversion of one side with respect to the other. The input transformer thus converts the input signal of two out-of-phase signals for the transistors. Notice that both transistors are npn types. Because of the signal inversion, Q_1 will conduct on the positive part of the cycle and Q_2 will conduct on the negative part. The output transformer combines the signals by permitting current in both the directions, even though one transistor is always cut-off. The positive power supply signal is connected to the center tap of the output transformer.

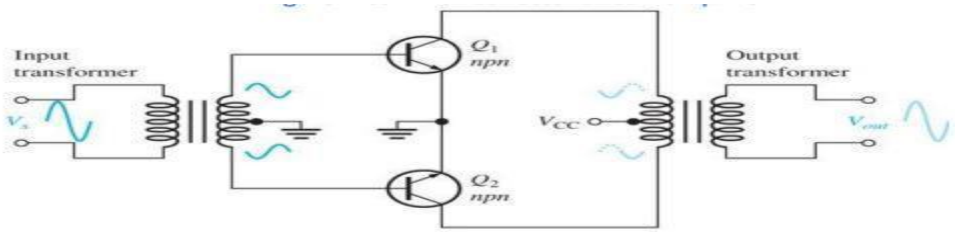

Fig.3: Transformer coupled push-pull amplifiers

COMPLEMENTARY SYMMETRY TRANSISTORS:

Fig.4 shows a push-pull class B amplifier using two emitter-followers and both positive and negative power supplies. This is a complementary amplifier because one emitter-follower uses an npn transistor and the other a pnp, which conduct on opposite alterations of the input cycle. In this circuit there is no dc base bias voltage (V_B=0) .Thus, only the signal voltage drives the transistors into conduction. Transistor Q_1conducts during the positive half of the input cycle, and Q_2 conduct during the negative half.

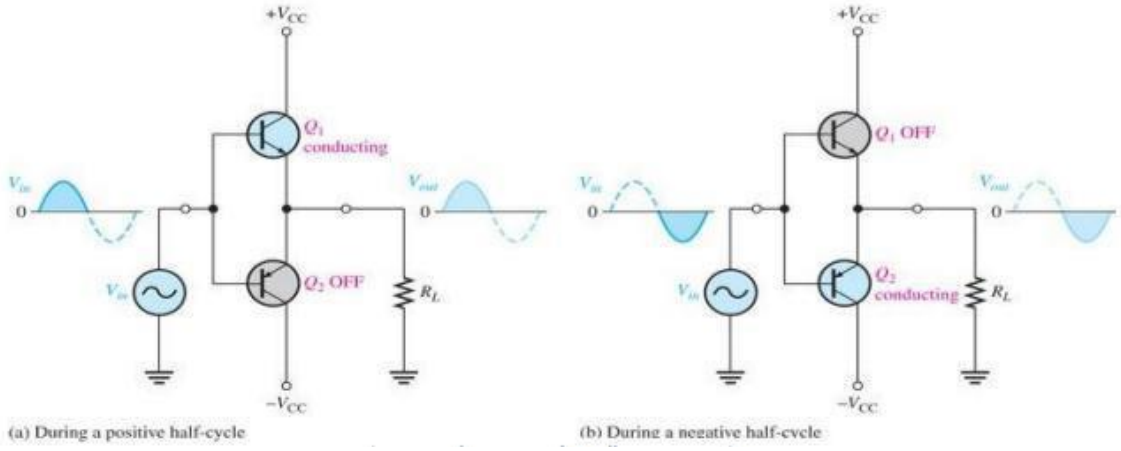

Fig.4: Class B push-pull ac operation.

CROSSOVER DISTORTION:

When the dc base voltage is zero, both transistors are off and the input signal voltage must exceed V_{BE} before a transistor conducts. Because of there is a time interval between the positive and negative alternations of the input when neither transistor is conducting as shown in fig.5. The resulting distortion in the output waveform is called crossover distortion.

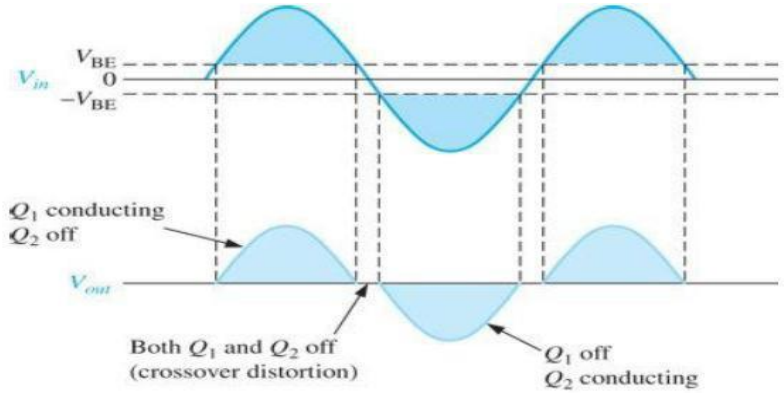

Fig.5: Crossover distortion in a class B push-pull amplifier

EFFICIENCY:

Efficiency is defined as the ratio of AC output power to DC input power .So

$$\eta = \frac{\Pi * V_{out(peak)}}{4 * V_{cc}}$$

PRE-LAB ASSIGNMENT:

Use the computer software tool Orcad PSPICE to simulate the two circuit‟s .Make sure to bring the PSPICE results to the laboratory. In addition to being an aid in immediately verifying measured results, **they will be the basis of your Pre-lab grade for this lab.**

Specifically, the following items must be addressed using Orcad PSPICE as part of the pre lab assignment:

For the circuit in Fig 6.

- Transient response (time-domain) with v_{in} = 3 V (peak), Now increase the peak-to-peak input signal so that the output peaks just clip off. Measure the peak to peak voltage across the 1kΩ load resistor showing plots of input and output voltage waveforms separately.

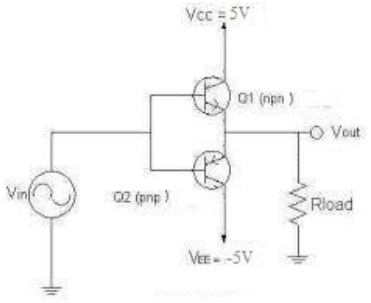

Fig. 6: Class B push-pull Power amplifier circuit to be implemented

PROCEDURE:

1. Wire the circuit shown in figure 6.
2. Connect channel 1 of your oscilloscope at the input and channel 2 at the output.
3. Apply power to the bread board and adjust the sine the wave output level of the generator at 6 V peak-to-peaks at a frequency of 1 kHz.
4. Now carefully increase the peak-to-peak input signal so that the output peaks just clip off. Measure the peak to peak voltage across the 1kΩ load resistor .Record the observations in table 1.
5. Finally, compute the percent efficiency (%η) of your amplifier.

USEFUL FORMULA:

$$\eta = \frac{\Pi * V_{out}(peak)}{4 * V_{cc}}$$

OBSERVATION:

Class B Amplifier Efficiency

Parameter	**Measured Value**
V_o(peak)	
Vcc	

CALCULATION:

RESULT:

The efficiency of class B amplifier is found to be:_____

LAB SESSION 11

To analyze and implement class AB push-pull power amplifier

Student Name: _____
Roll no.:_____ Batch: _____
Semester:_____ Year:_____

Total Marks	Marks Obtained

Remarks (if any) :_____

Instructor Name:_____

Instructor Signature:_____Date:_____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Psychomotor Domain Assessment Rubric-Level P2					
Skill Sets	**Extent of Achievement**				
	0	**1**	**2**	**3**	**4**
Equipment Identification Sensual ability to **identify** equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
Procedural Skills Displays skills to act upon sequence of steps in lab work	Unable to either learn or perform lab work procedure	Able to slightly understand lab work procedure and perform lab work	Able to somewhat understand lab work procedure and perform lab work	Able to moderately understand lab work procedure and perform lab work	Fully understands lab work procedure and perform lab work
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 11

OBJECTIVE:

To analyze and implement class AB push-pull power amplifier

EQUIPMENT REQUIRED:

- Proto board
- Function Generator
- Digital Multi meter
- Power Supply
- Resistors
- Capacitors 2x10µF, 220uF
- Diodes: 2x 1N914 or 1N4148
- Transistors: 1xQ2N3904, 1xQ2N3906

INTRODUCTION:

POWER AMPLIFIER:

Power Amplifiers are large signal amplifiers .This generally means that a much larger portion of the load line is used during signal operation than in a small signal amplifier.

Power amplifiers are normally used as the final stage of a communications receiver or transmitter to provide signal power to speakers or to transmitting antenna.

CLASS AB PUSH-PULL AMPLIFIERS:

When an amplifier is biased at cut-off so that it operates in the linear region for 180^{o} of the input cycle and is in cutoff for 180^{o}, it is a class B amplifier. Class AB amplifiers are biased to conduct for slightly more than 180^{o} .The primary advantage of a class B or class AB amplifier over a class A amplifier is that either one is more efficient than a class A amplifier; you can get more output power for a given amount of input power. A disadvantage of class B or class AB is that it is more difficult to implement the circuit in order to get a linear reproduction of the input waveform.

CLASS B OPERATION:

The class B operation is illustrated in fig.1. Where the output is shown relative to the input in terms of time (t)

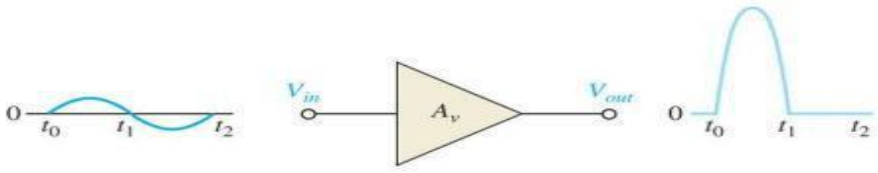

Fig. 1: Basic Class B Amplifier operation

THE Q-POINT IS AT CUTOFF:

The class B amplifier is biased at the cutoff point so that I_{CQ}= 0 and V_{CEQ} = $V_{CE\ (cutoff)}$. It is brought out of cutoff and operates in its linear region when the input signal drives the transistor into conduction. This is illustrated in fig.2 with an emitter-follower circuit where, the output is not replica of the input.

CROSSOVER DISTORTION:

When the dc base voltage is zero, both transistors are off and the input signal voltage must exceed V_{BE} before a transistor conducts. Because of there is a time interval between the positive and negative alternations of the input when neither transistor is conducting as shown in fig.2. The resulting distortion in the output waveform is called crossover distortion.

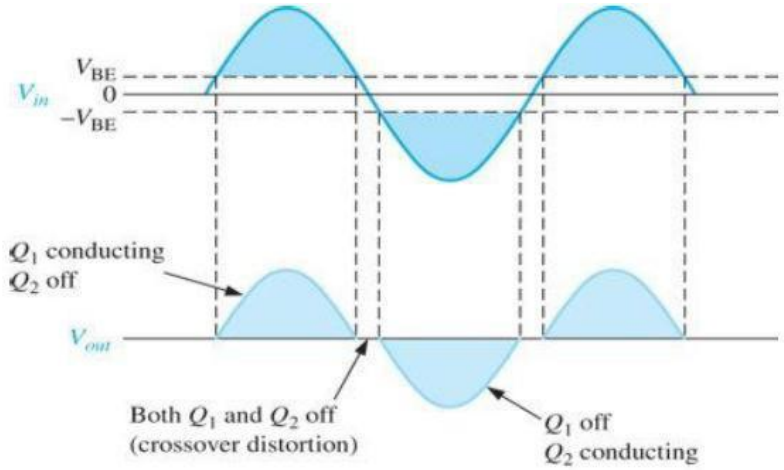

Fig.2: Crossover distortion in a class B push-pull amplifier

BIASING THE PUSH-PULL AMPLIFIER FOR CLASS AB OPERATION:

To overcome crossover distortion, the biasing is adjusted to overcome the V_{BE} of the transistors; this result in a modified form of operation called class AB. In class AB operation, the push-pull stages are biased into slight conduction, even when no input signal is present. This can be done with a voltage-divider and diode arrangement, as shown in fig.3.When the diode characteristics of both diodes are closely matched to the characteristics of the transistor emitter-base junctions, the current in the diodes and the current in the transistors are the same; this is a current mirror. In the bias path both the resistors are also of equal value.

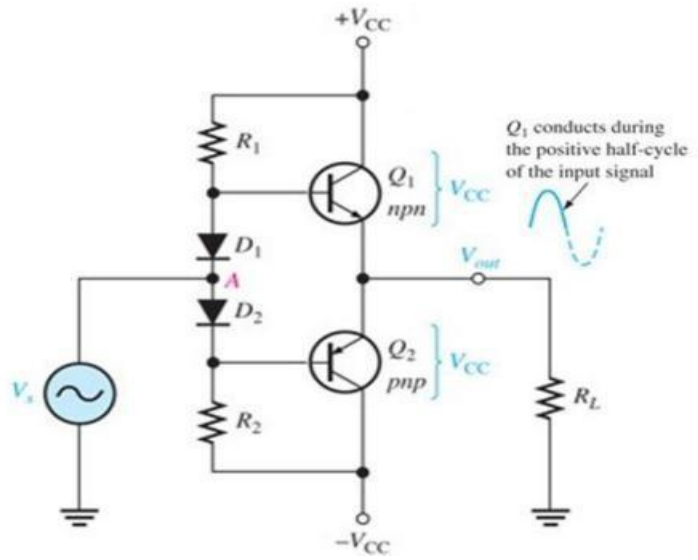

Fig.3: Biasing the push-pull amplifier to eliminate crossover distortion

The AC load line for the class AB amplifier is shown in fig.7

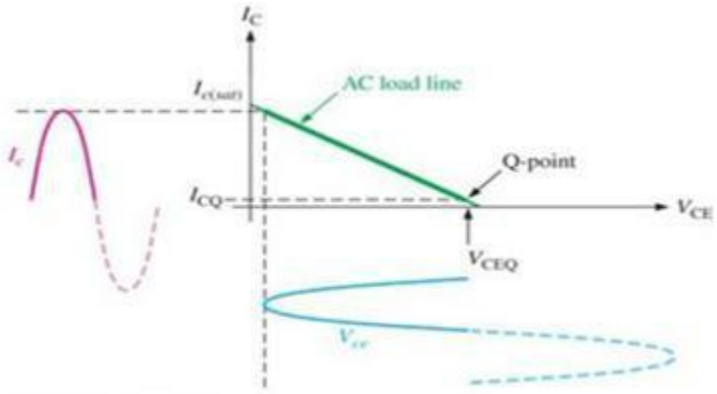

Fig.4: Load lines for a complementary symmetry push-pull amplifier. Only the load lines for the npn transistor are shown

Under maximum condition, $Q_1$and Q_2 is alternatively driven from near cutoff to near saturation that is for Q_1 from 0V to $+V_{CC}$ and for Q2 from 0V and to $-V_{CC}$. The main advantage of class B/AB amplifier over the class A is that there is very little current in the transistor when there is no input signal .This results in low power dissipation when there is no signal.

SINGLE-SUPPLY PUSH-PULL AMPLIFIER:

Push-Pull amplifiers using complementary symmetry transistors can be operated from a single voltage source as shown in fig.8.The circuit operation is the same as described previously, except the bias is set to force the output emitter voltage to be $V_{CC}/2$ instead of 0v used with two supplies. Because the output is not biased at 0V capacitive coupling for the input and output is necessary to block the bias voltage from the source and the load resistor .Ideally the output voltage can swing from zero to V_{CC}, but in practice it does not quite reach these ideal values.

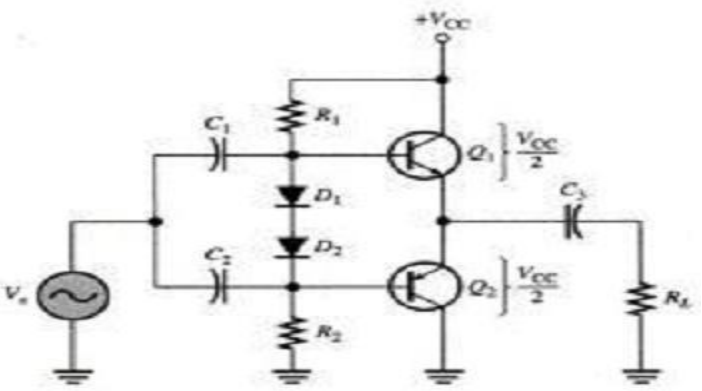

Fig.5:Single-ended push-pull amplifier

PRE LAB ASSIGNMENT:

Use the computer software tool Orcad PSPICE to simulate the two circuits. Make sure to bring the PSPICE results to the laboratory. In addition to being an aid in immediately verifying measured results, **they will be the basis of your Pre-lab grade for this lab.**

Specifically, the following items must be addressed using Orcad PSPICE as part of the pre lab assignment:

- Transient response (time-domain) with v_{in} = 3 V (peak), Now increase the peak-to-peak input signal so that the output peaks just clip off. Measure the peak to peak voltage across the 1kΩ load resistor showing plots of input and output voltage waveforms separately.

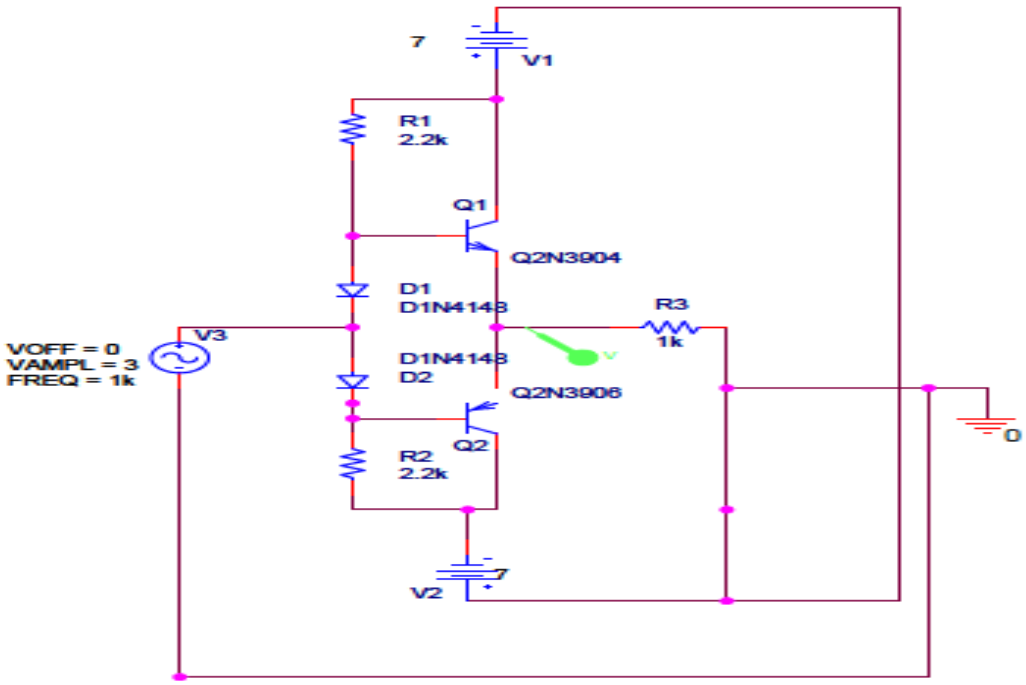

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Fig. 6: Class B push-pull Power amplifier circuit

PROCEDURE

1. Wire the circuit shown in figure 6(a).
2. Connect channel 1 of your oscilloscope at the input and channel 2 at the output.
3. Apply power to the bread board and adjust the sine the wave output level of the generator at 6 V peak-to-peaks at a frequency of 1 kHz .Observe amplifier's input and output waveform. Measure the base-to-emitter voltages required for both transistor to become forward biased, recording these values in table .
4. Now carefully increase the peak-to-peak input signal so that the output peaks just clip off. Measure the peak output voltage just before the output clips off.
5. Finally, compute the percent efficiency (%η) of your amplifier, and compare it with the theoretical efficiency slightly less than 78.5% of a class B amplifier. If a value greater than 78.5% is calculated, then repeat the steps trying to determine the source of your error.

USEFUL FORMULA:

$$\eta = \frac{\Pi * V_{out\ (peak)}}{4 * V_{cc}}$$

OBSERVATION:

Table : Voltage Divider Bias with no crossover distortion

Parameter	**Measured Value**
V_{BE1}	
V_{BE2}	

CALCULATIONS:

Result:

The efficiency of class AB amplifier is found to be:_____

LAB SESSION 12

To design and analyze op-amp based Wein Bridge oscillator.

Student Name: _____
Roll no.:_____ Batch: _____
Semester:_____ Year:_____

Total Marks	Marks Obtained

Remarks (if any) :_____

Instructor Name:_____

Instructor Signature:_____Date:_____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	**Extent of Achievement**				
	0	**1**	**2**	**3**	**4**
Equipment Identification Sensual ability to **identify** equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
Procedural Skills Displays skills to act upon sequence of steps in lab work	Unable to either learn or perform lab work procedure	Able to slightly understand lab work procedure and perform lab work	Able to somewhat understand lab wok procedure and perform lab work	Able to moderately understand lab work procedure and perform lab work	Fully understands lab work procedure and perform lab work
Response Capability to imitate the lab work on his/her own	Unable to imitate the lab work	Able to slightly imitate the lab work	Able to somewhat imitate the lab work	Able to moderately imitate the lab work	Fully imitates lab work
Observation's Use Displays skills to perform related mathematical calculations using the observations from lab work	Unable to use lab work observations for mathematical calculations	Able to slightly use lab work observations for mathematical calculations	Able to somewhat use lab work Observations for mathematical calculations	Able to moderately use lab work Observations for mathematical calculations	Fully use lab work observations for mathematical calculations
Equipment Use Sensory skills to describe the use of the equipment for the lab work	Unable to describe the use of equipment	Rarely able to describe the use of equipment	Occasionally describe the use of equipment	Often able to describe the use of equipment	Regularly able to describe the use of equipment
Equipment Handling equipment care during the use	Doesn't handle Equipment with required care	Rarely handles equipment with required care	Occasionally handles Equipment with required care	Often handles Equipment with required care	Handles equipment with required care
Ability to troubleshoot errors and try to resolve with/without the supervision or guidance	Unable to troubleshoot experimentation errors and resolve them	Able to troubleshoot experimentation errors but cannot resolve them	Able to troubleshoot experimentation errors and resolve them under supervision	Able to troubleshoot experimentation errors independently but need guidance in resolving them	Able to troubleshoot experimentation errors and resolve them without supervision or guidance

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 12

OBJECTIVE:
To design and analyze op-amp based Wein Bridge oscillator.

EQUIPMENT REQUIRED:
- Proto board
- Function Generator
- Digital Multi meter
- Power Supply
- Resistors
- Capacitors 2x1nF
- 741op-amp (8-pin mini DIP)

THEORY:
THE OSCILLATOR
Oscillators are electronic circuits that generate an output signal without the necessity of an input signal. It produces a periodic waveform on its output with only the DC supply voltage as an input. The output voltage can be either sinusoidal or non-sinusoidal, depending on the type of oscillator. Different types of oscillators produce various types of outputs including sine waves, square waves, triangular waves, and saw-tooth waves. A basic oscillator is shown in Figure 1.

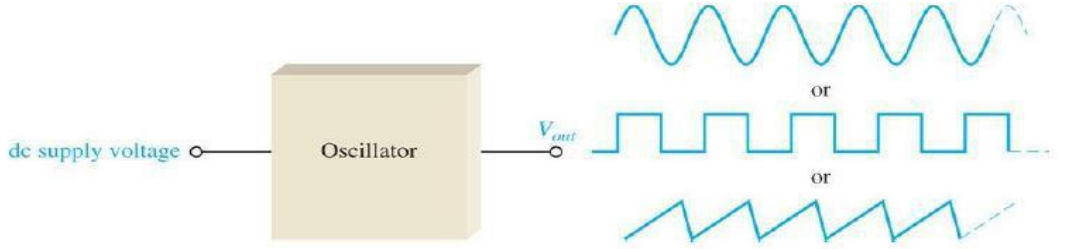


Figure 1 The basic oscillator concept showing three common types of output wave-forms: sine wave, square wave, and sawtooth.

TYPES OF OSCILLATOR:

Oscillators can be of 2 types.
1) Feedback Oscillators
2) Relaxation oscillators

FEEDBACK OSCILLATORS:
One type of oscillator is the feedback oscillator, which returns a fraction of the output signal to the input with no net phase shift, resulting in a reinforcement of the output signal. After oscillations are started, the loop gain is maintained at 1.0 to maintain oscillations.

A feedback oscillator consists of an amplifier for gain (either a discrete transistor or an op-amp) and a positive feedback circuit that produces phase shift and provides attenuation, as shown in Figure 2.

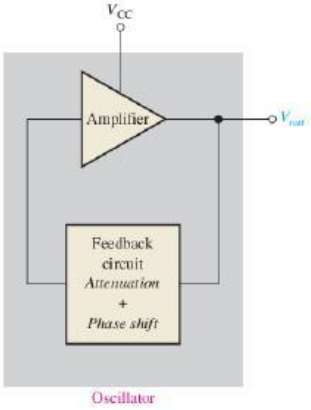


Figure 2 Basic elements of a feedback oscillator.

RELAXATION OSCILLATORS :

A second type of oscillator is the relaxation oscillator. Instead of feedback, a relaxation oscillator uses an RC timing circuit to generate a waveform that is generally a square wave or other non-sinusoidal waveform. Typically, a relaxation oscillator uses a Schmitt trigger or other device that changes states to alternately charge and discharge a capacitor through a resistor.

FEEDBACK OSCILLATORS:

Feedback oscillator operation is based on the principle of positive feedback. Feedback oscillators are widely used to generate sinusoidal waveforms.

POSITIVE FEEDBACK:

In positive feedback, a portion of the output voltage of an amplifier is fed back to the input with no net phase shift, resulting in a strengthening of the output signal. This basic idea is illustrated in Figure 3(a).

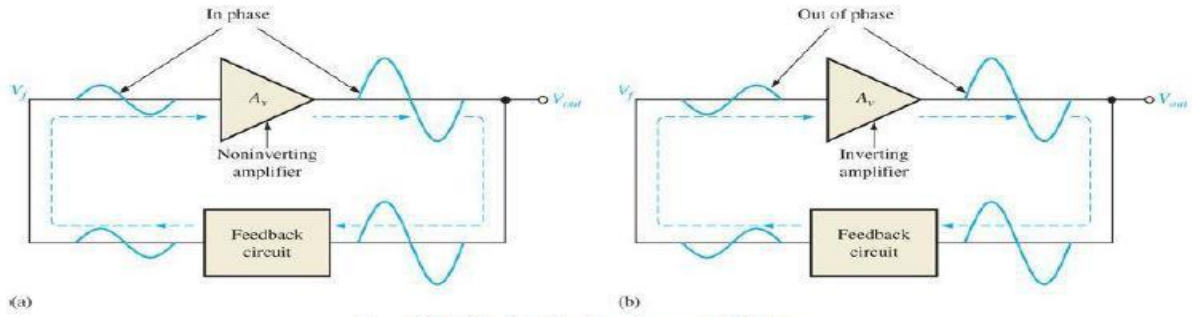


Figure 3 Positive feedback produces oscillation.

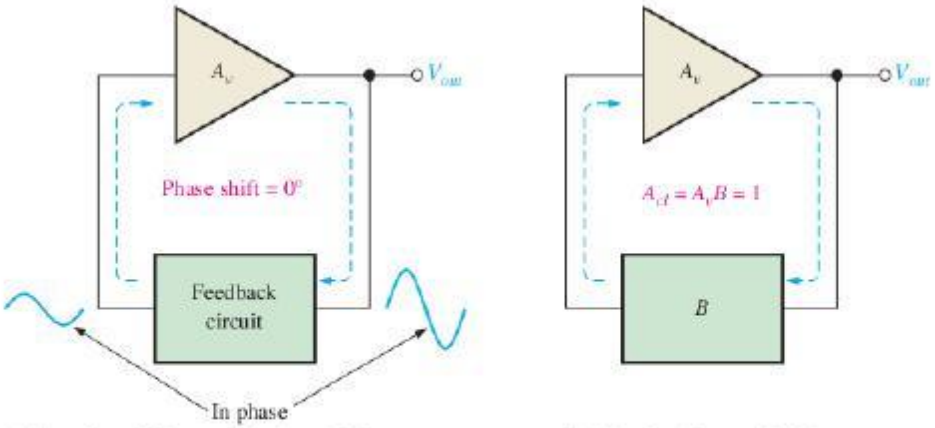
As you can see, the in-phase feedback voltage is amplified to produce the output voltage, which in turn produces the feedback voltage. That is, a loop is created in which the signal maintains itself and a continuous sinusoidal output is produced. This phenomenon is called oscillation.

In some types of amplifiers, the feedback circuit shifts the phase and an inverting amplifier is required to provide another phase shift so that there is no net phase shift. This is illustrated in Figure 3(b).

CONDITIONS FOR OSCILLATION:

Two conditions, illustrated in Figure 4, are required for a sustained state of oscillation:

1. The phase shift around the feedback loop must be effectively
2. The voltage gain, A_{cl}, around the closed feedback loop (loop gain) must equal 1 (unity).



(a) The phase shift around the loop is 0°. (b) The closed loop gain is 1.

Figure 4 General conditions to sustain oscillation.

The voltage gain around the closed feedback loop, A_{cl}, is the product of the amplifier gain, A_v, and the attenuation B, of the feedback circuit.

$$A_{cl} = A_v \text{ x } B$$

If a sinusoidal wave is the desired output, a loop gain greater than 1 will rapidly cause the output to saturate at both peaks of the waveform, producing unacceptable distortion. To avoid this, some form of gain control must be used to keep the loop gain at exactly 1 once oscillations have started.

For example, if the attenuation of the feedback circuit is 0.01, the amplifier must have a gain of exactly 100 to overcome this attenuation and not create unacceptable distortion(100 x0.01=1).
An amplifier gain of greater than 100 will cause the oscillator to limit both peaks of the waveform.

START-UP CONDITIONS:

The unity-gain condition must be met for oscillation to be maintained.
For oscillation to begin, the voltage gain around the positive feedback loop must be greater than 1 so that the amplitude of the output can build up to a desired level. The gain must then decrease to 1 so that the output stays at the desired level and oscillation is sustained. The voltage gain conditions for both starting and sustaining oscillation are illustrated in Figure 5.

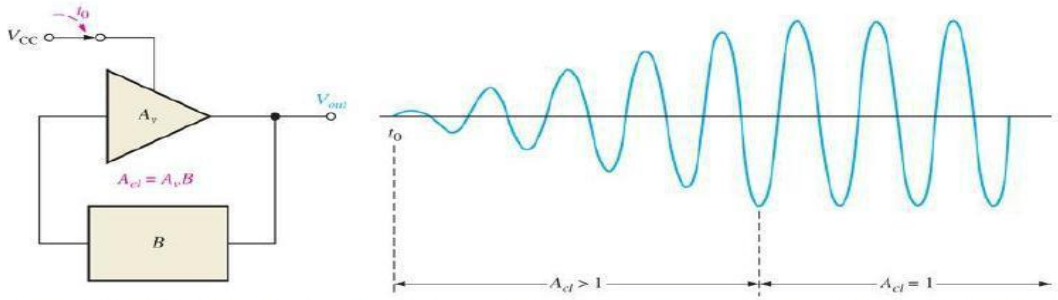


Figure 5 When oscillation starts at t_0, the condition $A_{cl} > 1$ causes the sinusoidal output voltage amplitude to build up to a desired level. Then A_{cl} decreases to 1 and maintains the desired amplitude.

OSCILLATION WITH *RC* FEEDBACK CIRCUITS:

Three types of feedback oscillators that use RC circuits to produce sinusoidal outputs are the

- Wien-bridge oscillator
- Phase-shift oscillator
- Twin-T oscillator

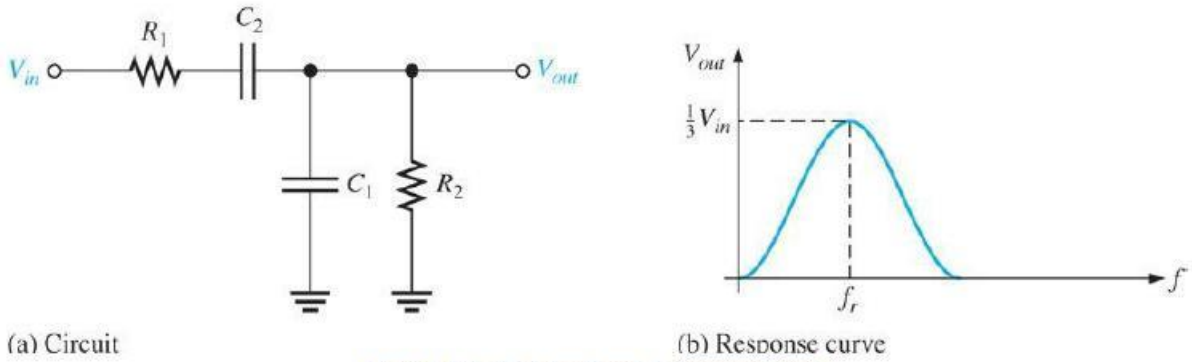
Generally, RC feedback oscillators are used for frequencies up to about 1 MHz.
The Wien-bridge is by far the most widely used type of RC feedback oscillator for this range of frequencies.

WIEN-BRIDGE OSCILLATOR

One type of sinusoidal feedback oscillator is the Wien-bridge oscillator. A fundamental part of the Wien-bridge oscillator is a lead-lag circuit like that shown in Figure 6(a). R_1 and C_1 together form the lag portion of the circuit; R_2 and C_2 form the lead portion.

The operation of this lead-lag circuit is as follows.

- At lower frequencies, the lead circuit takes over due to the high reactance of C_2.
- As the frequency increases, X_{C2} decreases, thus allowing the output voltage to increase.
- At some specified frequency, the response of the lag circuit takes over, and the decreasing value of X_{C1}causes the output voltage to decrease,



(a) Circuit (b) Response curve

Figure 6 A lead-lag circuit and its response curve.

The response curve for the lead-lag circuit shown in Figure 6(b) indicates that the output voltage peaks at a frequency called the resonant frequency, f_r. At this point, the attenuation (V_{out}/V_{in}) of the circuit is 1/3 if R_1=R_2 and X_{C1} =X_{C2} as stated by the following equation

$$\frac{V_{out}}{V_{in}} = \frac{1}{3}$$

The formula for the resonant frequency is

$$f_r = \frac{1}{2\pi RC}$$

To summarize, the lead-lag circuit in the Wien-bridge oscillator has a resonant frequency, at which the phase shift through the circuit is and the attenuation is 1/3.

Below, f_r the lead circuit dominates and the output leads the input. Above, f_r the lag circuit dominates and the output lags the input.

THE BASIC CIRCUIT:

The lead-lag circuit is used in the positive feedback loop of an op-amp, as shown in Figure 7(a).

A voltage divider is used in the negative feedback loop. The Wien-bridge oscillator circuit can be viewed as a non-inverting amplifier configuration with the input signal fed back from the output through the lead-lag circuit. Recall that the voltage divider determines the closed-loop gain of the amplifier.

$$A_{cl} = \frac{1}{B} = \frac{1}{R_2/(R_1 + R_2)} = \frac{R_1 + R_2}{R_2}$$

The circuit is redrawn in Figure 7(b) to show that the op-amp is connected across the bridge circuit. One leg of the bridge is the lead-lag circuit, and the other is the voltage divider.

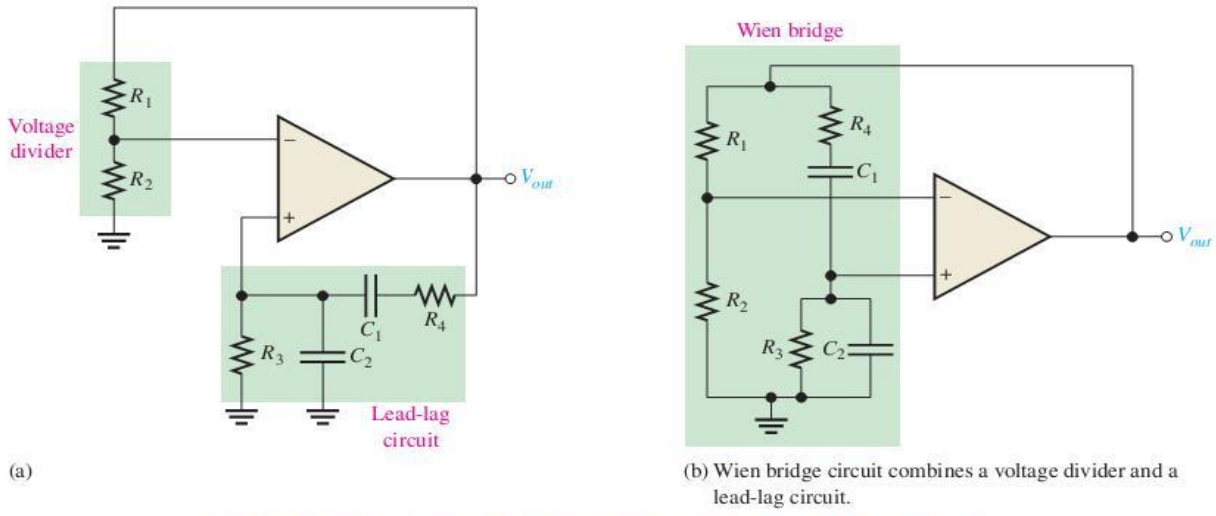
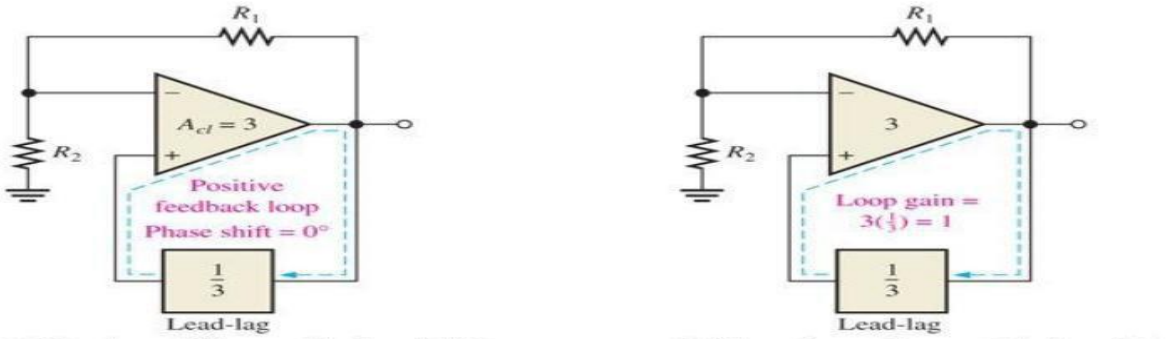


Figure 7 The Wien-bridge oscillator schematic drawn in two different but equivalent ways.

POSITIVE FEEDBACK CONDITIONS FOR OSCILLATION:

As you know, for the circuit output to oscillate, the phase shift around the positive feedback loop must be 0° and the gain around the loop must equal unity (1). The 0° phase-shift condition is met when the frequency is f_r because the phase shift through the lead-lag circuit is 0° and there is no inversion from the non-inverting input of the op-amp to the output. This is shown in Figure 8(a).



(a) The phase shift around the loop is 0°. (b) The voltage gain around the loop is 1.

Figure 8 Conditions for sustained oscillation.

The unity-gain condition in the feedback loop is met when

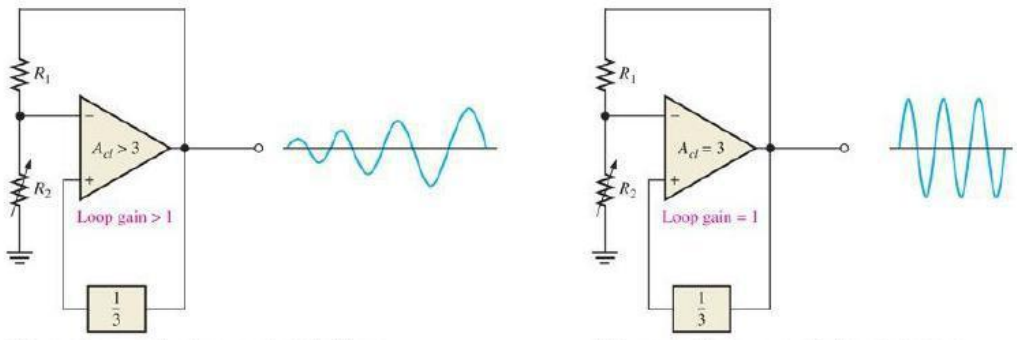
$$A_{cl} = 3$$

This offsets the 1/3 attenuation of the lead-lag circuit, thus making the total gain around the positive feedback loop equal to 1, as shown in Figure 8(b). - To achieve a closed-loop gain of 3,

$$R_1 = 2R_2$$

START-UP CONDITIONS

Initially, the closed-loop gain of the amplifier itself must be more than 3 ($A_{cl} > 3$) until the output signal builds up to a desired level. Ideally, the gain of the amplifier must then decrease to 3 so that the total gain around the loop is 1 and the output signal stays at the desired level, thus sustaining oscillation. This is illustrated in Figure 9.



(a) Loop gain greater than 1 causes output to build up. (b) Loop gain of 1 causes a sustained constant output.

Figure 9 Conditions for start-up and sustained oscillations.

Initially, a small positive feedback signal develops from noise. The lead-lag circuit permits only a signal with a frequency equal to appear in phase on the non-inverting input. This feedback signal is amplified and continually strengthened, resulting in a buildup of the output voltage. When the output signal reaches the zener breakdown voltage, the zeners conduct and effectively short out. This lowers the amplifier‟s closed-loop gain to 3. At this point, the total loop gain is 1 and the output signal levels off and the oscillation is sustained.

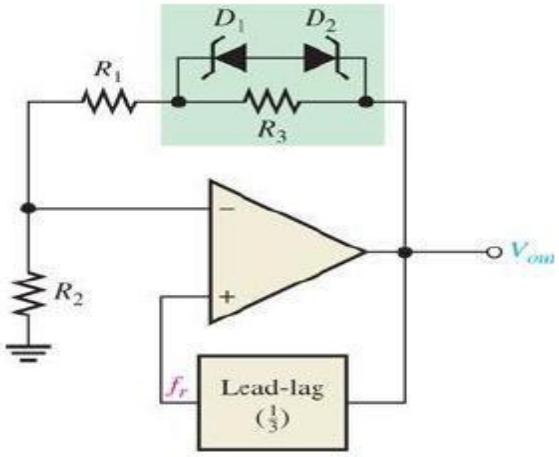


Figure 10 Self-starting Wien-bridge oscillator using back-to-back zener diodes.

PRELAB ASSIGNMENT:

Use the computer software tool Orcad PSPICE to simulate the circuit. Make sure to bring the PSPICE results to the laboratory. In addition to being an aid in immediately verifying measured results, they will be the basis of your Pre-lab grade for this lab.

Specifically, the following items must be addressed using Orcad PSPICE as part of the pre lab assignment:

- Transient response (time-domain) showing waveforms of output voltage

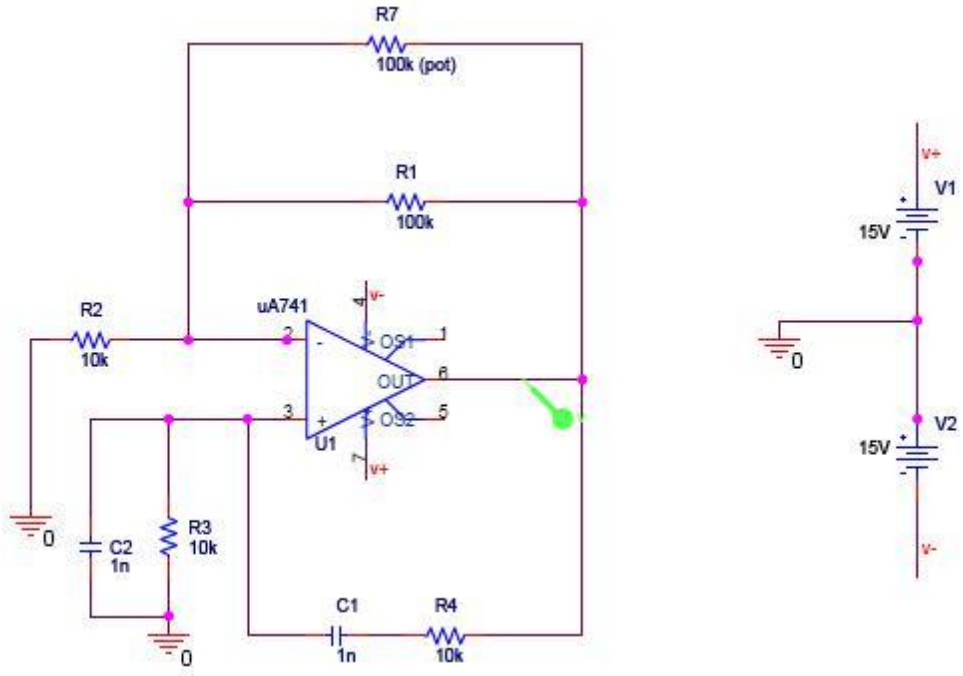


Fig. 11: Circuit to be implemented

PROCEDURE:

1. Wire the circuit
2. Apply ± 15V supply connections to the bread board.
3. Turn 100kΩ potentiometer completely clock-wise
4. Connect one probe of the oscilloscope to the output of the circuit and the second probe to the positive pin of op-amp.
5. Adjust the potentiometer to obtain a sine wave across the output.
6. Calculate the theoretical value of the frequency at which the circuit should oscillate as given by the formula.
7. Measure the oscillation frequency with an oscilloscope.

USEFUL FORMULA:

$$R_1 = 2R_2$$

$$f_r = \frac{1}{2\pi RC}$$

OBSERVATION:

Parameter	Measured	Expected	% error
R_2			
f_r			

CALCULATIONS:

RESULT:

The resonant frequency as measured comes out to be: _____
The resonant frequency as calculated comes out to be: _____
R_2 as measured comes out to be: _____
R_2 as calculated comes out to be: _____

LAB SESSION 13

To design and analyze an op-amp based Phase Shift oscillator.

Student Name: _____
Roll no.:_____ Batch: _____
Semester:_____ Year:_____

Total Marks	Marks Obtained

Remarks (if any) :_____

Instructor Name:_____

Instructor Signature:_____Date:_____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	**Extent of Achievement**				
	0	**1**	**2**	**3**	**4**
Equipment Identification Sensual ability to **identify** equipment and/or its component for a lab work	Unable to identify the equipment	Able to identify very few equipment and components to be used in lab work	Able to identify some of the equipment and components to be used in lab work	Able to identify most of the equipment and components to be used in lab work	Able to identify all of the equipment as well as its components
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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 13

OBJECTIVE:

To design and analyze an op-amp based Phase Shift oscillator.

EQUIPMENT REQUIRED:

- Proto board
- Function Generator
- Digital Multi meter
- Power Supply
- Resistors
- 5kΩ potentiometer
- Capacitors 3x0.1uF
- 741op-amp (8-pin mini DIP)

THEORY:

THE PHASE-SHIFT OSCILLATOR:

Figure 12 shows a sinusoidal feedback oscillator called the phase-shift oscillator.
Each of the three RC circuits in the feedback loop can provide a maximum phase shift approaching 90°.

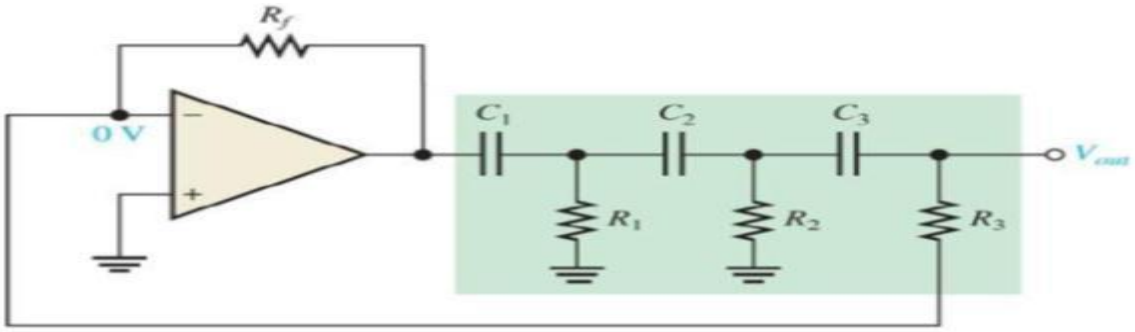

Figure 12 Phase-shift oscillator.

Oscillation occurs at the frequency where the total phase shift through the three RC circuits is 180°. The inversion of the op-amp itself provides the additional 180° to meet the requirement for oscillation of a 360° (or 0°) phase shift around the feedback loop. The attenuation, , of the three-section RC feedback circuit is

$$B = \frac{1}{29}$$

$$\text{where } B = R_3/R_f.$$

To meet the greater-than-unity loop gain requirement, the closed-loop voltage gain of the op-amp must be greater than 29 (set by $R_3$and R_f).The frequency of oscillation f_r is given as

$$f_r = \frac{1}{2\pi\sqrt{6}RC}$$

Where $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$.

PRE-LAB ASSIGNMENT:

Use the computer software tool Orcad PSPICE to simulate the circuit. Make sure to bring the PSPICE results to the laboratory. In addition to being an aid in immediately verifying measured results, they will be the basis of your Pre-lab grade for this lab.

Specifically, the following items must be addressed using Orcad PSPICE as part of the prelab assignment:

Transient response (time-domain) showing waveforms of output voltage

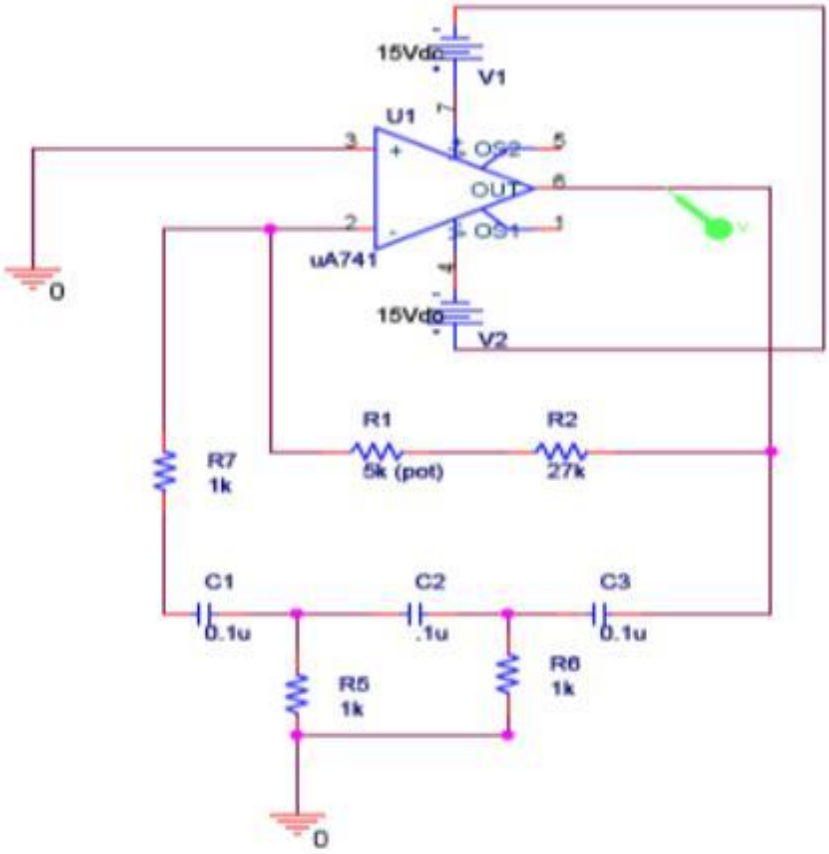

Fig. 1: Circuit to be implemented

PROCEDURE:

1. Wire the circuit
2. Apply ± 15V supply connections to the bread board.
3. Depending on the setting of the 5 kΩ potentiometer the circuit may or may not be oscillating when power is applied. If a sine wave is not displayed on the oscilloscope, carefully adjust the 5 kΩ potentiometer until a sine wave starts to appear on the oscilloscope's display.
4. On the other hand, if a sine wave is seen when power is applied on the bread board, carefully decrease the resistance of the potentiometer to obtain the best looking sine wave.
5. Measure the output frequency of the phase shift oscillator recording your result in table. Compare this value with the expected frequency found using equation.
6. Measure the value of the feedback resistance that produced maximum oscillation.

USEFUL FORMULA:

Output Frequency:

$$f_o = \frac{1}{2\Pi RC\sqrt{6}}$$

For oscillation:

$$\frac{R_f}{R} = 29$$

OBSERVATION:

Parameter	Measured	Expected	% error
Output Frequency, f_o			
R_f			

CALCULATIONS:

RESULT:

The output frequency as measured comes out to be: _____

The output frequency as calculated comes out to be: _____

R_f as measured comes out to be :_____

R_f as calculated comes out to be :_____

LAB SESSION 14

To analyze an astable multivibrator with:

- **Symmetrical square wave output**

Student Name: _____

Roll no.:_____ Batch: _____

Semester:_____ Year:_____

Total Marks	Marks Obtained

Remarks (if any) :_____

Instructor Name:_____

Instructor Signature:_____Date:_____

NED University of Engineering and Technology, Karachi
Department of Electronic Engineering

Course Code: _____ Course Name: _____

Laboratory Session No. _____ Date: _____

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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 14

OBJECTIVE:

To analyze an astable multivibrator with:

- Symmetrical square wave output

EQUIPMENT REQUIRED:

Bread Board
Resistors (1/4 Watt), Capacitor
Digital multimeter
Function generator
Oscilloscope

THEORY:

With an astable multivibrator, the op amp operates only in the non-linear region. So its output has only two voltage levels, Vmin and Vmax. The astable continually switches from one state to the other, staying in each state for a fixed length of time. The circuit of an astable multivibrator is shown in figure f7.01. Note that this circuit does not need an input signal. To find out the relations governing the operation of the astable, we start with the usual hypothesis that the operational amplifier has an ideal behavior. Suppose the output is in the state Vo = Vmax. When Vo takes this value the voltage V_{Al} of the non inverting input is:

$$V_{Al} = Vmax .R\ 1/ (R1 + R2)$$

The capacitor C starts charging through resistor R towards the value Vmax. This charging continues until the voltage V_B of the inverting input reaches the value V_{Al}. At this point, as the inverting input voltage is more than the non-inverting input, the output switches low, to Vmin. The voltage V_{A2} is now given by:

$$V_{A2}= Vmin .R1 / (R1 + R2)$$

At this point, the capacitor C starts discharging through R towards the voltage Vmin until it reaches the value V_{A2}, at which point the output switches to Vmax .The cycle then starts again.

We have seen that the voltage across the capacitor C can vary from V_{Al} to V_{A2}, so in the period of time when the output is low, at Vmin, the voltage on the capacitor is given by:

$$V_B(t)=Vmin – (Vmin-Vmax*R1/(R1 + R2))*e^{-t/R*C}$$

While in the period of time when the output is at *Vmax,* the capacitor voltage is:

$$V_B(t)=Vmax – (Vmax-Vmin*R1/(R1 + R2))*e^{-t/R*C}$$

The period T1 for which the output voltage is at *Vmax* can be found by calculating the time the capacitor voltage takes to equal V_{Al}. So:

$$Vmax/(R1+R2) = (Vmin/(R1+R2)-Vmax)*e^{-T1/R*C} + Vmax$$

From which:

$$T1=R*C*\ln \frac{Vmax-R1/(R1+R2)*Vmin}{Vmax-R1/(R1+R2)*Vmax}$$

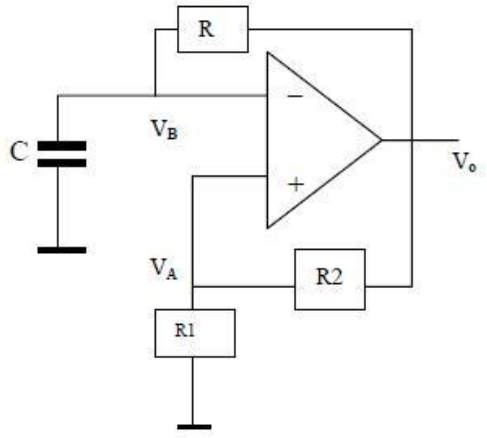
Similarly we can find the period T2 for which the output stays at *Vmin:*

$$T2=R*C*\ln \frac{Vmax*R1/(R1+R2)-Vmin}{Vmin*R1/ (R1+R2)-Vmin}$$

Supposing that *Vmin* = -*Vmax* we obtain: $T1=T2=2R*C*\ln \frac{1+R1/ (R1+R2)}{1-R1/ (R1+R2)}$

The total period *T* of the square-wave is given by the sum of *T* 1 and *T2.* We can see that the square-wave period and so the frequency can be varied by varying the values of R1, R2, R and C. To obtain an asymmetrical square-wave (duty cycle not 50%) we can make the capacitor charge and discharge through resistors of different values.

Figure
F1.1



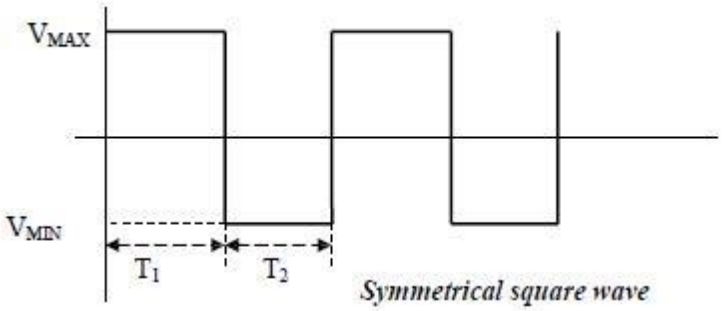


Fig F1.2

PRELAB ASSIGNMENT:

Use the computer software tool Orcad PSPICE to simulate the circuit .Make sure to bring the PSPICE results to the laboratory. In addition to being an aid in immediately verifying measured results, **they will be the basis of your Pre-lab grade for this lab.**

- Transient response (time-domain). Also mark label to the maximum output voltage (using PSpice.

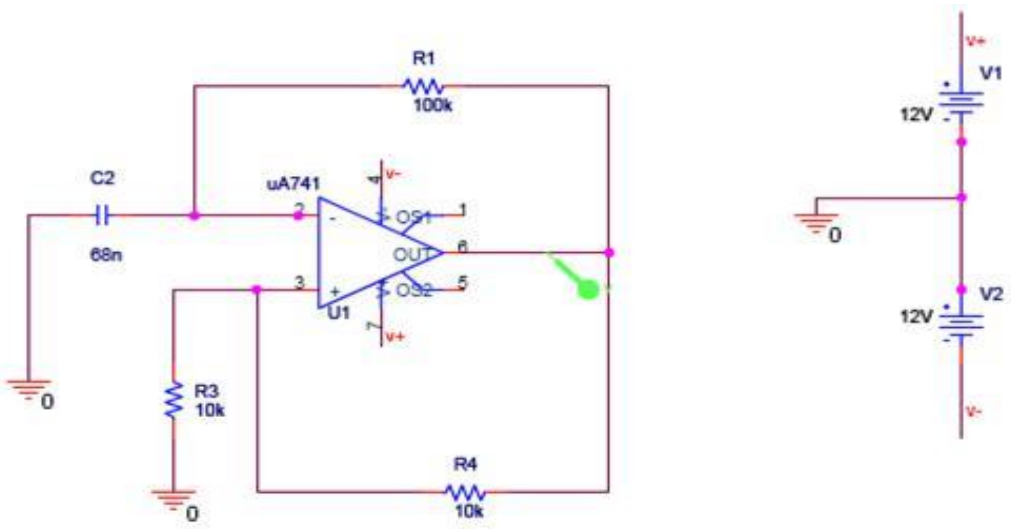


Figure F1.3

PROCEDURE:

- Implement the circuit of Figure F1.3.
- Calculate the output frequency with the formulae.
- Connect the first probe of the oscilloscope to the output V_o of the amplifier and the second probe to the inverting input V_B.
- Measure the frequency with the oscilloscope, and compare it with the theoretical result
- Calculate the capacitor voltages at which output switching occurs, according to the formulae
- Measure the capacitor voltages at which output switching occurs and compare the results with those calculated from theory.

- Calculate the values of T1 and T2 as given by the formulae.

- Measure the values of T1 and T2 with the oscilloscope.

OBSERVATION(SYMMETRICAL SQUARE WAVE):

S.NO.	Quantity	Observed Value	Calculated Value
1	$V_{B\ (P-P)}$		
2	$V_{O(P-P)}$		
3	Frequency		
4	Vmax		
5	Vmin		
6	Capacitor charging time		
7	Capacitor discharging time		

OUTCOME:

The approximate frequency of the oscillation of the astable multivibrator (Symmetrical square wave), when R1=R2=10k and R=100K, C = 68nf and Vmin = -Vmax comes out to be: $1 / T_1+T_2 =$