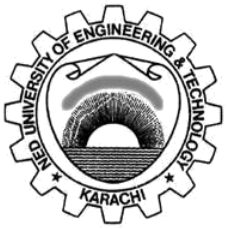

Department of Electronic Engineering

NED University of Engineering and Technology

Practical Work Book

For the course

INTEGRATED CIRCUITS
(EL-202) For S.E (EL)

Instructor Name: _____

Student Name: _____

Roll No: _____ **Batch:** _____

Semester: _____ **Year:** _____

Department: _____

LABORATORY WORK BOOK
FOR THE COURSE

EL-202 INTEGRATED CIRCUITS

Prepared and Reviewed By:
Dr. Saleha Bano (Assistant Professor)
and
Ayesha Akhtar (Lecturer)

Approved By:
Board of Studies of Department of Electronic Engineering

Integrated Circuits Laboratory Manual

CONTENTS

S.No.	List of Experiments	Weighted CLO	Sign.
1.	To OPERATE UNDER SUPERVISION the CMOS op-amp to determine CMRR.		
2.	To PRACTICE NMOS Inverter circuit with resistive load and determine the noise margin with the help of its voltage transfer characteristics.		
3.	To OPERATE UNDER SUPERVISION the NMOS Inverter to determine its average power dissipation and TRY NMOS NAND gate and NMOS NOR gate with resistive load.		
4.	To PRACTICE NMOS Inverter circuit with Enhancement load MOS and TRY the logic function $f = \overline{(a+b)c}$.		
5.	To OPERATE UNDER SUPERVISION the CMOS Inverter circuit and determine its propagation delay and power dissipation.		
6.	To PRACTICE CMOS NAND gate and CMOS NOR gate and also TRY exclusive OR-gate (XOR) function.		
7.	To OPERATE UNDER SUPERVISION SR Flip Flop and D-Flip Flop.		
8.	To OPERATE UNDER SUPERVISION JK Flip Flop and T-Flip Flop.		
9.	To OPERATE UNDER SUPERVISION the Pseudo NMOS Logic inverter and TRY complex logic function $f = \overline{A(B+CD)}$.		
10.	To OPERATE UNDER SUPERVISION pass transistor logic to implement two input AND gate and PRACTICE 2-to-1 multiplexer using CMOS transmission gates.		
11.	To OPERATE UNDER SUPERVISION the Dynamic logic circuit and PRACTICE the function $Y = \overline{A+BC}$.		
12.	To OPERATE UNDER SUPERVISION two single-input Domino CMOS logic gates connected in cascade.		
13.	Open Ended Lab		

LAB SESSION 01

OBJECTIVE:

To OPERATE UNDER SUPERVISION the CMOS op-amp to determine CMRR.

EQUIPMENT REQUIRED:

- Protoboard
- Function Generator
- Digital Multimeter
- Oscilloscope
- Op-amp IC MCP601/MCP602 : 2
- Resistors: 1K and 10K

THEORY:

The Common-Mode Rejection Ratio (CMRR) indicates the ability of a differential amplifier to suppress signals common to the two inputs. It means that any undesired (or noise) signals that appear in polarity, or common to both input terminals, will be largely rejected, or cancelled out at the differential amplifier output. It is the ratio of the differential voltage gain (A_d) to the common-mode gain (A_{cm}). This ratio is the CMRR.

$$CMRR = \frac{A_d}{A_{cm}}$$

A well-designed differential amplifier typically has a high differential gain and low common mode gain, resulting in a high CMRR. The CMRR is often expressed in decibels (dB) as:

$$CMRR = 20log\left(\frac{A_d}{A_{cm}}\right)$$

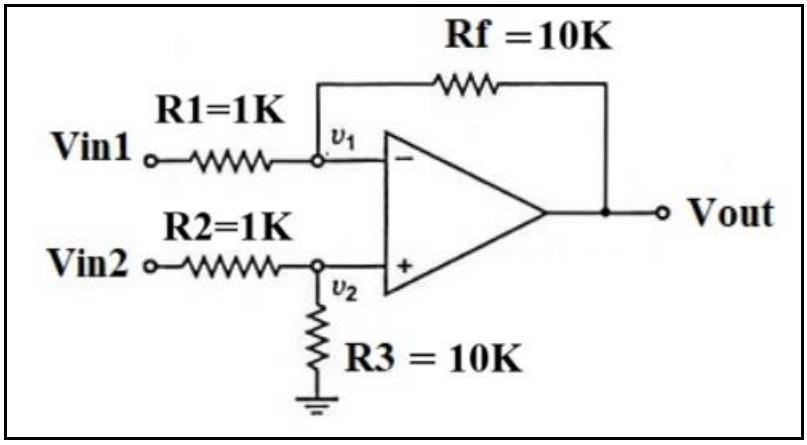

Figure 1: A CMOS op-amp circuit diagram

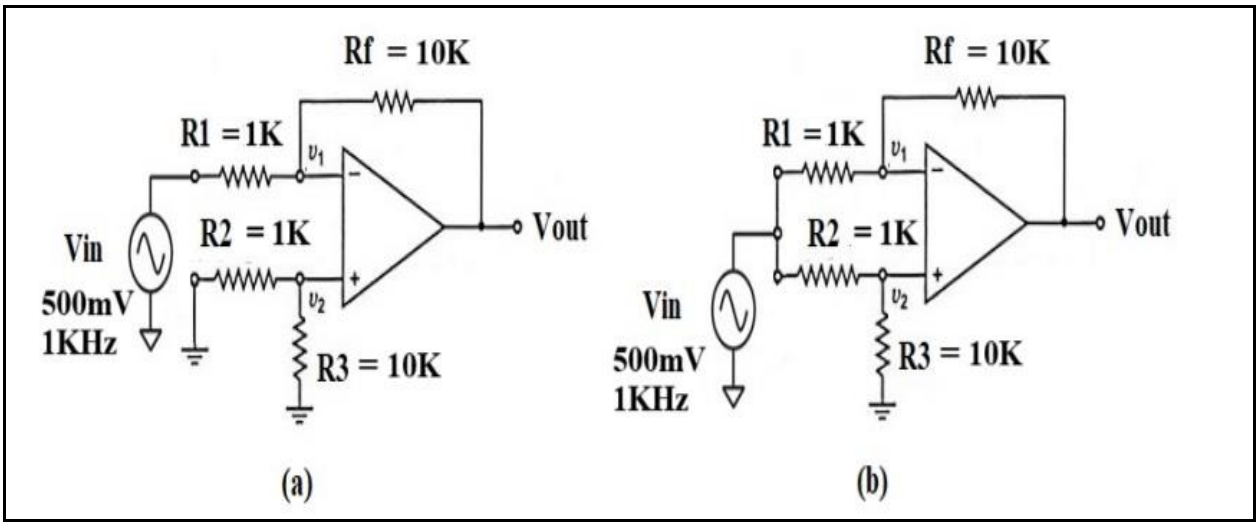

Figure 2: (a) Circuit configurations for CMRR calculation (a) differential gain (A_d) measurement and (b) common-mode gain (A_C) measurement

PROCEDURE:

1. Assemble the op-amp shown in Figure 1 on the breadboard. Provide +/-5V to the op-amp.
2. Connect one of the op-amp inputs to a function generator and ground the other input as shown in Figure 2(a) and find the differential gain (Ad) of the op-amp.
3. Connect the op-amp in common mode configuration providing or shorting both op-amp inputs to a signal generator as shown in Figure 2(b) and find the common-mode gain (Ac) of the op-amp.
4. Note down the observed values in the given Table 1.
5. Calculate the CMRR.

OBSERVATIONS:

Table 1: For CMRR of CMOS op-amp

Quantity	Observed value
Ad	
Acm	
CMRR	

CALCULATIONS:

RESULTS:

Differential gain of CMOS op-amp is: _____
Common mode gain of CMOS op-amp is: _____
CMRR of CMOS op-amp is: _____

NED University of Engineering & Technology
Department of Electronic Engineering
Course Code and Title: EL-202 Integrated Circuits

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Remarks	
Instructor's Signature with Date:	

LAB SESSION 02

OBJECTIVE:

To PRACTICE NMOS Inverter circuit with resistive load and determine the noise margin with the help of its voltage transfer characteristics.

EQUIPMENT REQUIRED:

- Protoboard
- Variable Power Supply
- Digital Multimeter
- NMOS transistors 2N7000: 1
- Resistors: 1K
- LED

THEORY:

The basic transistor level realization of an inverter using an N-channel MOS transistor and a resistor is shown in the Figure 1. Here, enhancement type NMOS acts as the driver transistor. The load consists of a simple linear resistor R_L. The power supply of the circuit is $V_{DD.}$
When the transistor is used as an inverter, the transistor is either cut-off and has a large voltage between its drain and source, or operates in triode region where its drain to source voltage is very small.

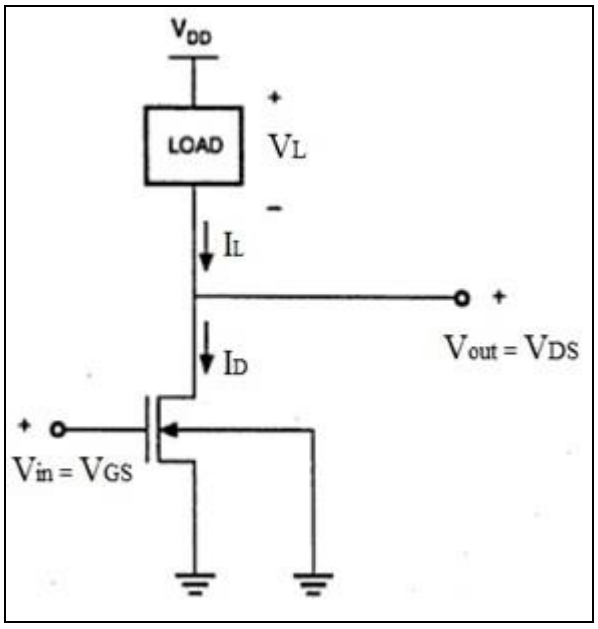

Figure 1: NMOS Inverter

When the input of the driver transistor is less than threshold voltage V_{TH} ($V_{in} < V_{TH}$), driver transistor is in the cut – off region and does not conduct any current. So, the voltage drop across the load resistor is ZERO and output voltage is equal to the V_{DD}. The transistor is equivalent to

an open switch. Similarly, when input of the driver transistor is greater than the threshold voltage V_{TH} ($V_{in} > V_{TH}$), the transistor is ON and connects the drain to source which is equivalent to a close switch and pulls the output voltage down to 0V.

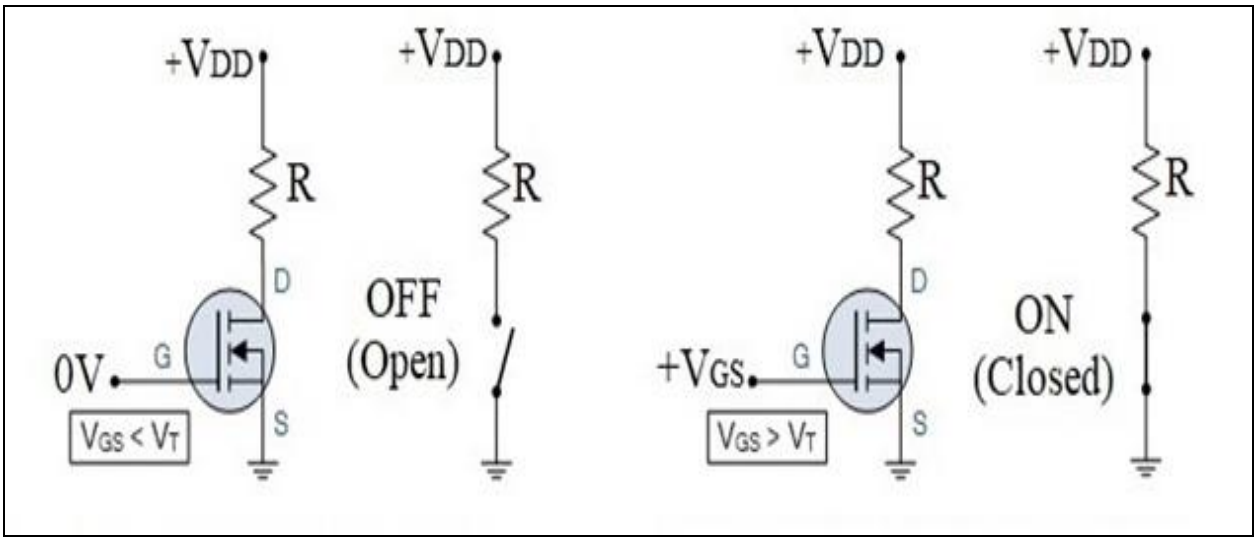

Figure 2: (a) NMOS biased OFF (b) NMOS biased ON

Noise Margin:

Noise margin is the amount of noise that a NMOS circuit could withstand without compromising the operation of circuit. It essentially represents the inverter's robustness against noise. Noise margin is typically divided into low noise margin (NML) and high noise margin (NMH).

NML (Low Noise Margin):

NML is defined as the difference between the maximum low input voltage (VIL) recognized by the receiving gate and the maximum low output voltage (VOL) produced by the driving gate. A larger NML means the inverter is more tolerant to noise when the output is intended to be low.

The low-side noise margin is:

$$NML = VIL - VOL$$

NMH (High Noise Margin):

NMH is defined as the difference between the minimum high output voltage (VOH) of the driving gate and the minimum high input voltage (VIH) recognized by the receiving gate. A larger NMH means the inverter is more tolerant to noise when the output is intended to be high.

The high-side noise margin is:

$$NMH = VOH - VIH$$

Figure 3 shows the voltage transfer characteristics (VTC) of the logic inverter, voltage levels, logic states and noise margins. Voltages between VIL and VIH are in the undefined range. If they are applied to a logic gate, the output cannot be predicted with certainty.

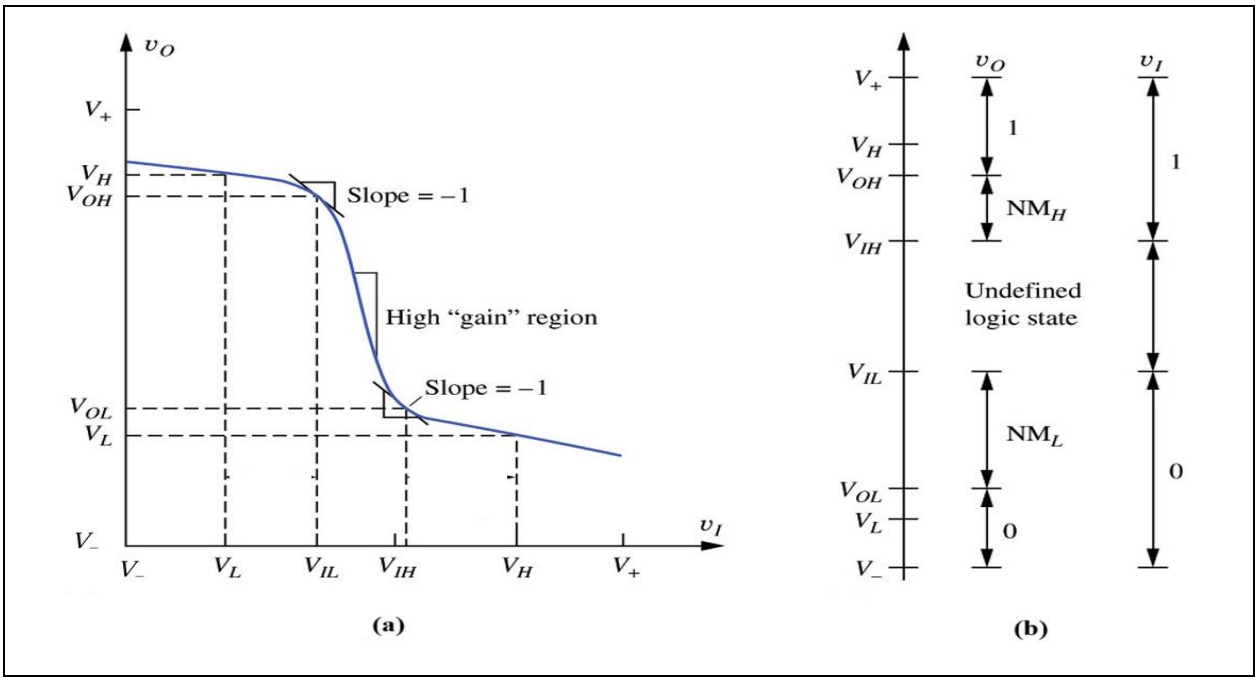

Figure 3: (a) Voltage Transfer Characteristics of NMOS inverter (b) Voltage levels & Noise Margins

The points, where the slope are -1, are important on the voltage transfer characteristics. These points specify the limits of the voltage ranges used to specify Logic 0 and logic 1.

PROCEDURE:

1. Connect the circuit on breadboard according to the given Figure 1 for implementing NMOS inverter and note down the observed values in Table 1. Provide +5V to the circuit.
2. To observe the voltage transfer characteristics (VTC), vary the input voltage of NMOS inverter from 0V to 5V in 0.1V steps and measure the corresponding Vout with the help of digital multimeter (DMM).
3. Note down the observed input (Vin) and Output (Vout) voltages in Table 2 and sketch the VTC in Figure 4.
4. Note down the values of VIL, VOL, VIH and VOH in Table 3.
5. Calculate the noise margin NMH and NML.

Table1: For NMOS Inverter

Vin (Input)	Vout (Output)
0V	
5V	

Table 2: For Voltage Transfer Characteristics (VTC)

Input Voltage (Vin)	Output Voltage (Vout)	Input Voltage (Vin)	Output Voltage (Vout)	Input Voltage (Vin)	Output Voltage (Vout)
0		1.7		3.4	
0.1		1.8		3.5	
0.2		1.9		3.6	
0.3		2		3.7	
0.4		2.1		3.8	
0.5		2.2		3.9	
0.6		2.3		4	
0.7		2.4		4.1	
0.8		2.5		4.2	
0.9		2.6		4.3	
1		2.7		4.4	
1.1		2.8		4.5	
1.2		2.9		4.6	
1.3		3		4.7	
1.4		3.1		4.8	
1.5		3.2		4.9	
1.6		3.3		5	

Table 3: For Noise Margin

Voltage Levels	Observed values
VIL	
VOL	
VIH	
VOH	
NML	
NMH	

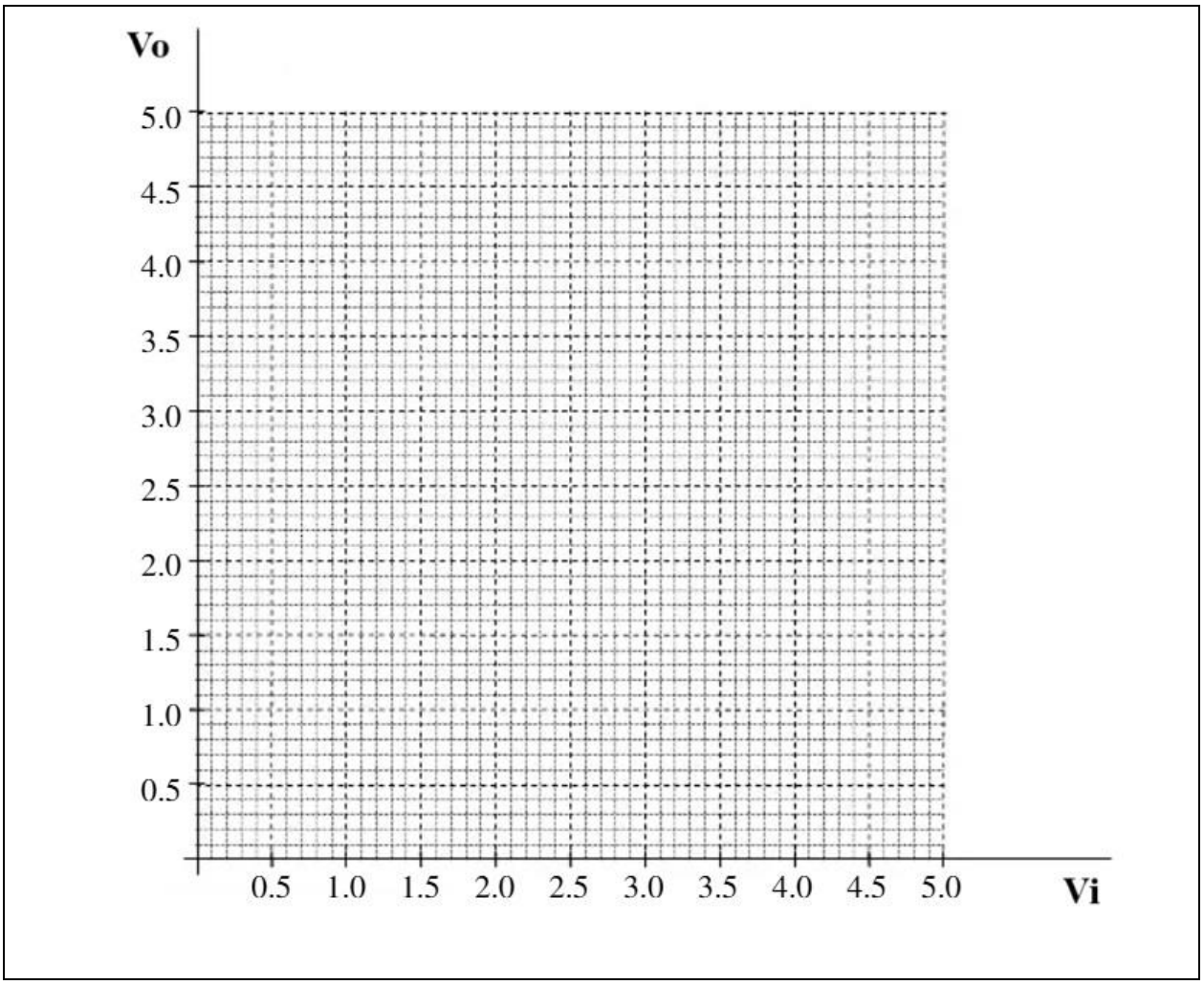

Figure 4: Voltage Transfer Characteristics of NMOS inverter

CALCULATIONS:

RESULTS:

Noise Margin low of NMOS (NML) inverter is: _____
Noise Margin high of NMOS (NMH) inverter is: _____

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Department of Electronic Engineering
Course Code and Title: EL-202 Integrated Circuits

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Laboratory Session No. _____ Date: _____

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 03

OBJECTIVE:

To OPERATE UNDER SUPERVISION the NMOS Inverter to determine its average power dissipation and TRY NMOS NAND gate and NMOS NOR gate with resistive load.

EQUIPMENT REQUIRED:

- Protoboard
- Variable Power Supply
- Digital Multimeter
- NMOS transistors 2N7000: 5
- Resistors: 1K
- LED

THEORY:

An NMOS inverter with resistive load and its voltage transfer characteristics are shown in Figure 1(a) and Figure 1(b) respectively.

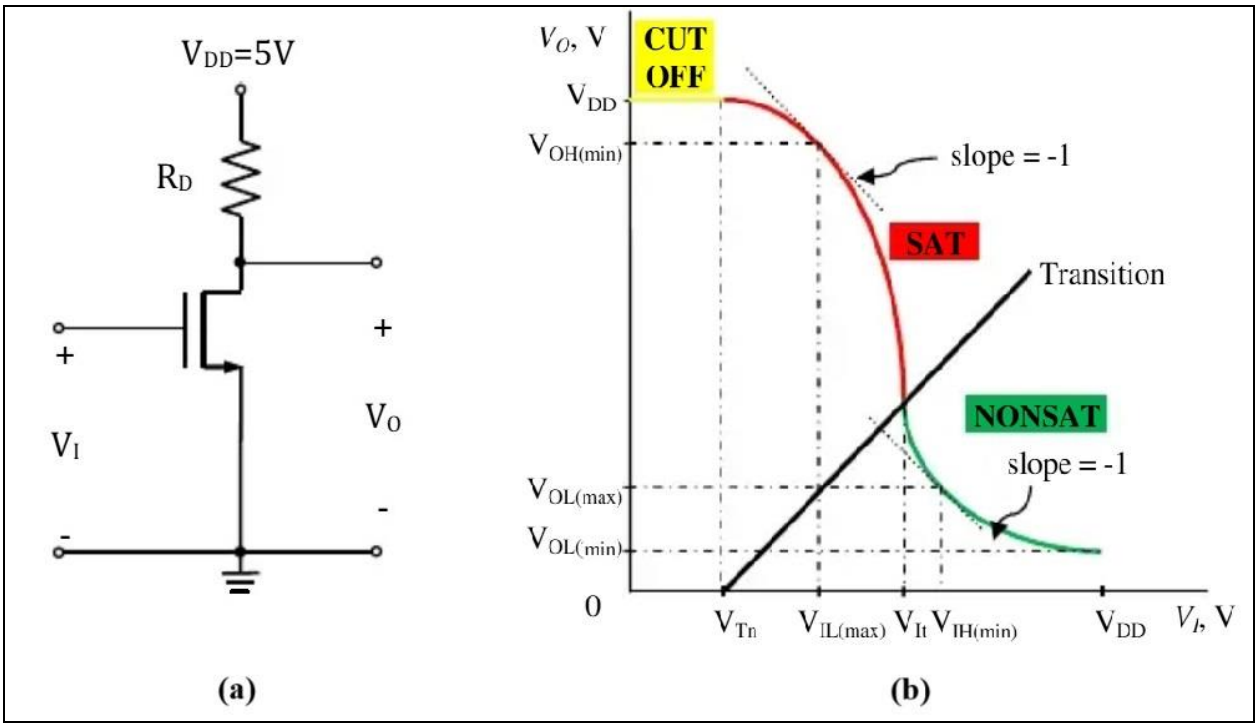

Figure 1: (a) NMOS inverter with resistive load (b) Voltage Transfer Characteristics of NMOS inverter

The average power dissipated in the NMOS logic gate is calculated assuming half of the period, input is high (output is low) and during the other half input is low (output is high). When the

output is high (Vin = 0 V), the output current is zero, $I_{D(OH)}$ = 0 V, since the transistor is off. For Vin = 5 V, the output is low ($V_{OL(min)}$ as shown in the above characteristic curve) and the current through it is:

$$I_{D(OL)} = \frac{V_{DD} - V_{OL}}{R_D}$$

Then the average current is:

$$I_{D(avg)} = \frac{I_{D(OL)} + I_{D(OH)}}{2}$$

and the average power dissipation is:

$$P_{D(avg)} = V_{DD}.I_{D(avg)}$$

PROCEDURE:

1. Connect the circuit on breadboard according to the given Figure 1(a) for implementing NMOS inverter with resistive load. Provide +5V to the circuit.
2. Apply a stable input (0/1) to the input of the NMOS inverter.
3. Use a Digital Multimeter (DMM) to find V_{OL} and calculate $I_{D(OL)}$ and $I_{D(avg)}$.
4. Calculate the average power dissipation ($P_{D(avg)}$) and note down the value in Table 1.
5. For implementing NAND gate, connect two transistors in series and note down the observed value in Table 2.
6. For implementing NOR gate, connect two transistors in parallel and note down the observed value in Table 2.

OBSERVATIONS:

Table 1: For Average Power Dissipation of NMOS Inverter

Average Current and Power	Observed Values
$I_{D(avg)}$	
$P_{D(avg)}$	

Table 2: For NAND and NOR gate

NAND GATE			NOR GATE		
Vin		Vout	Vin		Vout
0V	0V		0V	0V	
5V	0V		5V	0V	
0V	5V		0V	5V	
5V	5V		5V	5V	

CALCULATIONS:

RESULTS:

Average Power dissipation of NMOS inverter is: _____

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Department of Electronic Engineering
Course Code and Title: EL-202 Integrated Circuits

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LAB SESSION 04

OBJECTIVE:

To PRACTICE NMOS Inverter circuit with Enhancement load MOS and TRY the logic function $f = \overline{(a+b)c}$.

EQUIPMENT REQUIRED:

- Protoboard
- Power Supply
- Digital Multimeter
- Oscilloscope
- NMOS transistors 2N7000: 6
- LED

THEORY:

NMOS inverter using enhancement type NMOS transistor as load is shown in Figure 1. The NMOS load transistor is operated in saturation region. Its gate and drain are shorted together and connected to a supply voltage VDD. When the input to the inverter is at logic low, the driver NMOS transistor is turned off and the output is at logic high through the load transistor. Conversely, when the input is at logic high, the driver NMOS transistor is turned on connecting the output to ground through the driver transistor.

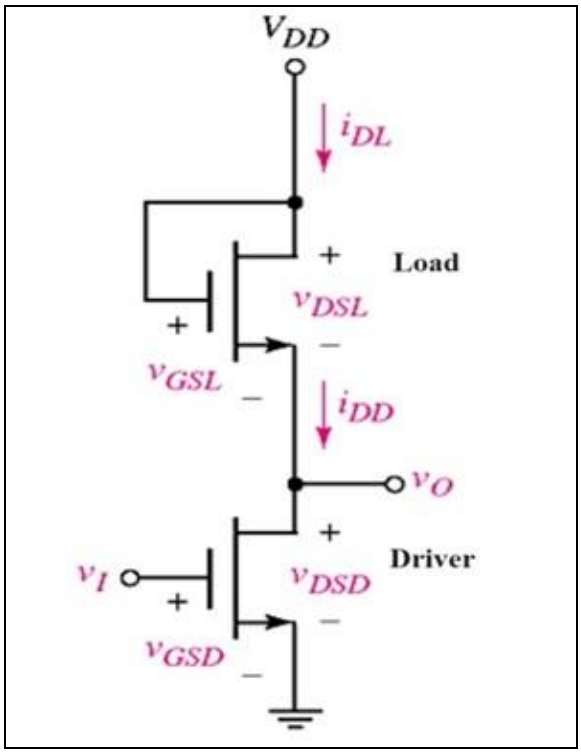

Figure 1: NMOS Inverter with Enhancement load

NMOS transistor with resistive load offers an advantage over resistive loads in terms of area efficiency but it can result in significant static power dissipation.

PROCEDURE:

1. For implementing NMOS inverter with Enhancement load MOS connect the circuit on breadboard according to the given Figure 1 and note down the observed values in Table 1. Provide +5V to the circuit.
2. For implementing the given logic function $f = \overline{(a+b)c}$, connect two transistors in parallel with input a and b.
3. Then connect a transistor with input c in series with the two parallel transistors having inputs a and b connected above.
4. Now note down the observed value in Table 2.

OBSERVATIONS:

Table 1: For NMOS Inverter with Enhancement Load MOS

Vin	Vout
0V	
5V	

Table 2: For $f = \overline{(a+b)c}$

$f = \overline{(a+b)c}$			
a	***b***	***c***	***f***

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LAB SESSION 05

OBJECTIVE:

To OPERATE UNDER SUPERVISION the CMOS Inverter circuit and determine its propagation delay and power dissipation.

EQUIPMENT REQUIRED:

- Protoboard
- Function Generator
- Oscilloscope
- Power Supply
- Digital Multimeter
- NMOS transistor 2N7000/IRF540 : 2
- PMOS transistor IRF9540 : 2
- Capacitor: 0.1uF and 1uF

THEORY:

The CMOS circuit implementation is shown in Figure 1. It consists of an NMOS transistor *QN* and a PMOS transistor *QP*, with the gate terminals connected together to constitute the inverter input terminal, to which a logic input *X* is applied. Also, both drain terminals are connected together to constitute the inverter output terminal on which the output logic variable *Y* appears.
When $X = 1$ that is, $VX = VDD$, the PMOS transistor will be off but the NMOS transistor will be on and will be connecting the inverter output terminal to ground through the small on-resistance *R*on. Thus, the output voltage will be zero and $Y = 0$. When $X = 0$, that is, $VX = 0$, as shown in Figure 1(b), the NMOS transistor will be off but the PMOS transistor will be on and will be connecting the output terminal to *VDD* through the small resistance *R*on. Thus the output voltage will be equal to *VDD* and *Y* will be 1.

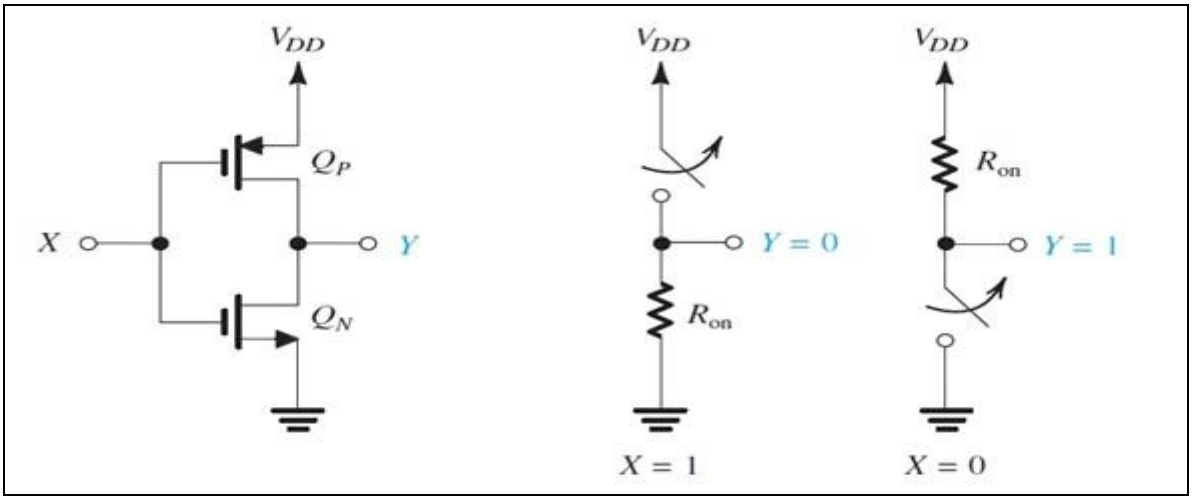

Figure 1: (a) CMOS inverter (b) Operation when input is at logic 1 and 0

Propagation Delay:

The propagation delay (tp) of a gate is defined as the time taken by a gate to respond when there is change at its inputs. It expresses the delay experienced by a signal when passing through a gate. It is measured between the **50%** transition points of the input and output waveforms as shown in Figure 2 for an inverter.

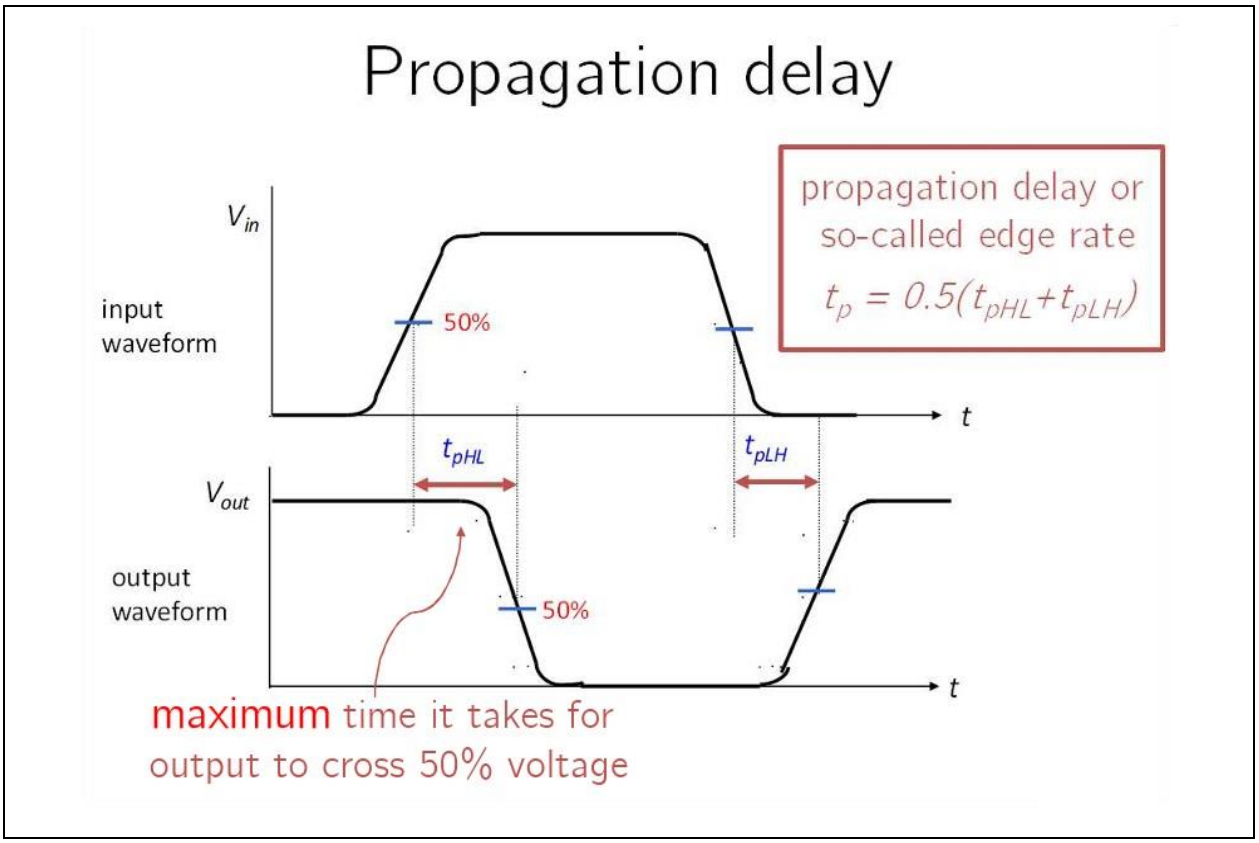

Figure 2: Propagation delay of CMOS Inverter

Propagation Delay from High to Low (tpHL):

This delay is the time it takes for the output to respond when the input switches from high to low. More specifically, it measures how long it takes the output to fall to **50%** of its full value after the input starts changing. The smaller this delay, the faster the inverter reacts to a falling edge input.

Propagation Delay from Low to High (tpLH):

This is similar to tpHL but in the opposite direction. It measures how long it takes for the output to rise to **50%** when the input goes from low to high. Again, shorter delay times mean the inverter can keep up with faster signal changes.

Total Propagation Delay (tp):

The total propagation delay is found by taking the average of tpHL and tpLH which represents the overall delay of the inverter.

$$t_P = \frac{(tpHL + tpLH)}{2}$$

This value gives you a good overall sense of how quickly the inverter reacts to any change, whether the input rises or falls.

Power Dissipation of CMOS Inverter:

Power dissipation in CMOS circuits comes from two components:

- Static Power Dissipation
- Dynamic Power Dissipation

Static Power Dissipation:

The power lost due to current leakage during which the circuit is dormant is referred to as a static power. This is caused by leakage currents, which are small currents flowing even when the transistors are in the cutoff region. Static power dissipation can be calculated as:

$$P_{static} = I * V_{DD}$$

Dynamic Power Dissipation:

The power consumed by the circuit when it is performing computational task is known as dynamic power. This power dissipation occurs when the inverter switches, causing the load capacitance (C_L) to charge and discharge as shown in Figure 3.

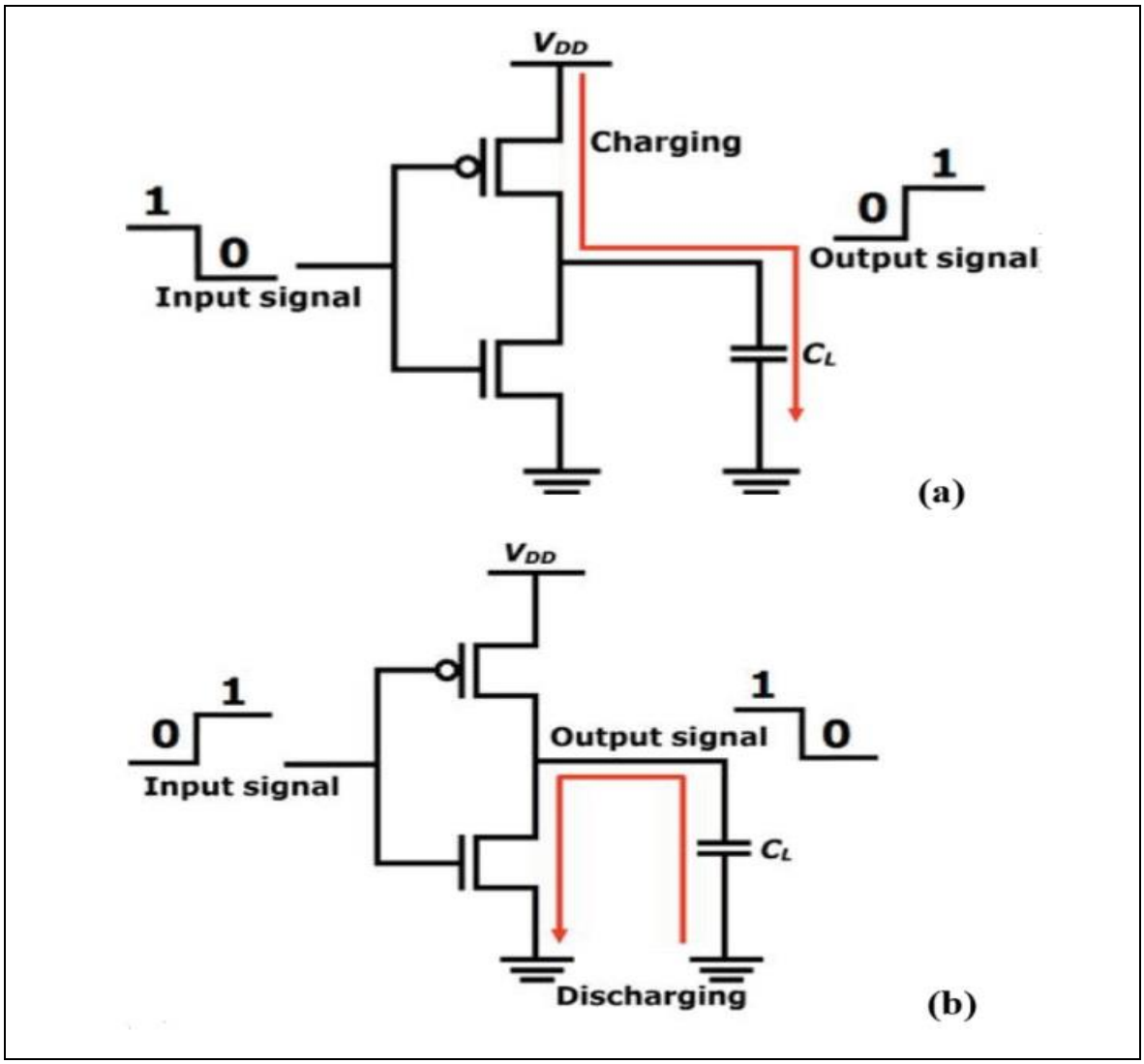

Figure 3: (a) Charging path (V_{DD} to C_L) (b) Discharging path (C_L to GND) in CMOS circuit

Whenever the input signal of the circuit changes its state with time, it causes some power dissipation. Dynamic power is required to charging and discharging the load capacitance when transistor input switches. When the input switches from 1 to 0 the PMOS transistor (PULL UP network) turns ON and charges the load to VDD. And that time energy stored in the capacitance is:

$$E_C = \frac{1}{2} C_L V_{DD}^2$$

The energy delivered from the power supply is:

$$E_C = C_L V_{DD}^2$$

Observed that only half of the energy from the power supply is stored in the capacitor. The other half is dissipated (converted to heat) in the PMOS transistor because transistor has a voltage across it at the same time current flows through it. The dissipated power depends on only the load capacitance not on transistor or speed at which the gate switches.

When the input switches from 0 to 1, the PMOS transistor turns off and the NMOS transistor is turned ON, and discharging the capacitor. The energy stored in the capacitor is dissipated in the NMOS transistor. No energy is drawn from the power supply in this case.
Depending upon the inputs at the gate of the transistor one gate is on the other is off because of charging and discharging of the capacitor. On rising edge output change $Q = C_L V_{DD}$ is required to charge the output node to V_{DD} (i.e. cap is charged to V_{DD}) and on falling edge the load capacitance is discharged to GND.
Now suppose gate switches at some average frequency f_{sw} (switching frequency). Over the time period T, the load is charging and discharging. So average power dissipation is:

$$P_{dynamic} = C_L V_{DD}^2 f_{sw}$$

This is called dynamic power because it arises from the switching of the load.
The total power dissipation can be calculated as:

$$P_{total} = P_{static} + P_{dynamic}$$

PROCEDURE:

For CMOS Inverter:

1. Connect the circuit on breadboard according to the given Figure 1(a) for implementing CMOS inverter. Provide +5V to the circuit.
2. Note down the observed values in Table 1.

For Propagation Delay:

1. Connect the circuit on breadboard according to the given Figure 3 for implementing CMOS inverter with the load capacitor of 0.1uF. Provide +5V V_{DD} to the circuit.
2. Apply 5V peak to peak square wave with 1 KHz frequency at the input of the CMOS inverter.
3. Observe the propagation delay directly on the oscilloscope by connecting both the input and output simultaneously.
4. Note down the values of tpHL, tpLH and tp in Table 2.
5. Observe how increasing the output load capacitance (0.1uF and 1uF) affects the propagation delay.

For Power Dissipation:

Static Power:

1. Connect the circuit on breadboard according to the given Figure 3 for implementing CMOS inverter. No need to connect a load capacitor. Provide +5V V_{DD} to the circuit.
2. Apply a stable input (0/1) to the input of the CMOS inverter.
3. Use a Digital Multimeter (DMM) in series with the power supply to measure the static current drawn from the supply.
4. Calculate the static power dissipation and note down the value in Table 3.

Dynamic Power:

1. Connect the circuit on breadboard according to the given Figure 3 for implementing CMOS inverter with a load capacitor of 1uF. Provide +5V V_{DD} to the circuit.
2. Apply 5V peak to peak square wave with 500 Hz frequency at the input of the CMOS inverter.
3. Calculate the dynamic power and total power dissipation of CMOS inverter and note down the values in Table 3.
4. Observe how the dynamic power increases with increase in input frequency (500 Hz and 1 KHz).

OBSERVATIONS:

Table1: For CMOS Inverter

X (Input)	Y (Output)
0V	
5V	

Table 2: For Propagation Delay of CMOS Inverter

Capacitor (0.1uF)		Capacitor (1uF)	
Propagation delay	**Observed Values**	**Propagation delay**	**Observed Values**
tpHL		tpHL	
tpLH		tpLH	
tp		tp	

Table 3: For Power Dissipation of CMOS Inverter

Frequency (500 Hz)		Frequency (1 KHz)	
Power Dissipation	**Observed Values**	**Power Dissipation**	**Observed Values**
P_{static}		P_{static}	
$P_{dynamic}$		$P_{dynamic}$	
P_{total}		P_{total}	

CALCULATIONS:

RESULTS:

Total propagation delay of CMOS inverter for 0.1uF and 1uF is: _____
Total Power dissipation of CMOS inverter for 500 Hz and 1 KHz is: _____

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Department of Electronic Engineering
Course Code and Title: EL-202 Integrated Circuits

Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	Extent of Achievement				
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Equipment Identification Sensory skill to ***identify*** equipment and/or its component for a lab work.	Not able to identify the equipment.	--	--	--	Able to identify equipment as well as its components.
Equipment Use Sensory skills to ***demonstrate*** the use of the equipment for the lab work.	Doesn't demonstrate the use of equipment.	Slightly demonstrates the use of equipment.	Somewhat demonstrates the use of equipment.	Moderately demon strates the use of equipment.	Fully demonstrates the use of equipment.
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Response Ability to ***imitate*** the lab work on his/her own.	Not able to imitate the lab work.	Able to slightly imitate the lab work.	Able to somewhat imitate the lab work.	Able to moderately imitate the lab work.	Able to fully imitate the lab work.
Observation's Use ***Displays*** skills to use the observations from lab work for experimental verifications and illustrations.	Not able to use the observations from lab work for experimental verifications and illustrations.	Slightly able to use the observations from lab work for experimental verifications and illustrations.	Somewhat able to use the observations from lab work for experimental verifications and illustrations.	Moderately able to use the observations from lab work for experimental verifications and illustrations.	Fully able to use the observations from lab work for experimental verifications and illustrations.
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Equipment Handling ***Equipment care*** during the use.	Doesn't handle equipment with required care.	Rarely handles equipment with required care.	Occasionally handles equipment with required care.	Often handles equipment with required care.	Handles equipment with required care.
Group Work ***Contributes*** in a group based lab work.	Doesn't participate and contribute.	Slightly participates and contributes.	Somewhat participates and contributes.	Moderately participates and contributes.	Fully participates and contributes.

Laboratory Session No. _____ Date: _____

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 06

OBJECTIVE:

To PRACTICE CMOS NAND gate and CMOS NOR gate and also TRY exclusive OR-gate (XOR) function.

EQUIPMENT REQUIRED:

- Protoboard
- Function Generator
- Digital Multimeter
- Power Supply
- NMOS transistor 2N7000/IRF540 : 8
- PMOS transistor IRF9540 : 8
- LED

THEORY:

The CMOS logic gate consists of two networks: the pull-down network (PDN) constructed of NMOS transistors, and the pull-up network (PUN) constructed of PMOS transistors as shown in Figure 1. The two networks are operated by the input variables, in a complementary fashion.

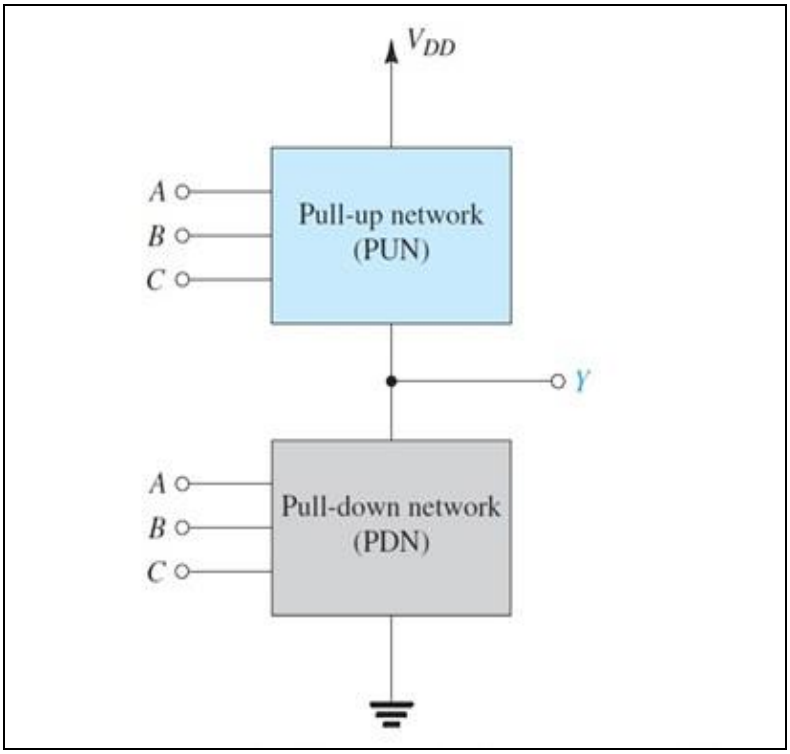

Figure 1: Representation of CMOS logic gate PUN comprises of PMOS transistor and PDN comprises of NMOS transistor

From the CMOS gate circuits, we observe that the PDN and the PUN are dual networks: Where a series branch exists in one, and a parallel branch exists in the other. Figure 2 shows a CMOS NAND gate and a CMOS NOR gate.

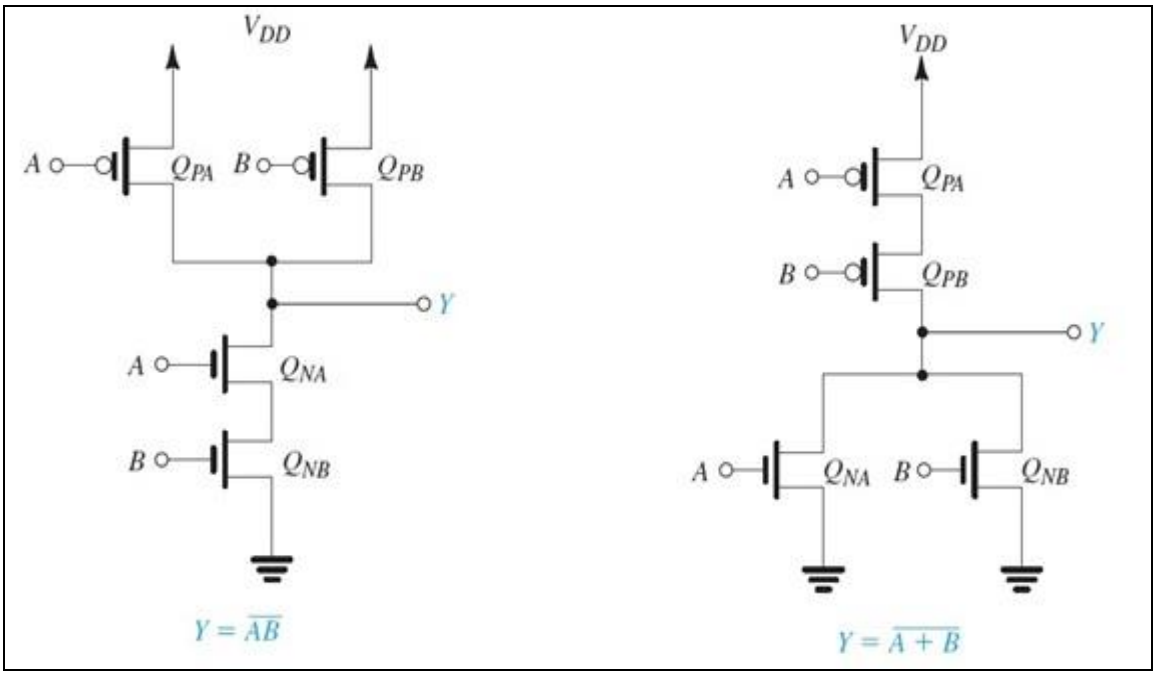

Figure 2: (a) A two input CMOS NAND gate (b) A two input CMOS NOR gate

An important function that often arises in logic design is the exclusive-OR (XOR) function,

$$\boldsymbol{Y = A\bar{B} + \bar{A}B} \qquad \textbf{(Equation 1)}$$

Here, Y (rather than $\bar{Y}$) is given, it is easier to synthesize the PUN. However, that unfortunately Y is not a function of the complemented variables only (as we would like it to be). Thus, there will be a need of additional inverters. The PUN obtained directly from Equation 1 is shown in Figure 2(a). Note that the Q1, Q2 branch realizes the first term ($A\bar{B}$), whereas the Q3, Q4 branch realizes the second term ($\bar{A}B$). Note also the need for two additional inverters to generate $\bar{A}$ and $\bar{B}$. As for synthesizing the PDN, it can be obtained as the dual network of the PUN in Figure 2(a). Alternatively, we can develop an expression for Y and use it to synthesize the PDN. Here, the direct synthesis approach is utilized. DeMorgan's law can be applied to the expression in Equation 1 to obtain $\bar{Y}$ as:

$$\boldsymbol{\bar{Y} = AB + \bar{A}\bar{B}} \qquad \textbf{(Equation 2)}$$

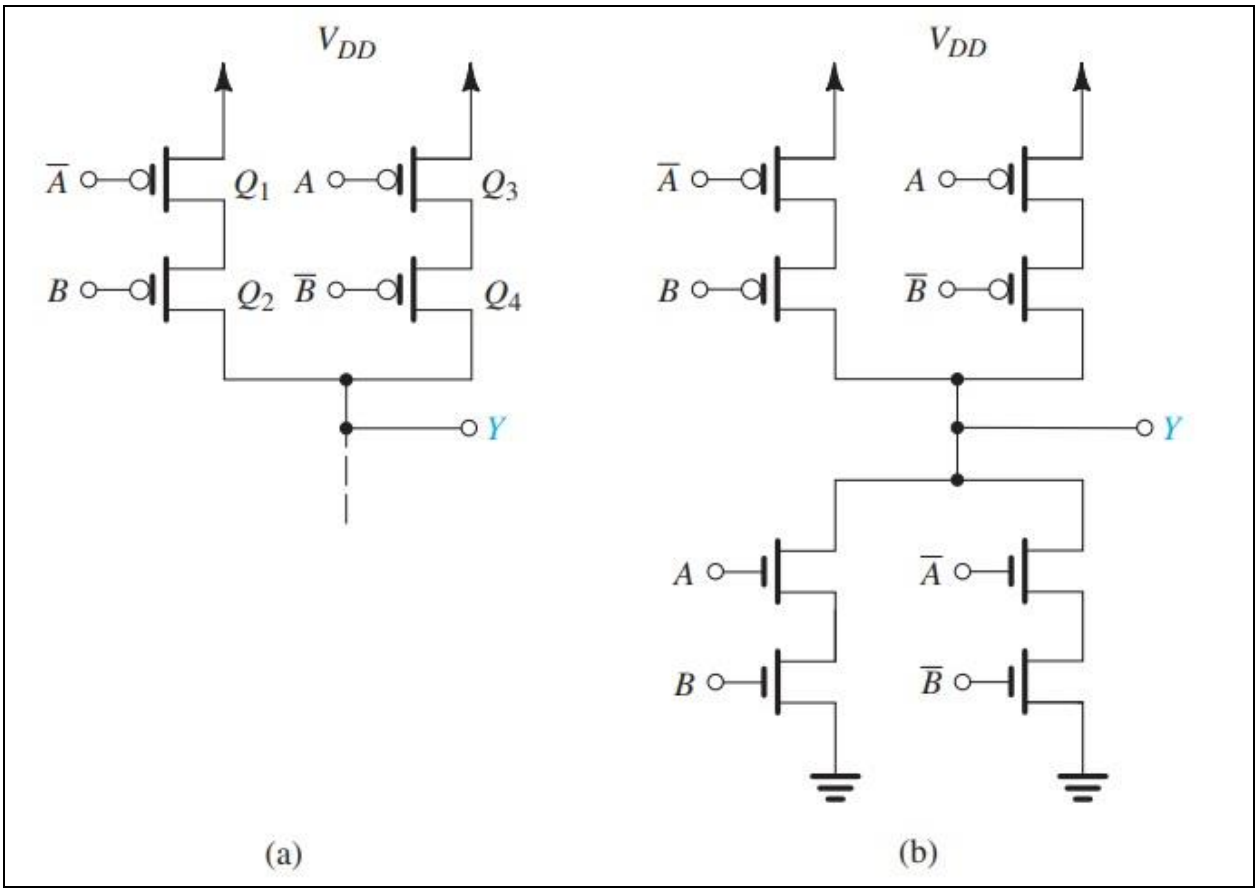

Figure 3: Realization of exclusive-OR function (a) PUN synthesized directly from Equation 1 (b) Complete XOR realization utilizing PUN from equation 1 and PDN from Equation 2

An interesting observation follows from the circuit in Figure 3(b). The PDN and the PUN here are not dual networks. Indeed, duality of the PDN and the PUN is not a necessary condition. Thus, although a dual of PDN (or PUN) can always be used for PUN (or PDN), the two networks are not necessarily duals.

PROCEDURE:

1. Connect the circuit on breadboard according to the given Figure 2 for implementing CMOS logic gates. Provide +5V to the circuit.
2. For implementing NAND gate, connect the PDN with two NMOS transistors in series with A and B as the inputs and the PUN with two parallel PMOS transistors with A and B applied to their gates as inputs. Putting PDN and PUN together results in the CMOS NAND gate implementation as shown in Figure 2(a).
3. For implementing NOR gate, connect the PDN with two parallel NMOS devices with *A* and *B* as inputs and the PUN with two series PMOS devices with A and B as the inputs. Putting the PDN and the PUN together results in CMOS NOR gate implementation as shown in Figure 2(b).
4. Now note down the observed value of CMOS NAND and NOR gate in Table 1.

5. Connect the circuit on breadboard according to the given Figure 3(b) for implementing CMOS XOR function and note down the observed values in Table 2. Provide +5V to the circuit.

OBSERVATIONS:

Table 1: For CMOS NAND and NOR gate

CMOS NAND GATE			CMOS NOR GATE		
A	**B**	**Y**	**A**	**B**	**Y**
0V	0V		0V	0V	
5V	0V		5V	0V	
0V	5V		0V	5V	
5V	5V		5V	5V	

Table 2: For CMOS exclusive-OR gate (XOR)

A (Input)	B (Input)	Y (Output)
0V	0V	
0V	5V	
5V	0V	
5V	5V	

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Laboratory Session No. _____ Date: _____

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 07

OBJECTIVE:

To OPERATE UNDER SUPERVISION SR Flip flop and D-Flip flop.

EQUIPMENT REQUIRED:

- Breadboard
- Power Supply
- IC SN74HC00N (Quadruple 2-input positive-NAND gates)
- IC HEF4013B (Dual D flip-flop)
- LM7805
- Switches
- Supply
- LEDS
- Resistor sheet
- Connecting wires

THEORY:

A flip-flop is a device designed to store a single bit of binary data, essentially functioning as a basic memory element. It maintains its state (0 or 1) until it receives a specific input signal that prompts it to change. Flip flops have two stable states and hence they are bistable multivibrators. The two stable states are High (logic 1) and Low (logic 0). The term "Flip-flop" relates to the actual operation of the device, as it can be "flipped" into one logic Set state or "flopped" back into the opposing logic Reset state. Flip-flop is the most fundamental building block of sequential logic circuits. The block diagram representation of a typical flip-flop is shown in Figure 1.

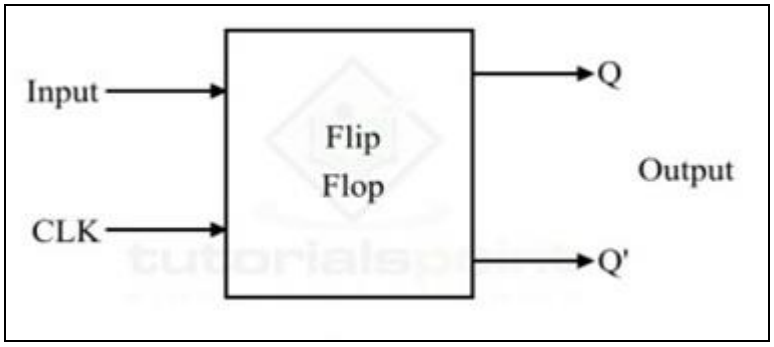

Figure 1: Flip Flop

A flip-flop has one or more inputs and two outputs, usually represented by Q and Q' along with a clock input. The clock input is used to trigger the flip-flop so that it can change states of its outputs.

Some of the most common flip flops are SR Flip flop (Set – Reset), D Flip-flop (Data or Delay), JK Flip -flop (Jack Kilby) and T Flip-flop (Toggle).

SR FLIP FLOP

The SR flip-flop is one of the fundamental parts of the sequential circuit logic. SR flip-flop is a memory device and a binary data of 1 – bit can be stored in it. SR flip-flop has two stable states in which it can store data in the form of either binary zero or binary one. Like all flip-flops, an SR flip-flop is also an edge sensitive device.

SR flip–flop is one of the most vital components in digital logic and it is also the most basic sequential circuit that is possible. The S and R in SR flip-flop means 'SET' and 'RESET' respectively. Hence it is also called Set–Reset flip- flop. The symbolic representation of the SR Flip Flop is shown in Figure 2.

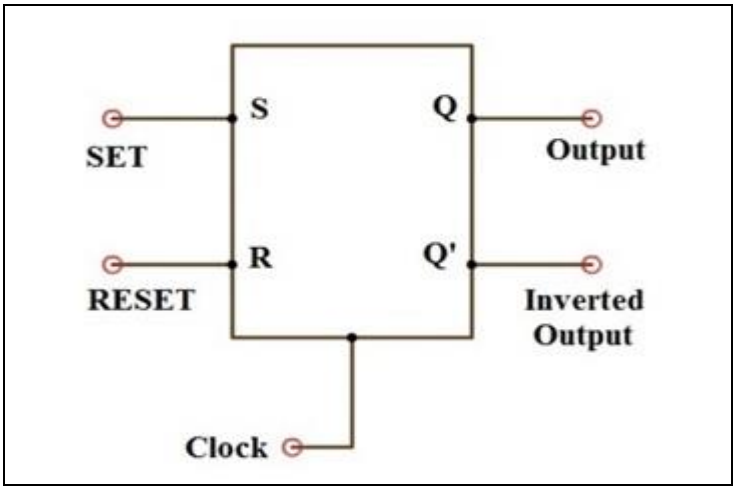

Figure 2: Symbolic representation of SR Flip Flop

S-R Flip-Flop Using NAND Gate

SR flip flop can be designed by cross coupling of two NAND gates. The circuit of SR flip-flop using NAND gates is shown in Figure 3:

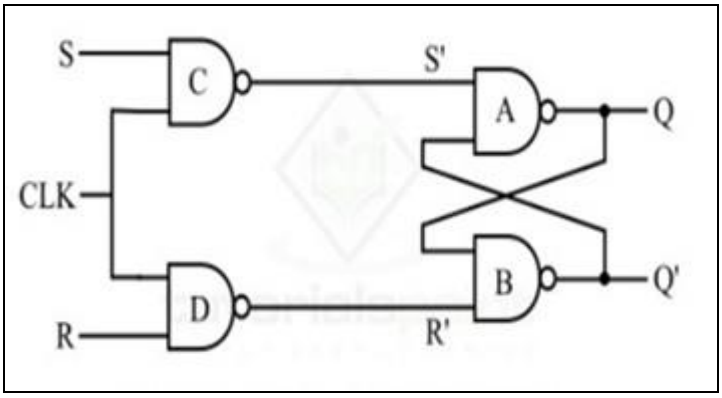

Figure 3: Clocked SR Flip Flop

When the clock signal is not applied, the SR flip-flop circuit remains inactive, and there is no change in the outputs of the flip-flop. When the clock signal is applied, the flip-flop circuit becomes active and operates as explained below:

There are two inputs to the flip-flop defined as R and S. When I/Ps R = 0 and S = 0 then O/P remains unchanged. This is called HOLD state of SR flip flop. When I/Ps R = 0 and S = 1 the flip-flop is switches to the stable state where O/P is 1 called SET state. The I/P condition is R = 1 and S = 0 the flip-flop is switched to the stable state where O/P is 0 called. RESET state. The I/P condition is R = 1 and S = 1 the flip-flop is switched to the stable state where O/P is forbidden i.e. the outputs of both NAND gates A and B try to become 1, which is not possible. This is called FORBIDDEN state of the SR flip flop.
This circuit Diagram for SR flip flop with **SN74HC00N** IC is shown in Figure 4.

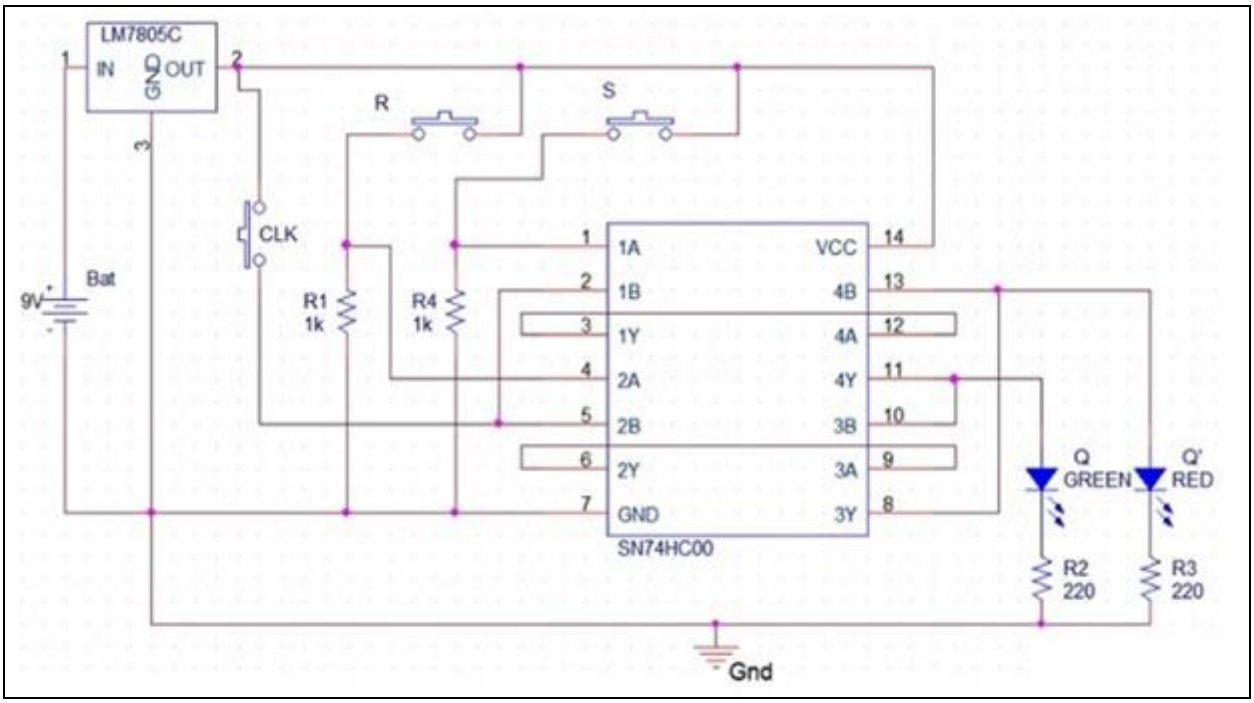

Figure 4: Circuit diagram of SR Flip Flop

SR Flip Flop can be implemented using NAND gate 7400 or it can also be implemented using **SN74HC00N** IC which consist a Quadruple 2-input positive-NAND gates.
IC **SN74HC00N** is used for demonstrating **SR Flip Flop Circuit,** which has four NAND gates inside. The two buttons S (Set) and R (Reset) are the input states for the SR flip-flop. The two LEDs Q and Q' represents the output states of the flip-flop. The 9V battery acts as the input to the voltage regulator LM7805. Hence, the regulated 5V output is used as the Vcc and pin supply to the IC. 5V can also be given directly from the protoboard. Thus, for different input at S' and R' the corresponding output can be seen through LED Q and Q'.
LM7805 regulator is used to limit the supply voltage and pin voltage to 5V maximum.

D FLIP FLOP

D flip flop is an electronic devices that is known as “delay flip flop” or “data flip flop” which is used to store single bit of data. D flip flops are synchronous or asynchronous. The clock single required for the synchronous version of D flip flops but not for the asynchronous one.The D flip flop has two inputs, data and clock input which controls the flip flop. When clock input is high, the data is transferred to the output of the flip flop and when the clock input is low, the output of the flip flop is held in its previous state.
The symbolic representation of the D Flip Flop is shown in Figure 5.

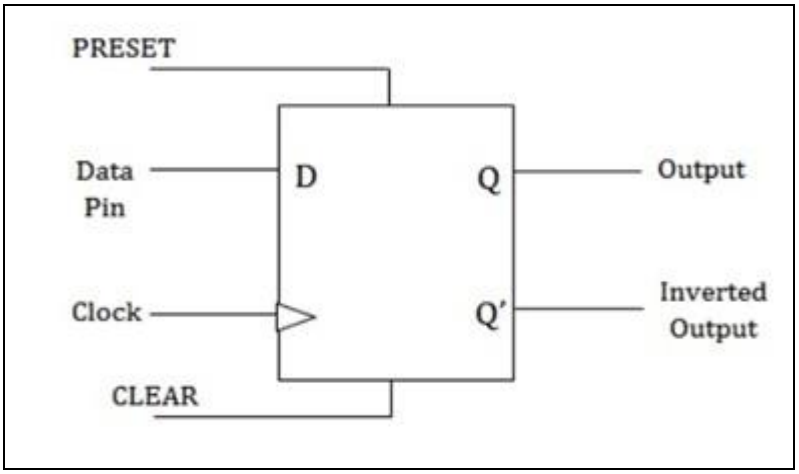

Figure 5: Symbolic representation of D Flip Flop

When the clock signal is low, the flip flop holds its current state and ignores the D input. When the clock signal is high, the flip flop samples and stores D input. The value that was previously fed into the D input is reflected at the flip flop’s Q output. If D = 0 then Q will be 0. If D = 1 then Q will be 1.
Data (D) flip-flop is a variation of a clocked SR flip-flop constructed using either NAND or NOR gates. By adding an inverter (NOT gate) between the Set and Reset inputs, the S and R inputs become complements of each other ensuring that the two inputs S and R are never equal (0 or 1) to each other at the same time allowing us to control the toggle action of the flip-flop using one single D (Data) input. Then this Data input, labelled “D” and is used in place of the “Set” signal, and the inverter is used to generate the complementary “Reset” input thereby making a level-sensitive D-type flip-flop from a level-sensitive SR-latch as now S = D and R = not D as shown in Figure 6.

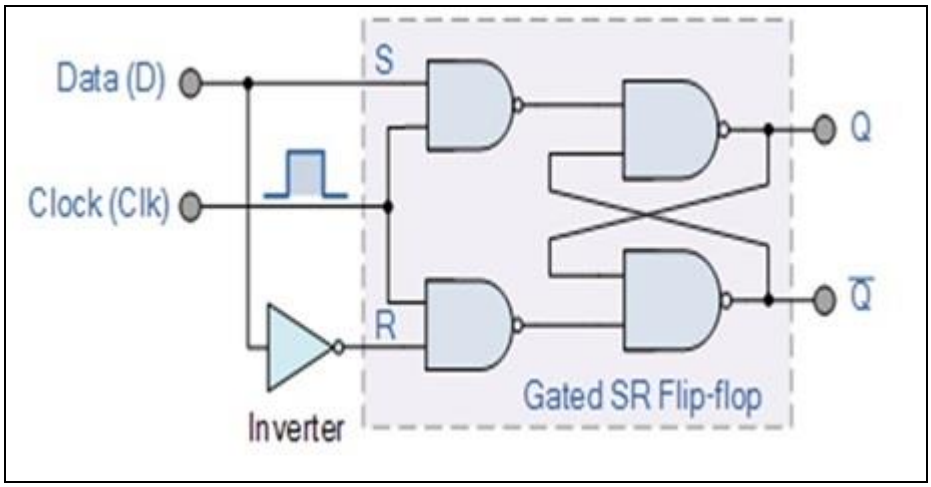

Figure 6: D Flip Flop

This circuit Diagram for SR flip flop with **HEF4013BP** IC is shown in Figure 7. IC **HEF4013BP** is used for demonstrating **D Flip Flop Circuit,** which has Two D type Flip flops inside.

The buttons D (Data), PR (Preset), CL (Clear) are the inputs for the D flip-flop. The two LEDs Q and Q' represents the output states of the flip-flop. The 9V battery acts as the input to the voltage regulator LM7805. Hence, the regulated 5V output is used as the Vcc and pin supply to the IC. 5V can also be given directly from the protoboard. Thus, for different input at D the corresponding output can be seen through LED Q and Q'.

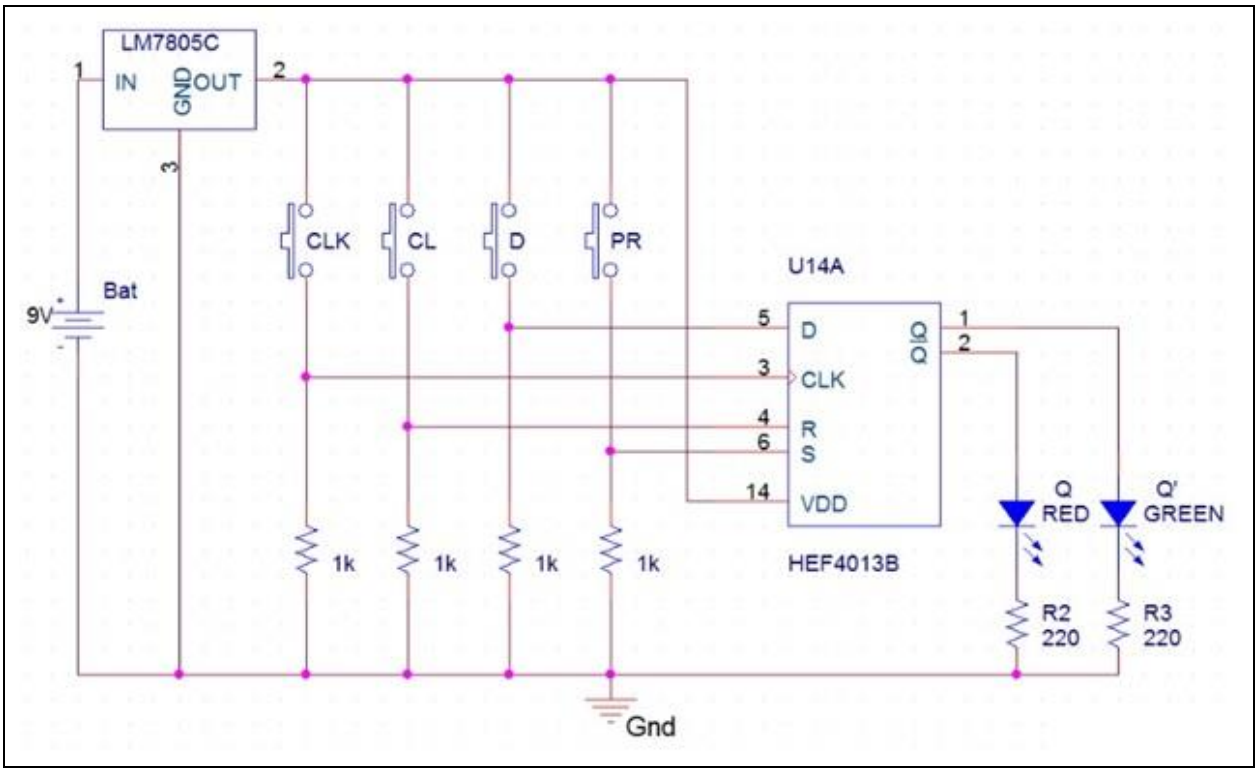

Figure 7: Circuit diagram of D Flip Flop

PROCEDURE:

Implementation of SR Flip-flop

1. Implement SR flip flop circuit with **SN74HC00N** IC by looking into schematic provided in Figure 4.
2. Connect the SET and RESET inputs to two switches.
3. Connect the outputs Q and Q to two LEDs.
4. Turn the SET input, with the switch, to 1 and then to 0.
5. Analyze the behavior of the outputs.
6. Set the RESET line to 1, and then to 0.
7. Analyze the behavior of the outputs again.
8. Repeat the operations with the switches according to the truth table.
9. Note down the observed values in Table 1.

Implementation of D Flip-Flop

1. Implement the circuit of D flip-flop with IC **HEF4013B** by looking into the schematic as shown in Figure 7.
2. Connect the inputs PR and CL to 0.
3. Check the operation of the flip flop D by means of switches and the Clock.
4. Note down the observed values in Table 2.

OBSERVATIONS:

Table 1: Truth Table for S-R Flip Flop

Clock	*S*	*R*	*Q*	*Q'*
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Table 2: Truth Table for D Flip Flop

Clock	*D*	*Q*
1	0	
1	1	

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Psychomotor Domain Assessment Rubric-Level P3					
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Laboratory Session No. _____ Date: _____

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 08

OBJECTIVE:

To OPERATE UNDER SUPERVISION JK Flip Flop and T-Flip Flop.

EQUIPMENT REQUIRED:

- Breadboard
- Power Supply
- IC MC74HC73A (Dual JK flip-flop)
- LM7805
- Switches
- Supply
- LEDS
- Resistor sheet
- Connecting wires

THEORY:

JK FLIP FLOP

The sequential operation of the JK flip flop is exactly the same as for the previous SR flip-flop with the same "Set" and "Reset" inputs. The difference this time is that the "JK flip flop" has no invalid or forbidden input states of the SR Latch even when S and R are both at logic "1".

The **JK flip flop** is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level "1". Due to this additional clocked input, a JK flip-flop has four possible input combinations, "logic 1", "logic 0", "no change" and "toggle".

The symbolic representation of the JK Flip Flop is shown in Figure 1.

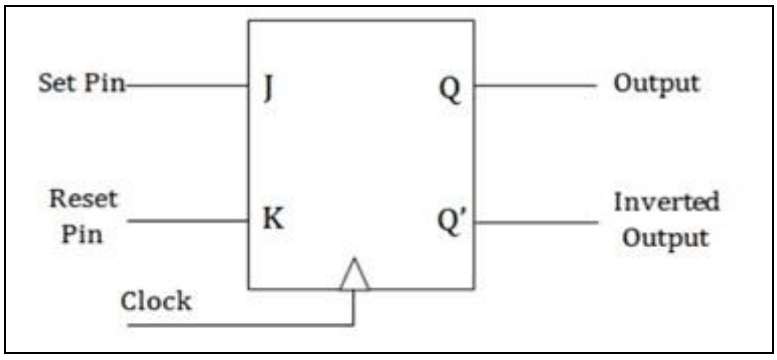

Figure 1: Symbolic representation of JK Flip Flop

JK flip flop can be designed by using NAND gates and it is based on SR flip flop. The circuit of JK flip-flop using NAND gates is shown in Figure 2:

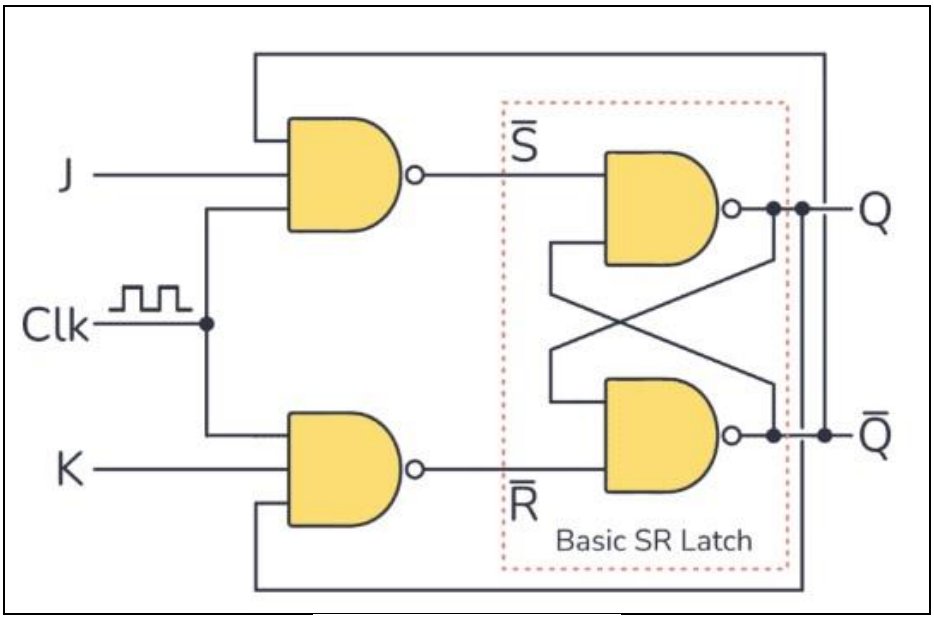

Figure 2: JK Flip Flop

Whenever the clock signal is LOW, the input is never going to affect the output state. The clock has to be high for the inputs to get active. Thus, JK flip-flop is a controlled Bi-stable latch where the clock signal is the control signal. Thus, the output has two stable states based on the inputs selected. The J and K inputs of the J-K flip-flop are synchronous inputs because data on these inputs are transferred to the flip-flops output only on the triggering edge of the clock pulse. When J is HIGH and K is LOW, the Q output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET. When J is LOW and K is HIGH, the Q output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET. When both J and K are LOW, the output does not change from its prior state. When J and K are both HIGH, the flip-flop changes state. This called the toggle mode.

The circuit diagram for JK flip flop with MC74HC73A IC is shown in Figure 3. IC MC74HC73A is used for demonstrating JK flip-flop circuit, which has a Dual JK flip-flop with RESET inside.
The buttons J (Data1), K (Data2), R (Reset), CLK (Clock) are the inputs for the JK flip-flop. The two LEDs Q and Q' represents the output states of the flip-flop. The 9V battery acts as the input to the voltage regulator LM7805. Hence, the regulated 5V output is used as the Vcc and pin supply to the IC. 5V can also be given directly from the protoboard. Thus, for different input at J and K the corresponding output can be seen through LED Q and Q'.

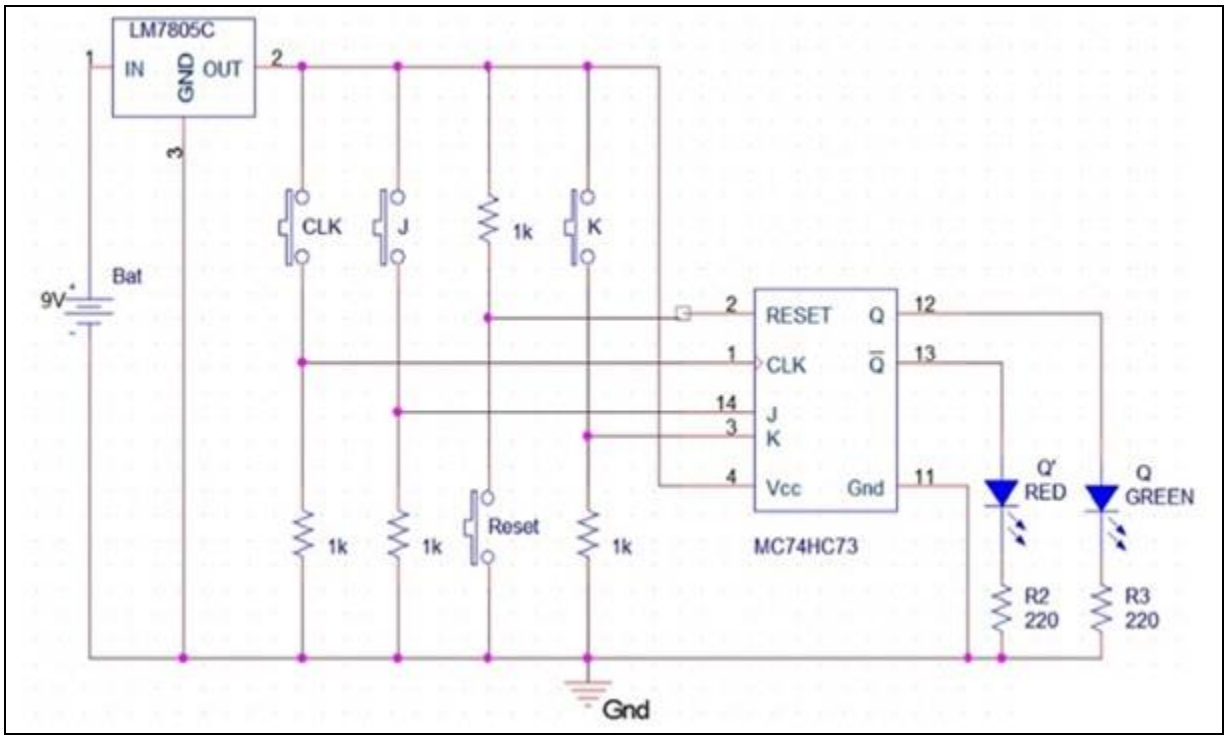

Figure 3: Circuit diagram of JK Flip Flop

T FLIP FLOP

The Toggle (T) flip-flop is a variation of the clocked JK flip-flop. The toggle or T-type flip-flop gets its name from the fact that its two outputs Q and Q' invert from their previous state as it toggles back and forth every time it is triggered (T = 1). The Toggle schematic symbol has two inputs available; one represents the "toggle" (T) input and the other the "clock" (CLK) input.
The basic construction of a T flip flop is almost the same as that of a JK flip flop. The only difference is that the J & K inputs are connected together to make the T input. It has only one input along with the clock input.
The symbolic representation of the T Flip Flop is shown in Figure 4.

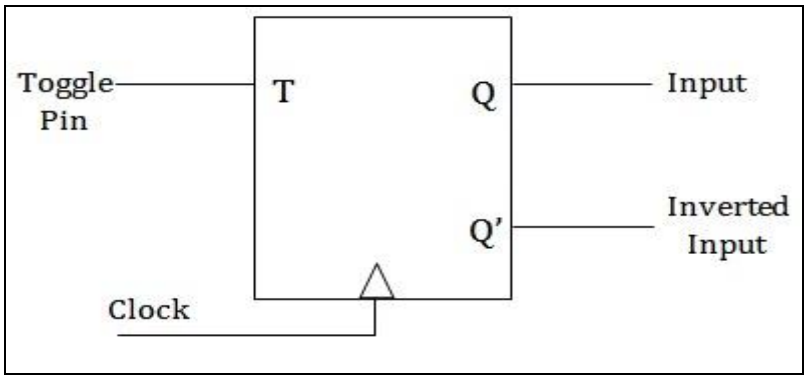

Figure 4: Symbolic representation of T Flip Flop

The simplest construction of a T Flip Flop is with JK Flip Flop. Both the inputs of the "JK Flip Flop" are connected as a single input T. The logical circuit of the T Flip Flop" which is formed from the "JK Flip Flop" is shown in Figure 5.

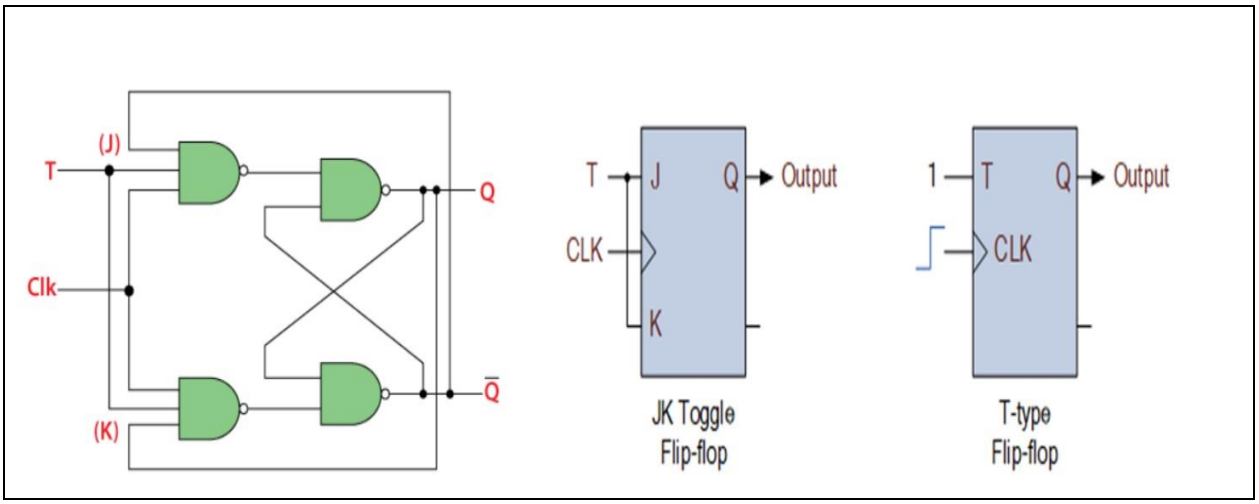

Figure 5: T Flip Flop

Whenever the clock signal is LOW, the input is never going to affect the output state. The clock has to be high for the inputs to get active. Thus, the T flip-flop is a controlled Bi-stable latch where the clock signal is the control signal. Thus, the output has two stable states based on the inputs selected. The T represents the input while the Q and Q' represent the output states of the flip-flop. The RESET input is used to reset the outputs to the default state regardless of the clock or T input. During the normal operation, the RESET pin is held HIGH. During this, the outputs will toggle depending on the T input with a corresponding clock pulse. But, the important thing to consider is all these can occur only in the presence of the clock signal. This, works unlike SR flip Flop & JK flip-flop for the complimentary inputs. This only has the toggling function.

The circuit diagram for T flip flop with MC74HC73A IC is shown in Figure 6. IC MC74HC73A is used for demonstrating T flip-flop circuit, which has a Dual JK flip-flop with RESET inside. The J and K inputs will be shorted and used as a T input.
The buttons T (Toggle), R (Reset), CLK (Clock) are the inputs for the T flip-flop. The two LEDs Q and Q' represents the output states of the flip-flop. The 9V battery acts as the input to the voltage regulator LM7805. Hence, the regulated 5V output is used as the Vcc and pin supply to the IC. 5V can also be given directly from the protoboard. Thus, for HIGH and LOW inputs at T the corresponding output can be seen through LED Q and Q'.

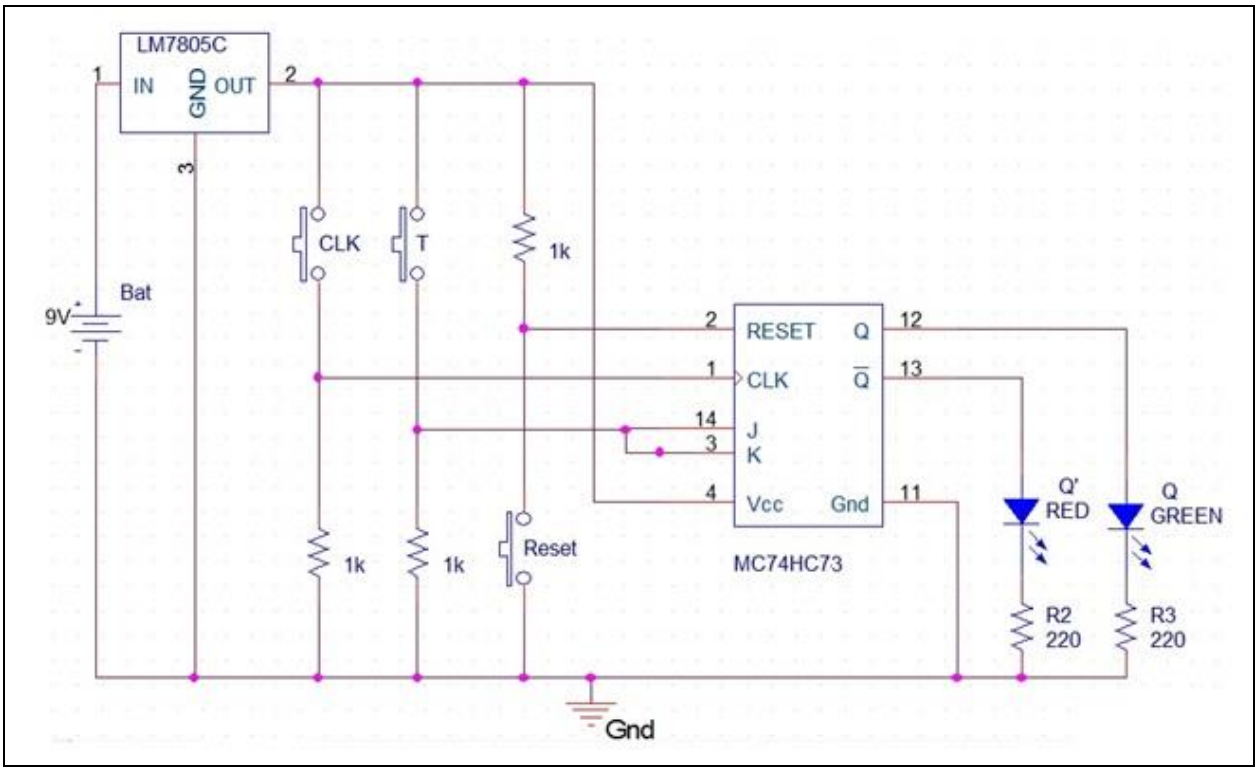

Figure 6: Circuit diagram of T Flip Flop

PROCEDURE:

Implementation of JK Flip-flop

1. Implement the circuit of a JK flip-flop by using **MC74HC73A** according to the given schematic diagram shown in Figure 3.
2. Connect the inputs J and K to two switches, and the outputs to two LEDs.
3. Set the switches connected to the inputs alternatively high.
4. Analyze the behavior of the LEDs.
5. Now, set both switches to logic level 1 and logic level 0 and observe the behavior of the flip-flop.
6. Note down the observed values in Table 1.

Implementation of T Flip-Flop

1. Implement the circuit of T flip-flop by means of J-K flip-flop according to the given schematic diagram shown in Figure 6.
2. Check the operation of the flip-flop T by means of switches and the Clock input.
3. Note down the observed values in Table 2.

OBSERVATIONS:

Table 1: Truth Table for JK Flip Flop

Clock	*J*	*K*	*Q*	*Q'*
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Table 2: Truth Table for T Flip Flop

Clock	*T*	*Q*
1	0	
1	1	

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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 09

OBJECTIVE:

To OPERATE UNDER SUPERVISION the Pseudo NMOS Logic inverter and TRY complex logic function $f = \overline{A(B + CD)}$.

EQUIPMENT REQUIRED:

- Protoboard
- Function Generator
- Digital Multimeter
- Power Supply
- NMOS transistor 2N7000/IRF540 : 5
- PMOS transistor IRF9540 :2
- LED

THEORY:

The modified form of the CMOS inverter is shown in Figure 1. Here, only Q_N is driven by the input voltage while the gate of Q_P is grounded, and Q_P acts as an active load for Q_N. An advantage over standard CMOS is that each input needs to be connected to the gate of only one transistor or, alternatively, only one additional transistor (an NMOS) will be needed for each additional gate input. Thus the area and delay penalties arising from increased fan-in in a standard CMOS will be reduced. This is indeed the motivation for exploring this modified inverter circuit.

The inverter circuit of Figure 1 resembles other forms of NMOS logic that consist of a driver transistor (Q_N) and a load transistor (in this case, Q_P); hence the name pseudo-NMOS.

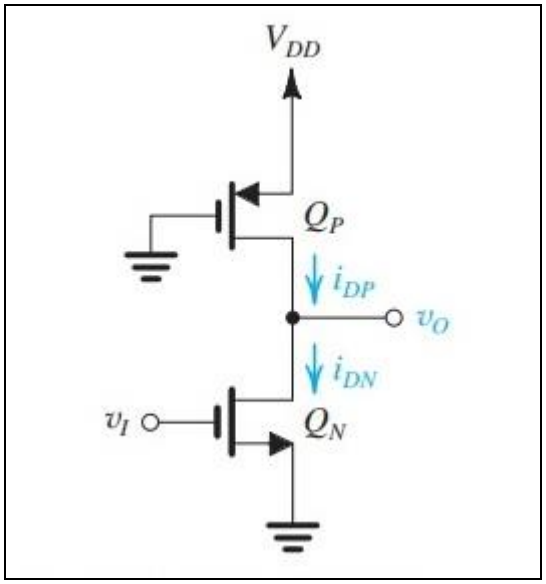

Figure 1: Pseudo NMOS logic Inverter

Except for the load device, the pseudo-NMOS gate circuit is identical to the PDN of the complementary CMOS gate. Pseudo-NMOS realization of complex gate $f = \overline{A(B + CD)}$ is shown in Figure 2. Note that five transistors are used compared to the eight used in standard CMOS.

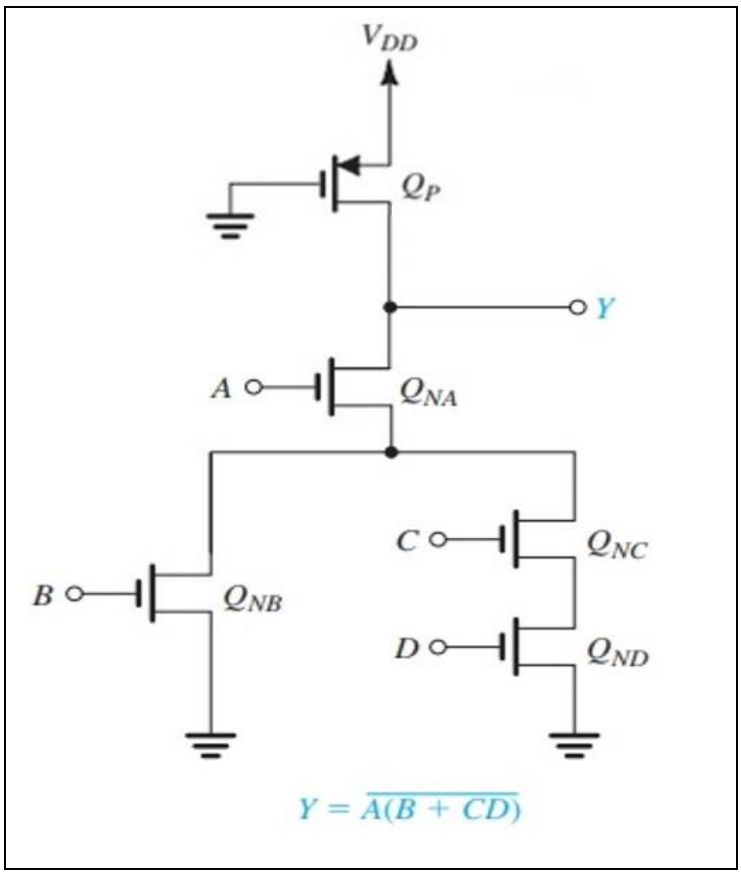

Figure 2: Pseudo NMOS realization of complex gate

PROCEDURE:

1. Connect the circuit on breadboard according to the given Figure 1 for implementing Pseudo NMOS inverter and note down the observed values in Table 1. Provide +5V VDD to the circuit.
2. For implementing Pseudo NMOS complex logic function $f = \overline{A(B + CD)}$, connect the NMOS transistors as shown in Figure 2.
3. Now note down the observed value of Pseudo NMOS complex logic function in Table 2.

OBSERVATIONS:

Table 1: For Pseudo NMOS Inverter

Vi (Input)	Vo (Output)
0V	
5V	

Table 2: For $Y = \overline{A(B + CD)}$

$Y = \overline{A(B + CD)}$				
A	***B***	***C***	***D***	***Y***

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Remarks	
Instructor's Signature with Date:	

LAB SESSION 10

OBJECTIVE:

To OPERATE UNDER SUPERVISION pass transistor logic to implement two input AND gate and PRACTICE 2-to-1 multiplexer using CMOS transmission gates.

EQUIPMENT REQUIRED:

- Protoboard
- Function Generator
- Digital Multimeter
- Power Supply
- NMOS transistor 2N7000/IRF540 : 4
- PMOS transistor IRF9540 : 2
- Inverter IC 4049 : 2
- LED

THEORY:

Figure 1 shows a conceptually simple approach for implementing logic functions that utilizes series and parallel combinations of switches that are controlled by input logic variables to connect the input and output nodes. Each of the switches can be implemented either by a single NMOS transistor or by a pair of complementary MOS transistors connected in what is known as the **CMOS transmission-gate** configuration as shown in Figure 2(a) and Figure 2(b). A logic which utilizes MOS transistors in the series path from input to output, to pass or block signal transmission, is known as pass-transistor logic (PTL). It is basically a transistor used as a switch to pass logic levels between nodes of a circuit, instead of as a switch connected directly to a supply voltage.

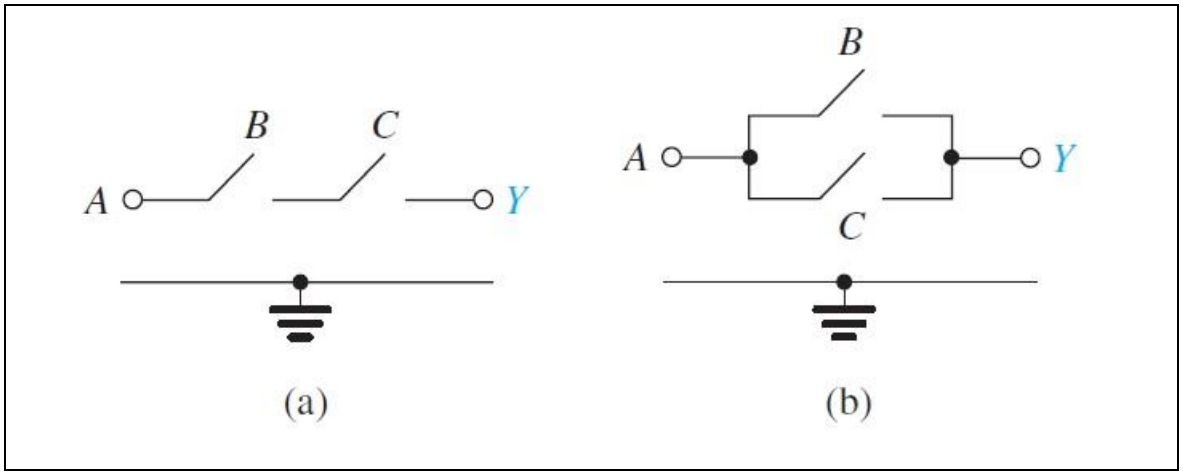

Figure 1: Conceptual pass transistor logic (a) two switches connected in series (b) two switches connected in parallel

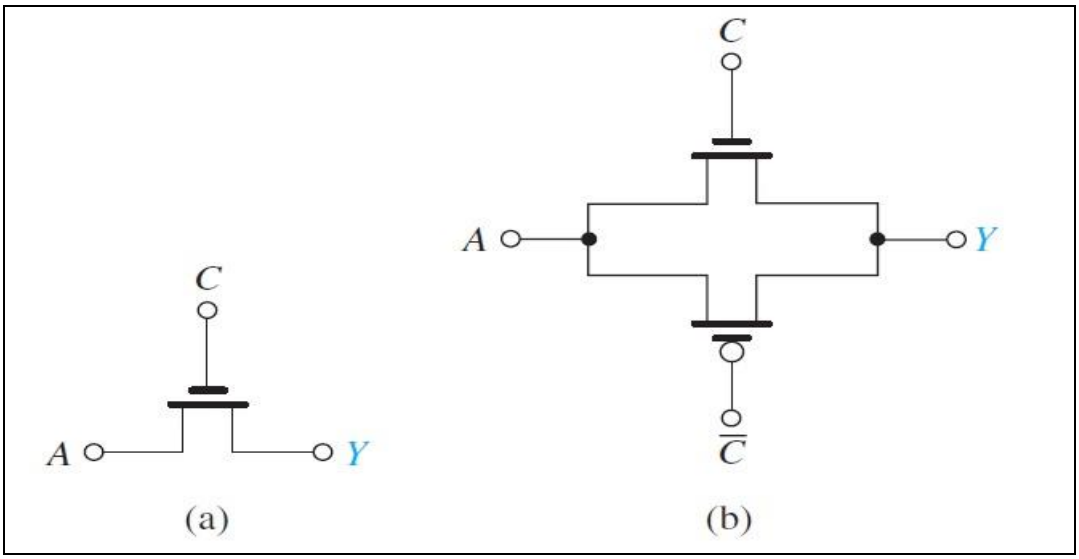

Figure 2: Two possible implementations of a voltage-controlled switch connecting nodes *A* and *Y*: (a) single NMOS transistor and (b) CMOS transmission gate.

NMOS transistors as switches

Figure 3 shows the circuit of an NMOS transistor *Q* which is used to implement a switch connecting an input node with an output node.

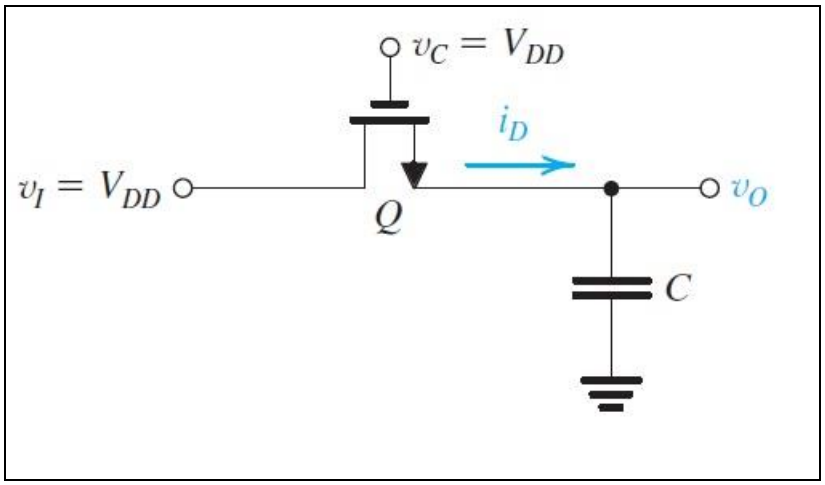

Figure 3: Operation of NMOS transistor as a switch in the implementation of PTL circuits.

Implementing the switches in a PTL circuit with single NMOS transistors results in a simple circuit with small area and small node capacitances.

CMOS transmission gates as switches

Great improvements in static and dynamic performance are obtained when the switches are implemented with CMOS transmission gates. The transmission gate utilizes a pair of complementary transistors connected in parallel. It acts as an excellent switch, providing

bidirectional current flow, and it exhibits an on-resistance that remains almost constant for wide ranges of input voltage. These characteristics make the transmission gate not only an excellent switch in digital applications but also an excellent analog switch in such applications as data converters and switched-capacitor filters.

NMOS transistor transmits the 0-V level to the output perfectly and thus produces a "good 0." It has difficulty, however, in passing the *VDD* level thus producing a "poor 1." PMOS transistor does exactly the opposite; that is, it passes the *VDD* level perfectly and thus produces a "good 1" but has trouble passing the 0-V level, thus producing a "poor 0." It is natural therefore to think that placing an NMOS and a PMOS transistor in parallel would produce good results in both the 0 and 1 cases. Another way to describe the performance of the two transistor types is that the NMOS is good at pulling the output down to 0 V, while the PMOS is good at pulling the output up to *VDD*. Interestingly, these are also the roles they play in the standard CMOS inverter.

Figure 4 shows the transmission gate together with its frequently used circuit symbol. The transmission gate is a bilateral switch that results in $vY = vX$ when vC is high (*VDD*).

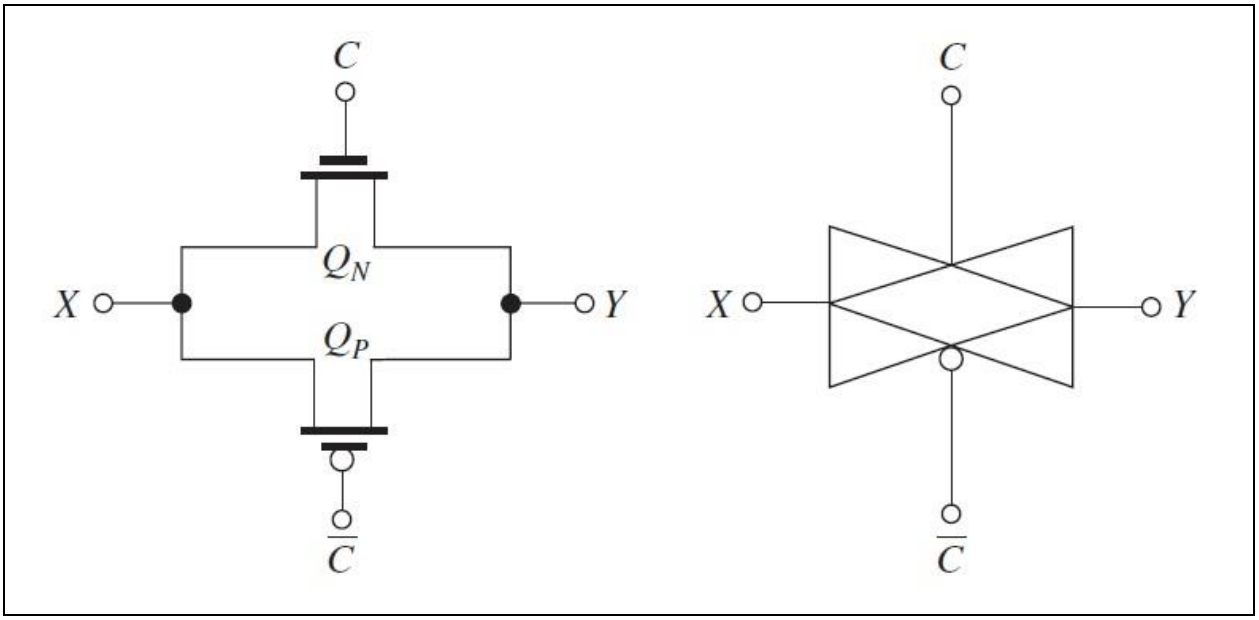

Figure 4: CMOS transmission gate and its circuit symbol

Transmission gates provide far superior performance, both static and dynamic, than is possible with single NMOS switches. The price paid is increased circuit complexity, area, and capacitance.

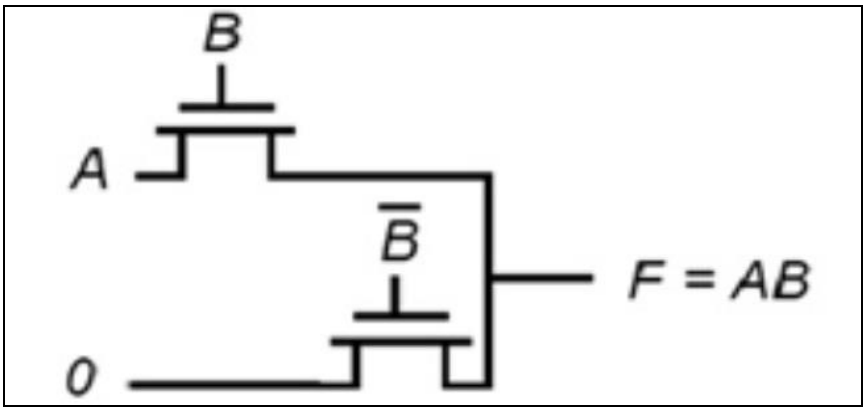

Figure 5: AND gate using pass transistor logic

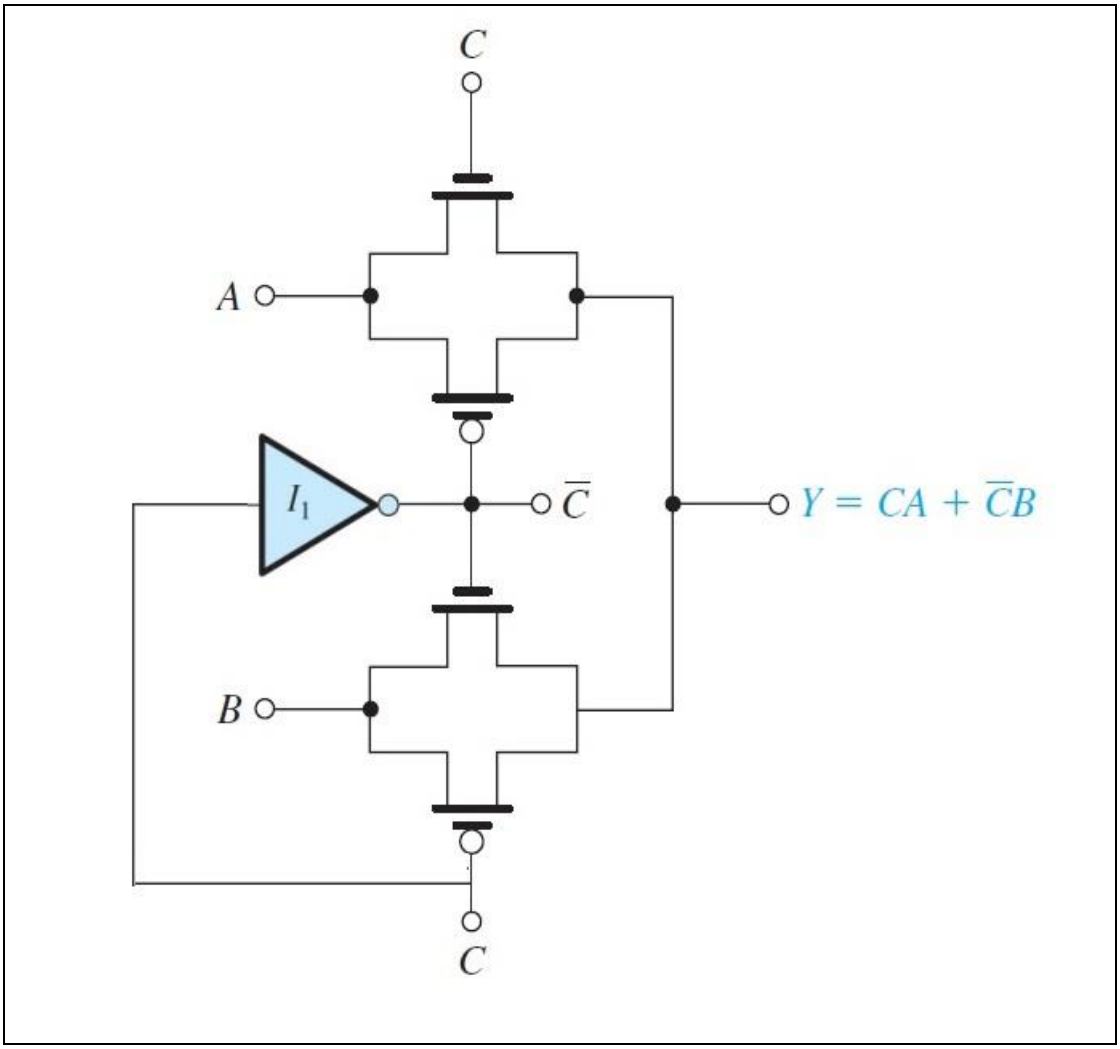

Figure 6: Realization of 2-to-1 multiplexer using CMOS transmission gates

PROCEDURE:

1. For the implementation of AND operation using pass transistor logic (PTL) connect the circuit as shown in Figure 5. One inverter is required to generate the complement of B. Note down the observed values in Table 1.
2. For the implementation of 2-to-1 multiplexer using CMOS transmission gates connect the circuit as shown in Figure 6. One inverter is required to generate the complement of C. Note down the observed values in Table 2.

OBSERVATIONS:

Table 1: For AND operation using PTL

A	***B***	***F***
0V	0V	
0V	5V	
5V	5V	

Table 2: For 2-to-1 multiplexer using CMOS transmission gates

A	***B***	***C***	***Y***
5V	0V	0V	
5V	0V	5V	
5V	5V	0V	
5V	5V	5V	

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Equipment Handling ***Equipment care*** during the use.	Doesn't handle equipment with required care.	Rarely handles equipment with required care.	Occasionally handles equipment with required care.	Often handles equipment with required care.	Handles equipment with required care.
Group Work ***Contributes*** in a group based lab work.	Doesn't participate and contribute.	Slightly participates and contributes.	Somewhat participates and contributes.	Moderately participates and contributes.	Fully participates and contributes.

Laboratory Session No. _____ Date: _____

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 11

OBJECTIVE:

To OPERATE UNDER SUPERVISION the Dynamic logic circuit and PRACTICE the function $Y = \overline{A + BC}$.

EQUIPMENT REQUIRED:

- Protoboard
- Logic probe
- Digital Multimeter
- Power Supply
- NMOS transistor 2N7000/IRF540 : 4
- PMOS transistor IRF9540 : 1
- Capacitor: 10uF

THEORY:

Static circuits do not need clocks (i.e., periodic timing signals) for their operation, although clocks may be present for other purposes. In contrast, the dynamic logic circuits rely on the storage of signal voltages on parasitic capacitances at certain circuit nodes. Since charge will leak away with time, the circuits need to be periodically refreshed; thus the presence of a clock with a certain specified minimum frequency is essential. In static logic families the pull up and pull down networks operate concurrently. Dynamic logic on the other hand uses a sequence of precharge and conditional evaluation phases governed by the clock to realize complex logic functions.

Figure 1(a) shows the basic dynamic logic gate. It consists of a pull-down network (PDN) that realizes the logic function in exactly the same way as the PDN of a standard CMOS gate or a pseudo-NMOS gate. The operation of the pulldown network (PDN) can be divided into two major phases. The precharge and the evaluation phase. In what mode the circuit is operating is determined by the signal φ, the "clock" signal. Here, however, we have two switches in series that are periodically operated by the clock signal φ whose waveform is shown in Figure 1(b). When φ is low, *Qp* is turned on, and the circuit is said to be in the setup or **precharge phase**. When φ is high, *Qp* is off and *Qe* turns on, and the circuit is in the **evaluation phase**. Finally, note that *CL* denotes the total capacitance between the output node and ground.

Precharge phase

During precharge, *Qp* conducts and charges capacitance *CL* so that at the end of the precharge interval, the voltage at *Y* is equal to *VDD*. Also during precharge, the inputs *A*, *B*, and *C* are allowed to change and settle to their proper values. Observe that because *Qe* is off, no path to ground exists.

Evaluation phase

During the evaluation phase, *Qp* is off and *Qe* is turned on. Now, if the input combination is one that corresponds to a high output, the PDN does not conduct (just as in a standard CMOS gate)

and the output remains high at *VDD*; thus *VOH* = *VDD*. Observe that no low-to-high propagation delay is required, thus *tPLH* = 0. On the other hand, if the combination of inputs is one that corresponds to a low output, the appropriate NMOS transistors in the PDN will conduct and establish a path between the output node and ground through the on transistor *Qe*. Thus *CL* will be discharged through the PDN, and the voltage at the output node will reduce to *VOL* = 0 V. The high-to-low propagation delay *tPHL* can be calculated in exactly the same way as for a standard CMOS circuit, except that here we have an additional transistor, *Qe*, in the series path to ground. Although this will increase the delay slightly, the increase will be more than offset by the reduced capacitance at the output node as a result of the absence of the PUN. The only possible path between the output node and a supply rail is to GND, consequently, once "OUT" is discharged, it cannot be charged again. This is in contrast with the static circuit, where the output node is low-impedance under all possible circumstances. The inputs to the circuit can therefore make at most one transition during evaluation.

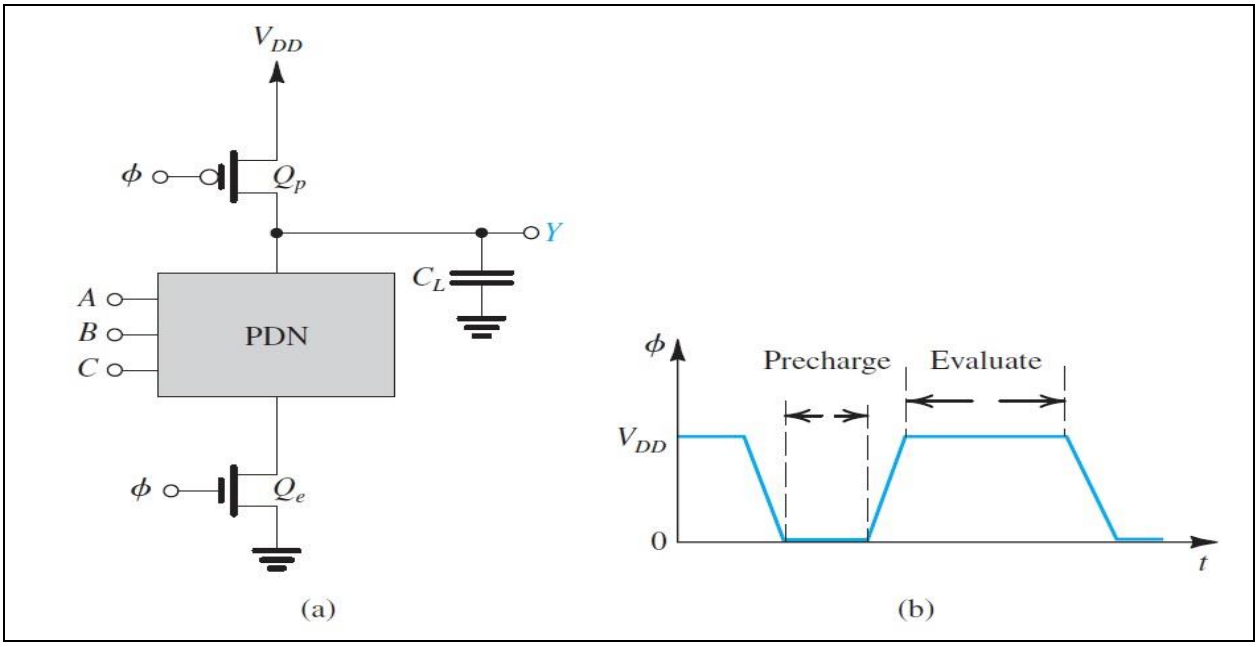

Figure 1: (a) Basic structure of dynamic MOS logic circuits. (b) Waveform of the clock needed to operate the dynamic logic circuit.

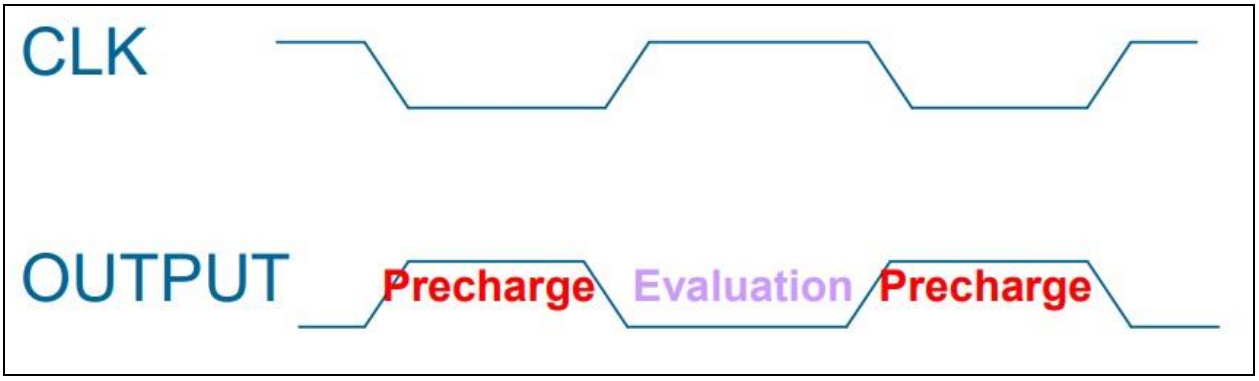

Figure 1(c): waveform of clock and output

Figure 2 shows the circuit that realizes the function $\overline{Y = A + BC}$.

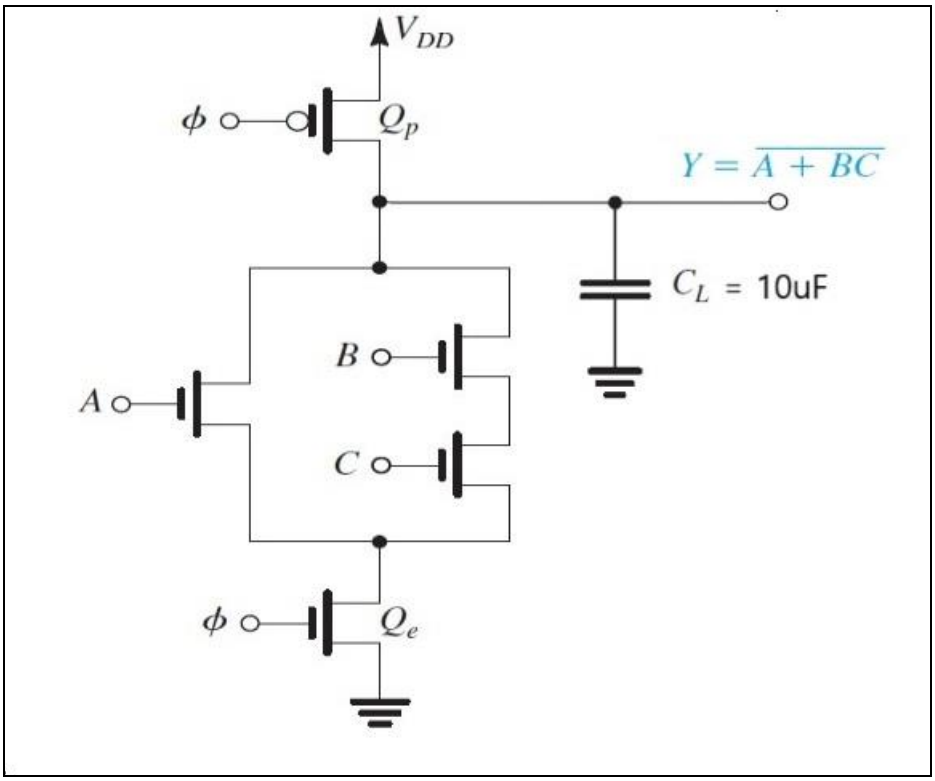

Figure 2: Realization of function $Y = \overline{A + BC}$

The action of charging and discharging is shown in the following Figure 3:

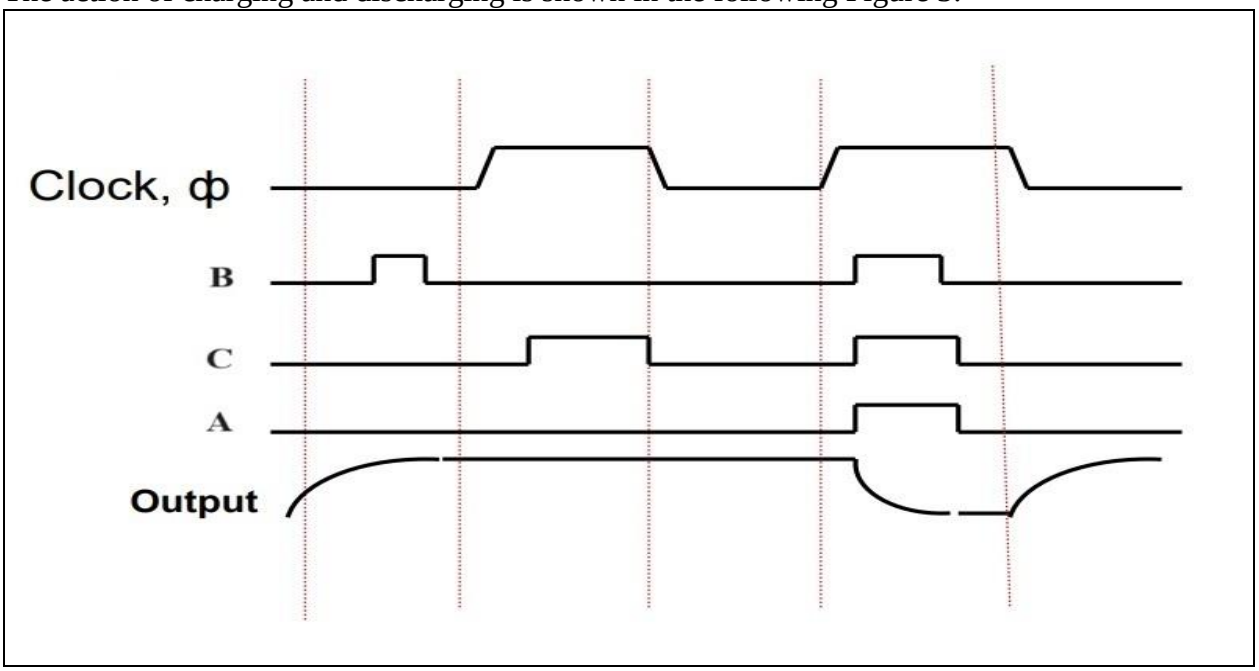

Figure 3: Input/output relationship of Figure 2

PROCEDURE:

1. Implement the circuit shown in Figure 2. Provide +7V supply to the circuit.
2. Apply a square wave signal, 300Hz, 7Vpp from the function generator for the clock input at the gates of transistor *Qp and Qe*.
3. Note down the observed values in Table 1.

OBSERVATIONS:

Table 1: For Realization of function $Y = \overline{A + BC}$

Clock (Φ)	*A*	*B*	*C*	*Y*

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NED University of Engineering & Technology
Department of Electronic Engineering
Course Code and Title: EL-202 Integrated Circuits

Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	Extent of Achievement				
	0	1	2	3	4
Equipment Identification Sensory skill to ***identify*** equipment and/or its component for a lab work.	Not able to identify the equipment.	--	--	--	Able to identify equipment as well as its components.
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Laboratory Session No. _____ Date: _____

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 12

OBJECTIVE:

To OPERATE UNDER SUPERVISION two single-input Domino CMOS logic gates connected in cascade.

EQUIPMENT REQUIRED:

- Protoboard
- Function Generator
- Digital Multimeter
- Power Supply
- NMOS transistor 2N7000/IRF540 : 6
- PMOS transistor IRF9540 : 4
- CD4049 (Inverter IC): 1
- Capacitors (47uF): 2

THEORY:

Domino CMOS logic is a form of dynamic logic that results in cascadable gates. Figure 1 shows the structure of the Domino CMOS logic gate. The circuit consists of a dynamic MOS logic gate with a static CMOS inverter connected to the output. During evaluation, *Y* either will remain low (at 0 V) or will make one 0-to-1 transition (to *VDD*).

Operation of the gate is straightforward. During precharge, *X* will be raised to *VDD*, and the gate output *Y* will be at 0 V. During evaluation, depending on the combination of input variables, either *X* will remain high and thus the output *Y* will remain low (*tPHL* = 0) or *X* will be brought down to 0 V and the output *Y* will rise to *VDD* (*tPLH* finite). Thus, during evaluation, the output either remains low or makes only one low-to-high transition.

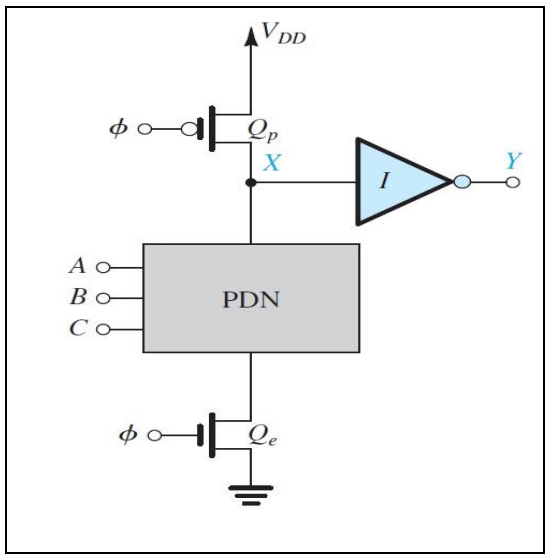

Figure 1: The Domino CMOS logic

To see why Domino CMOS gates can be cascaded, consider the situation in Figure 2 (a), where two Domino gates are connected in cascade.

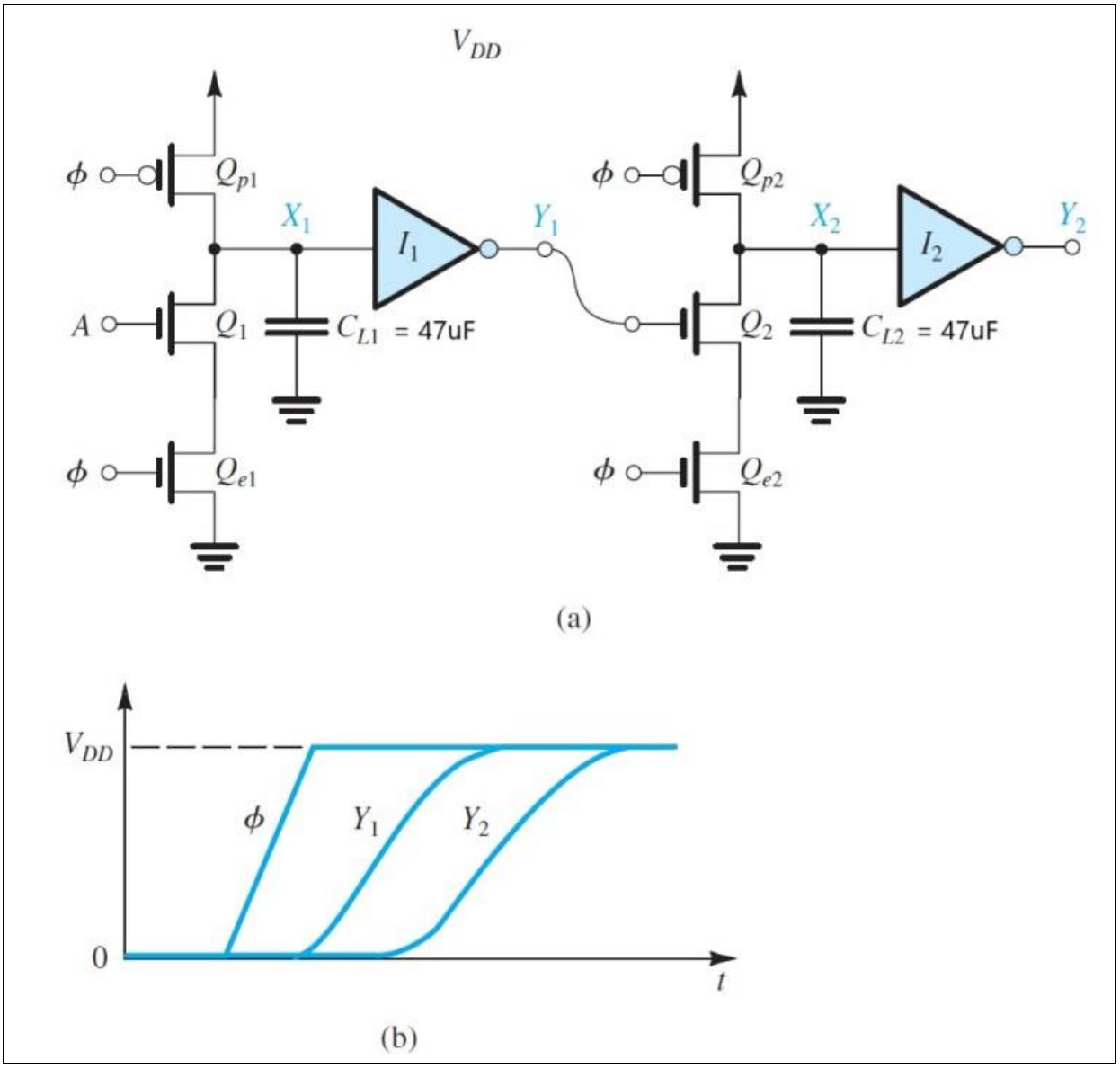

Figure 2: (a) Two single-input Domino CMOS logic gates connected in cascade. (b) Waveforms during the evaluation phase.

For simplicity, we show single-input gates. At the end of precharge, *X*1 will be at *VDD*, *Y*1 will be at 0 V, *X*2 will be at *VDD*, and *Y*2 will be at 0 V. As in the preceding case, assume that *A* is high at the beginning of evaluation. Thus, as φ goes up, capacitor *CL*1 will begin discharging, pulling *X*1 down. Meanwhile, the low input at the gate of *Q*2 keeps *Q*2 off, and *CL*2 remains fully charged. When *vX*1 falls below the threshold voltage of inverter *I*1, *Y*1 will go up, turning *Q*2 on, which in turn begins to discharge *CL*2 and pulls *X*2 low. Eventually, *Y*2 rises to *VDD*.

From this description, it can be seen that the output of the Domino gate is low at the beginning of evaluation, no premature capacitor discharge will occur in the subsequent gate in the cascade. As indicated in Figure 2(b), output *Y*1 will make a 0-to-1 transition *tPLH* seconds after the rising edge of the clock. Subsequently, output *Y*2 makes a 0-to-1 transition after another *tPLH* interval. The propagation of the rising edge through a cascade of gates resembles contiguously placed dominoes falling over, each toppling the next, which is the origin of the name Domino CMOS logic. Domino CMOS logic finds application in the design of address decoders in memory chips, for example.

PROCEDURE:

1. Implement the circuit shown in Figure 2(a). Provide +7V supply to the circuit.
2. Apply a square wave signal, 300Hz, 7Vpp from the function generator for the clock input at the gates of transistor *Qp and Qe*.
3. Place a static CMOS inverter CD4049 IC in place of I_1 and I_2.
4. Note down the observed values in Table 1.

OBSERVATIONS:

Table 1: For Two single-input Domino CMOS logic gates connected in cascade

Clock (Φ)	***A***	***Y_1***	***Y_2***

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Laboratory Session No. _____ Date: _____

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

Open Ended Lab

OBJECTIVE:

To PRACTICE and implement a multiplexer using transmission gates to efficiently select and route data from multiple input sources to a single output line for a traffic control to efficiently manage signals to prioritize and route traffic data for smoother traffic flow.

PREAMBLE:

A **transmission gate** (**TG**) is an analog gate similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. It is a CMOS-based switch, in which PMOS passes a strong 1 but poor 0, and NMOS passes strong 0 but poor 1. Both PMOS and NMOS work simultaneously. Two MOS transistors are connected back-to-back in parallel with an inverter used between the gate of the NMOS and PMOS to provide the two complementary control voltages. When the input control signal, V_C is LOW, both the NMOS and PMOS transistors are cut-off and the switch is open. When V_C is high, both devices are biased into conduction and the switch is closed. Thus the transmission gate acts as a "closed" switch when $V_C = 1$, while the gate acts as an "open" switch when $V_C = 0$ operating as a voltage-controlled switch. The bubble of the symbol indicating the gate of the PMOS FET.
Transmission gates are used in order to implement electronic switches and analog multiplexers. A multiplexer is an essential component in digital logic circuits that enables the selection and routing of multiple input lines to a common output line. It is used to control the flow of data by selecting one input line and directing it to the output line based on the control signals provided.

ASSOCIATED COURSE LEARNING OUTCOME:

Following CLO will be assessed in this open ended lab task.

Course Learning Outcome (CLO)	Description	Taxonomy Level	Mapped PLO
CLO-3	Practice various Integrated Circuits to validate theoretical concepts on hardware and software platform.	P3	PLO-4

Complex Engineering Activity Mapping with PLO, Knowledge Profile (WK) and CEA Attributes

PLO/GA	Knowledge Profile (WK) (Select appropriate)	CEA Attributes (Select appropriate)
☐PLO1 ☐PLO2 ☐ PLO3 ■ PLO4 ☐ PLO5 ☐ PLO6 ☐ PLO7 ☐ PLO8 ☐ PLO9 ☐ PLO10 ☐ PLO11 ☐ PLO12	☐ WK1: Natural Sciences ☐ WK2: Mathematics and Computing ☐ WK3: Engineering Fundamentals ☐WK4: Engineering Specializations ☐ WK5: Engineering Design ☐WK6: Engineering Practices ☐ WK7: Engineering in Society ■WK8: Research Literature	■Range of Resources ☐Level of interaction ☐ Innovation ☐ Consequence to society and the environment ☐ Familiarity

PROJECT ACTIVITY:

Through this open ended lab task, the students are required to:

1. **Research the literature** for the understanding of transmission gates based multiplexer operation.
2. Use the **range of resources** such as software, breadboard, power supply, function generator, logic probes and related equipment's for the designing of the required transmission gates based multiplexer
3. Develop the hardware of a transmission gates based multiplexer based on the **familiarity** with transmission gates and advanced multiplexer design knowledge.

DELIVERABLES:

1. Each group is required to submit a report documenting the entire lab task including detailed theory, truth table and the circuit diagram verified with the submitted designed hardware.
2. Circuit diagram for the multiplexer using transmission gates with complete details of the component used.

3. Experiment with different configurations of transmission gates to optimize the multiplexer's performance using different control strategies and evaluate the performance of the multiplexer under various traffic conditions.
4. Schematic and the simulation results (values and properly labeled output) of the designed circuit.
5. Hardware of the complete multiplexer using transmission gates with proper arrangement of transmission gates, input sources, and output device connections.

INSTRUCTIONS:

1. Students should submit the open ended lab task in a group of **four**.
2. Attach **four rubric sheet**, separate rubric sheet for each member of the group with the report.
3. Please make sure to submit the report in a **readable** format.

NED University of Engineering & Technology
Department of Electronic Engineering
Course Code and Title: EL-202 Integrated Circuits

Psychomotor Domain Assessment Rubric-Level P3					
Criterion	**Level of Attainment**				
	Below Average (0)	**Average (1)**	**Good (2)**	**Very Good (3)**	**Excellent (4)**
Literature review for understanding of the designed circuit	No literature review	Limited understanding of transmission gates and multiplexer design without reference citation.	Basic understanding of transmission gates and multiplexer design with some reference cited.	Solid understanding of transmission gates and multiplexer design principles; with relevant reference cited.	Thorough understanding of transmission gates and multiplexer design concept; with recent research and referencing.
Simulation of the designed circuit	No simulation	Schematic entry only with no simulation results	Schematic with Incomplete and inaccurate simulation	Complete schematic with complete simulation but inaccurate	Accurate and complete simulation with proper schematic
Truth Table and Circuit diagram	Unable to show truth table observations and circuit diagram	Truth table shown with significant errors and incorrect circuit.	Truth table shown with minor errors and mistake in circuit.	Truth table shown with no errors but mistake in circuit	Truth table and circuit diagram both shown correctly
Hardware Results	No hardware results	Incomplete hardware with wrong results	Complete hardware with totally wrong results	Complete hardware with partially correct results	Complete hardware with proper output results
Demonstration	No demonstration	Partial and incorrect demonstration	Partial and better demonstration	Improved demonstration	Correct demonstration

Laboratory Session No. _____ Date: _____

Weighted CLO (Psychomotor Score)	
Student Name and Roll No:	
Instructor's Signature with Date:	