Department of Electronic Engineering

N.E.D. University of Engineering & Technology,

PRACTICAL WORK BOOK

For the course

ELECTRONIC DEVICES AND CIRCUITS (EL-201) For S.E (EL)

Instructors name: ______________________

Student Name: ______________________

Roll no.: ____________ **Batch:** ____________

Semester: ____________ **Year:** ____________

Department: ______________________

LABORATORY WORK BOOK
FOR THE COURSE

EL - 201 ELECTRONIC DEVICES AND CIRCUITS

Prepared by:
Ayesha Akhtar (Lecturer)
Revised by:
Maheen Mazhar (Lecturer)
Reviewed by:
Dr. Faizan Shirazi

Approved By:
The Board of Studies of Department of Electronic Engineering

Electronic Devices and Circuits Laboratory Manual

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LAB SESSION 01

OBJECTIVE:

To OPERATE UNDER SUPERVISION the MOS Current source circuit

EQUIPMENT REQUIRED:

- Proto board
- Function Generator
- Digital Multimeter
- Power Supply
- Resistors
- Transistors: 2 x 2N7000

THEORY:

A current mirror replicates the input current of a current sink or current source as an output current. The output current may be identical to the input current or can be a scaled version of it.
The current mirror circuit is used to **copy the flow of current in one active device** and controlling the flow of current in another device by maintaining the output current stable instead of loading.

$$I_{ref} = I_0$$

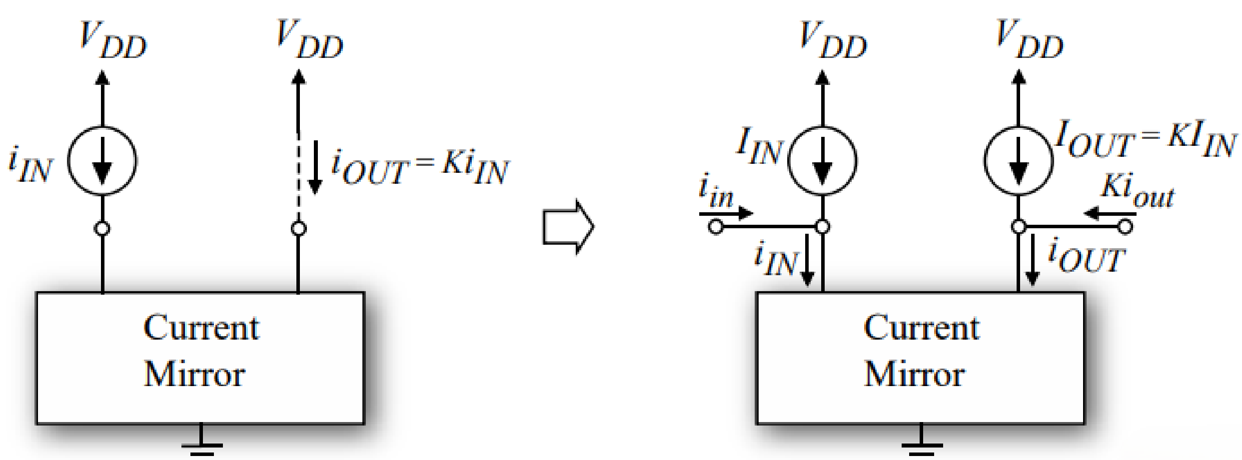

Figure 1. Concept of current mirror

The goal for a current mirror is to establish a stable I_{ref} value and then to mirror (or replicate) current I_{ref} in other branches of the circuit as shown in figure 1. I_0 is to be equal to I_{ref} regardless of the applied value of V_{DS} of the mirroring transistor.
An error or deviation can result from following factors:
(1) the mirroring transistor's finite output drain-to-source resistance r_0,
(2) a parametric mismatch between transistors Q_1 and Q_2, and
(3) a temperature difference between transistors Q_1 and Q_2.
In integrated circuits the transistors are physically close together for thermal matching and they are fabricated simultaneously on the same wafer. So, they should be well matched and thermally coupled as well as physically possible.

A finite output resistance r_o causes I_0 to deviate from I_{ref}. The equations for the drain currents of transistors Q_1 & Q_2 are as follows:

$$I_{ref} = \frac{1}{2}\mu_n\left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2(1 + \lambda V_{DS1}); where\ V_{DS1} = V_{GS}\ in\ Q_1$$

$$I_o = \frac{1}{2}\mu_n\left(\frac{W}{L}\right)_2 (V_{GS} - V_t)^2(1 + \lambda V_{DS2})$$

Taking ratio of the above two equations, yields;

$$\frac{I_o}{I_{ref}} = \frac{\left(W/_L\right)_2(1 + \lambda V_{DS2})}{\left(W/_L\right)_1(1 + \lambda V_{GS}}$$

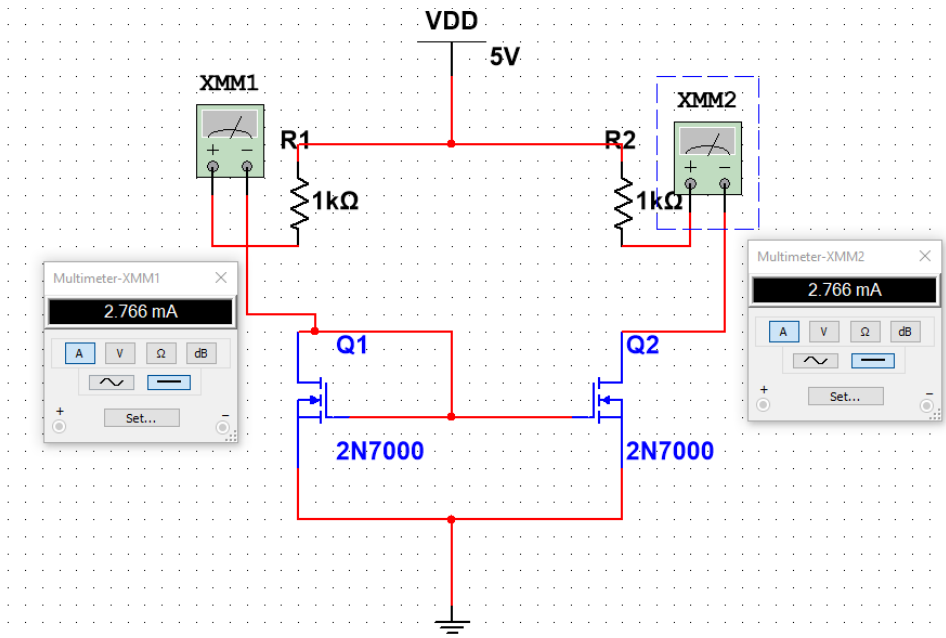

Fig.2 Simple MOS Mirror

PROCEDURE:

- Implement the circuit provided in figure 2 for Simple MOS current Mirror.
- Vary R_2 step by step & observe readings for I_{ref} & I_o.

OBSERVATIONS:

V_{GS1} =

$V_{GS\ 2}$=

V_{DS1} =

S. No.	**R_2 (load)**	**I_{ref}**	I_0	$V_{DS\,2}$	Mode of operation of Q_2
1	**680 Ω**				
2	**820 Ω**				
3	**1K Ω**				
4	**1.2 kΩ**				
5	**1.5 kΩ**				
6	**2.2 kΩ**				
7	**2.7 KΩ**				

CALCULATIONS:

Condition for saturation mode of operation:

$$V_{DS} \geq V_{GS} - V_t$$

Calculate the percentage error.

$$\%\,\text{Error} = \frac{\text{Measured value} - \text{True value}}{True\ value} \times 100$$

RESULTS:

1. It is observed that by changing value of load resistor , $I_o = I_{ref}$ as far as MOSFET Q_2 remains in ____________ region of operation.

2. It is also observed that by increasing the value of load resistor R_2 ; eventually decreases the value of V_{DS2}, making the MOSFET Q_2 to enter into triode region, hence the difference in currents I_o and I_{ref} can be seen in the table of measurements.

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Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 02

OBJECTIVE:

To OPERATE UNDER SUPERVISION The MOS differential Amplifier circuit

EQUIPMENT REQUIRED:

- D.C power supply
- Oscilloscope
- Multimeter
- MOSFET 2N7000
- Resistors

THEORY:

MOS transistors are used in all significant digital designs, mixed-signal designs, analog amplifier designs, etc

The MOSFET differential amplifiers are used as input stages in op-amps, video amplifiers, high-speed comparators, and many other analog-based circuits. MOSFET differential amplifiers provide a high input impedance for the input terminals. A properly designed differential amplifier with its current-mirror biasing stages is made from matched-pair devices to minimize imbalances from one side of the differential amplifier to the other.

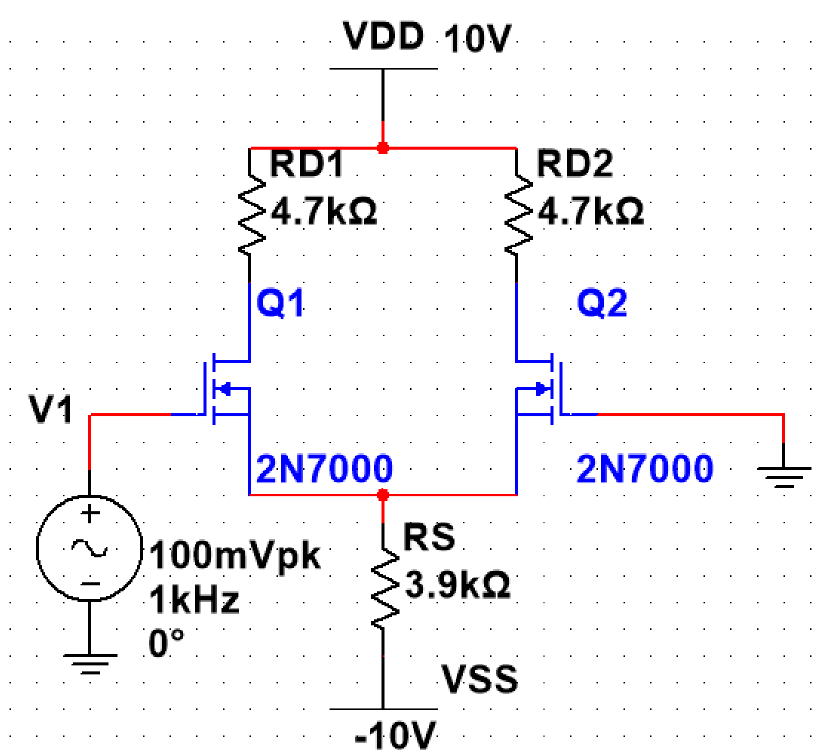

Figure 1. MOS Differential amplifier circuit diagram

PROCEDURE:

- Implement the MOS differential pair circuit shown in figure 1.
- First apply DC ground voltage to both inputs, i.e, $V_{G1}=V_{G2}$ = 0V(Common Mode)
- Observe the DC node voltages at drain (V_D) and source (V_S)
- Note readings as provided in observation table. .

OBSERVATIONS:

S.No	Input 1	Input 2	Differential input	Output 1	Output 2	Differential output
	V_{G1}	**V_{G2}**	**V_{G1}-V_{G2}**	**V_{D1}**	**V_{D2}**	**V_{D2}-V_{D1}**
1	50mV pk 1KHz	0V				
2	0V	50mV pk 1KHz				
3	50mV pk 1KHz(180)	50mV pk 1KHz				
	Common mode					
4	0V	0V				

RESULTS:

- The common mode output observed is………………
- The differential mode output observed, when AC input is applied : ………………
- The AC differential gain is ………………
- The differential pair can take both AC and DC signals at the input if applied within specified range
- The MOSFET must remain in saturation region

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Remarks	
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LAB SESSION 03

OBJECTIVE:

To OPERATE UNDER SUPERVISION the BJT circuit to identify type of transistor and mode of operation

EQUIPMENT REQUIRED:

- D.C power supply
- Multimeter
- Resistors
- Breadboard
- BJT 2N3904

THEORY:

A transistor is a solid state device made from semiconductor material with connections made at three or more points where the electrical characteristics are different. The term transistor comes from the words transfer and resistor. The term was adopted because it best describes the actual operation of transistor, the transfer of an input signal current from a low resistance circuit to a high resistance output circuit.

A transistor must be properly biased in order to operate as an amplifier. DC biasing is used to establish a steady level of transistor current and voltage called the dc operating point (Q-Point). Voltage divider bias provides good Q-point stability with a single polarity supply voltage. It is the most common bias circuit.

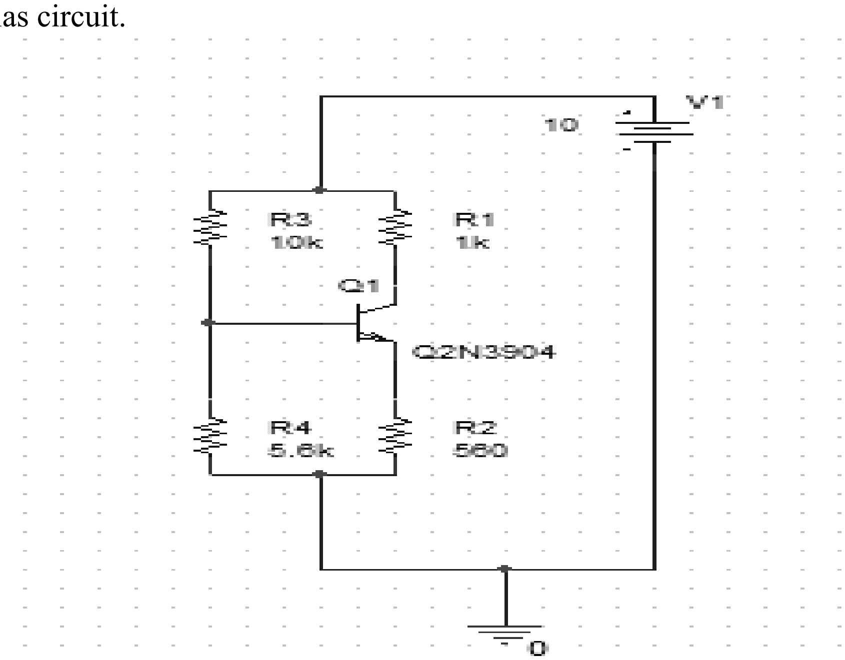

Fig.1: The Schematic diagram of voltage divider biased DC circuit for BJT operation

PROCEDURE:

- Implement the circuit in Fig. 1
- Measure the voltage readings at Base, Emitter and Collector

OBSERVATIONS:

Parameters	Measured value	Expected value
I_C		
V_E		
V_B		
V_C		
V_{CE}		

Mode of operation: ______________________________

CALCULATIONS:

RESULTS:

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LAB SESSION 04

OBJECTIVE:

To OPERATE UNDER SUPERVISION a class A power amplifier.

EQUIPMENT REQUIRED:

- Proto board
- Function Generator
- Digital Multi meter
- Power Supply
- Resistors
- Transistors: 1xQ2N3904
- Capacitors 2x10μF

THEORY:

An amplifier receives a signal from some pickup transducer or other input source and provides a larger version of the signal to some output device or to another amplifier stage. An input transducer signal is generally small (a few millivolts from a cassette or CD input, or a few microvolts from an antenna) and needs to be amplified sufficiently to operate an output device (speaker or other power-handling device).

In small-signal amplifiers, the main factors are usually amplification linearity and magnitude of gain. Since signal voltage and current are small in a small-signal amplifier, the amount of power-handling capacity and power efficiency are of little concern. A voltage amplifier provides voltage amplification primarily to increase the voltage of the input signal.

POWER AMPLIFIER:

Large-signal or power amplifiers, primarily provide sufficient power to an output load to drive a speaker or other power device, typically a few watts to tens of watts. One method used to categorize amplifiers is by class. Basically, amplifier classes represent the amount the output signal varies over one cycle of operation for a full cycle of input signal.

TYPES OF POWER AMPLIFIER:

Class A: The output signal varies for a full 360° of the input signal. Fig. 1 shows that this requires the Q -point to be biased at a level so that at least half the signal swing of the output may vary up and down without going to a high enough voltage to be limited by the supply voltage level or too low to approach the lower supply level, or 0 V in this description.

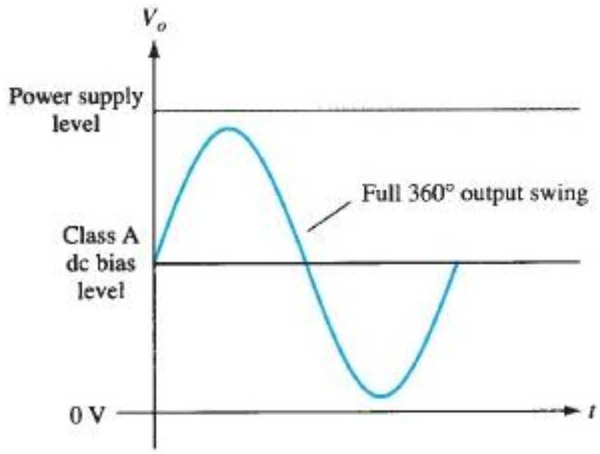

Fig.1: Class A Power Amplifier

AMPLIFIER EFFICIENCY:

The power efficiency of an amplifier, defined as the ratio of power output to power input. Class A amplifier, with dc bias at one-half the supply voltage level, uses a good amount of power to maintain bias, even with no input signal applied. This results in very poor efficiency, especially with small input signals, when very little ac power is delivered to the load. The maximum efficiency of a class A circuit, is only 25%

SERIES FED CLASS A POWER AMPLIFIER:

The simple fixed-bias circuit connection shown in Fig.3 can be used to discuss the main features of a class A series-fed amplifier. The only differences between this circuit and the small-signal version considered previously is that the signals handled by the large signal circuit are in the range of volts, and the transistor used is a power transistor that is capable of operating in the range of a few to tens of watts. As will be shown in this section, this circuit is not the best to use as a large-signal amplifier because of its poor power efficiency.
The beta of a power transistor is generally less than 100, the overall amplifier circuit using power transistors that are capable of handling large power or current while not providing much voltage gain.

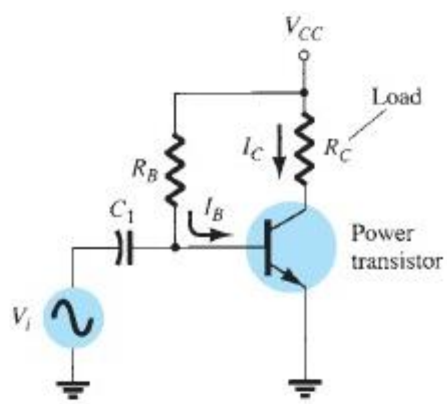

Fig.3 Series-fed class A large-signal amplifier.

DC BIAS OPERATION:

The dc bias set by V_{CC} and R_B fixes the dc base-bias current at

$$I_B = \frac{V_{CC} - 0.7V}{R_B}$$

with the collector current then being

$$I_C = \beta I_B$$

with the collector–emitter voltage then

$$V_{CE} = V_{CC} - I_C R_C$$

To appreciate the importance of the dc bias on the operation of the power amplifier, consider the collector characteristic shown in Fig.4 .A dc load line is drawn using the values of V_{CC} and R_C . The intersection of the dc bias value of I_B with the dc load line then determines the operating point (Q - point) for the circuit. The quiescent-point values are those calculated using Eqs.(1) through (3). If the dc bias collector current is set at one-half the possible signal swing (between 0 and V_{CC} > R_C), the largest collector current swing will be possible. Additionally, if the quiescent collector–emitter voltage is set at one-half the supply voltage, the largest voltage swing will be possible.

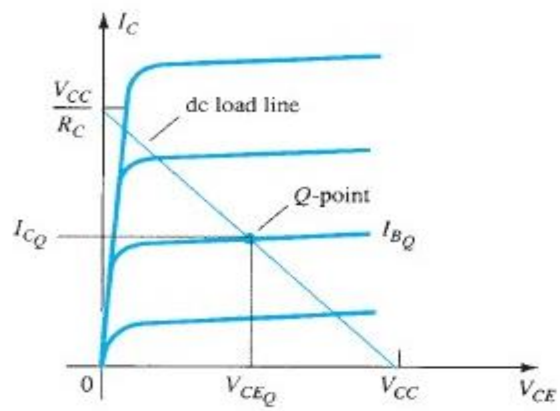

Fig.4 Transistor characteristic showing load line and Q-point.

AC OPERATION:

When an input ac signal is applied to the amplifier of Fig.3 , the output will vary from its dc bias operating voltage and current. A small input signal, as shown in Fig.5 , will cause the base current to vary above and below the dc bias point, which will then cause the collector current (output) to vary from the dc bias point set as well as the collector–emitter voltage to vary around its dc bias value. As the input signal is made larger, the output will vary further around the established dc bias point until either the current or the voltage reaches a limiting condition. For the current this limiting condition is either zero current at the low end or V_{CC}/R_Cat the high end of its swing. For the collector–emitter voltage, the limit is either 0 V or the supply voltage,V_{CC} .

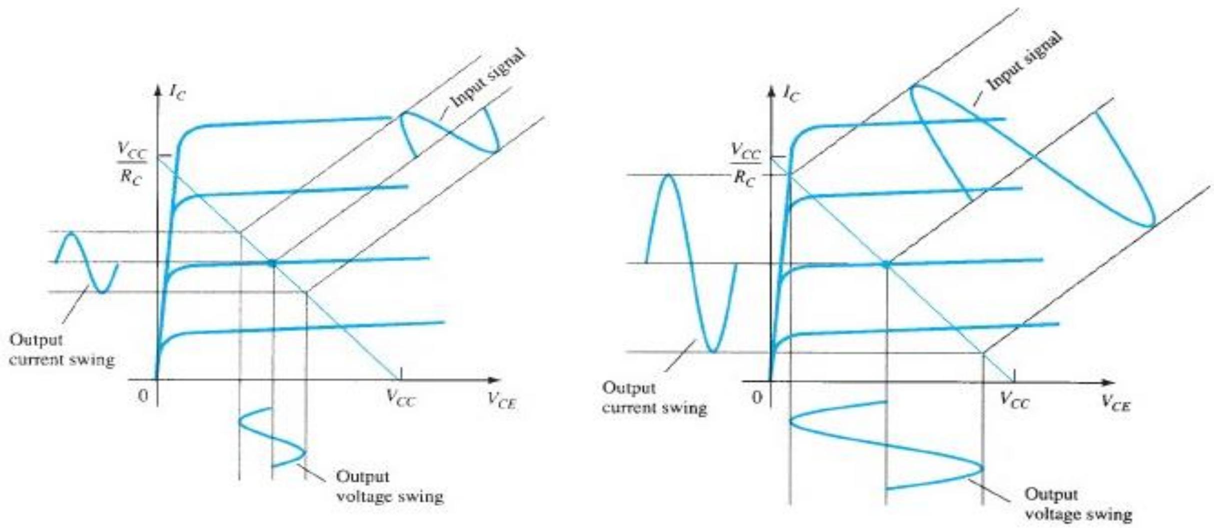

Fig.5 Amplifier input and output signal variation.

EFFICIENCY:

$$\%\ \eta = \frac{P_o\ (ac)}{P_i\ (dc)}$$

$$P_i = V_{cc} I_c$$

$$P_o(\text{ac}) = \frac{V_O(p-p)^2}{8\ R_L}$$

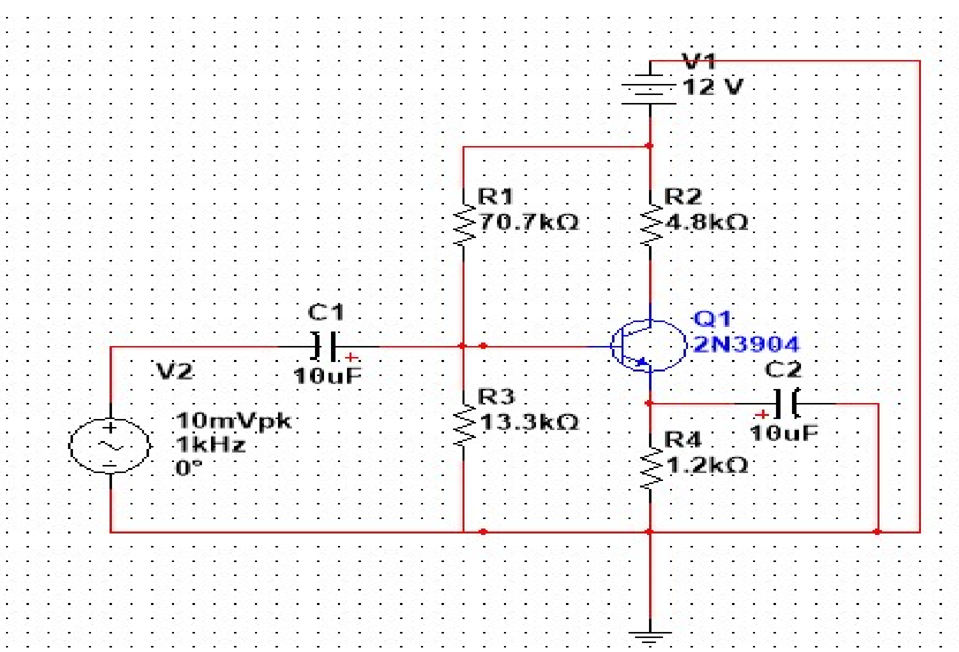

Fig. 6: Class A Power amplifier (practical circuit)

PROCEDURE:

1. Build the circuit as shown in figure 6.
2. Connect channel 1 of oscilloscope at the input and channel 2 at the output.
3. Apply power to the bread board and adjust the sine the wave output level of the generator at 50 mV peak-to-peaks at a frequency of 1 kHz.
4. Now carefully increase the peak-to-peak input signal so that the output peaks just clip off. Measure the peak to peak voltage across R_2 which is a 4.8 kΩ load resistor. Record the observations in table.
5. Finally, compute the percent efficiency (%η) of the amplifier.

USEFUL FORMULA:

$$\eta = \frac{{V_{O(P-P)}}^2 / 8\,R_L}{V_{CC} I_C}$$

OBSERVATIONS:

Parameter	Measured Value
$V_{O(P-P)}$	
V_{CC}	
I_C	

CALCULATIONS:

RESULTS:

The efficiency of class A amplifier is found to be: ____________

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LAB SESSION 05

OBJECTIVE:

To IMITATE a class B push-pull power amplifier

EQUIPMENT REQUIRED:

- Proto board
- Function Generator
- Digital Multi meter
- Power Supply
- Resistors
- Capacitors 2x10µF, 220uF
- Diodes: 2x 1N914 or 1N4148
- Transistors: 1xQ2N3904, 1xQ2N3906

THEORY:

POWER AMPLIFIER:

Power Amplifiers are large signal amplifiers. This generally means that a much larger portion of the load line is used during signal operation than in a small signal amplifier.

Power amplifiers are normally used as the final stage of a communications receiver or transmitter to provide signal power to speakers or to transmitting antenna.

CLASS B PUSH-PULL AMPLIFIERS:

When an amplifier is biased at cut-off so that it operates in the linear region for 180^{O} of the input cycle and is in cutoff for 180^{O}, it is a class B amplifier. The primary advantage of a class B amplifier over a class A amplifier is that either one is more efficient than a class A amplifier; you can get more output power for a given amount of input power. A disadvantage of class B is that it is more difficult to implement the circuit in order to get a linear reproduction of the input waveform.

CLASS B OPERATION:

The class B operation is illustrated in fig.1. Where the output is shown relative to the input in terms of time (t)

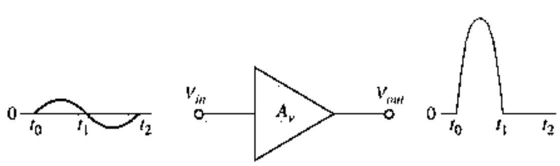

Fig. 1: Basic Class B Amplifier operation

THE Q-POINT IS AT CUTOFF:

The class B amplifier is biased at the cutoff point so that $I_{CQ} = 0$ and $V_{CEQ} = V_{CE\ (cutoff)}$. It is brought out of cutoff and operates in its linear region when the input signal drives the transistor into conduction. This is illustrated in fig.2 with an emitter-follower circuit where, the output is not replica of the input.

CLASS B PUSH-PULL OPERATION:

The circuit in fig.2 only conducts for the positive half cycle of the cycle. To amplify the entire cycle, it is necessary to add a second class B amplifier that operates on the negative half of the cycle. The combination of two class B amplifiers working together is called push-pull operation.
There are two common approaches for using for using push-pull amplifiers to reproduce the entire waveform. The first approach uses transformer coupling. The second uses two complementary symmetry transistors; these are a matching pair of npn/pnp BJTs or a matching pair of n-channel/p-channel FETs.

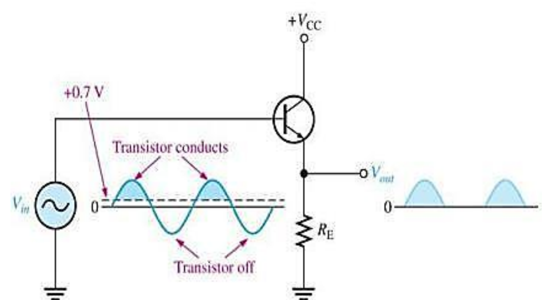

Fig.2: Common collector class B amplifier

TRANSFORMER COUPLING:

Transformer coupling is illustrated in fig.3.The input transformer is center-tapped secondary that is connected to ground, producing phase inversion of one side with respect to the other. The input transformer thus converts the input signal of two out-of-phase signals for the transistors. Notice that both transistors are npn types. Because of the signal inversion, Q1 will conduct on the positive part of the cycle and Q2 will conduct on the negative part. The output transformer combines the signals by permitting current in both the directions, even though one transistor is always cut-off. The positive power supply signal is connected to the center tap of the output transformer.

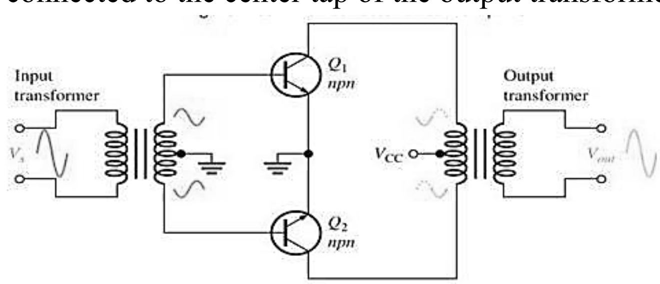

Fig.3: Transformer coupled push-pull amplifiers

COMPLEMENTARY SYMMETRY TRANSISTORS:

Fig.4 shows a push-pull class B amplifier using two emitter-followers and both positive and negative power supplies. This is a complementary amplifier because one emitter-follower uses an npn transistor and the other a pnp, which conduct on opposite alterations of the input cycle. In this circuit there is no dc base bias voltage (V_B=0). Thus, only the signal voltage drives the transistors into conduction. Transistor Q_1 conducts during the positive half of the input cycle, and Q_2 conduct during the negative half.

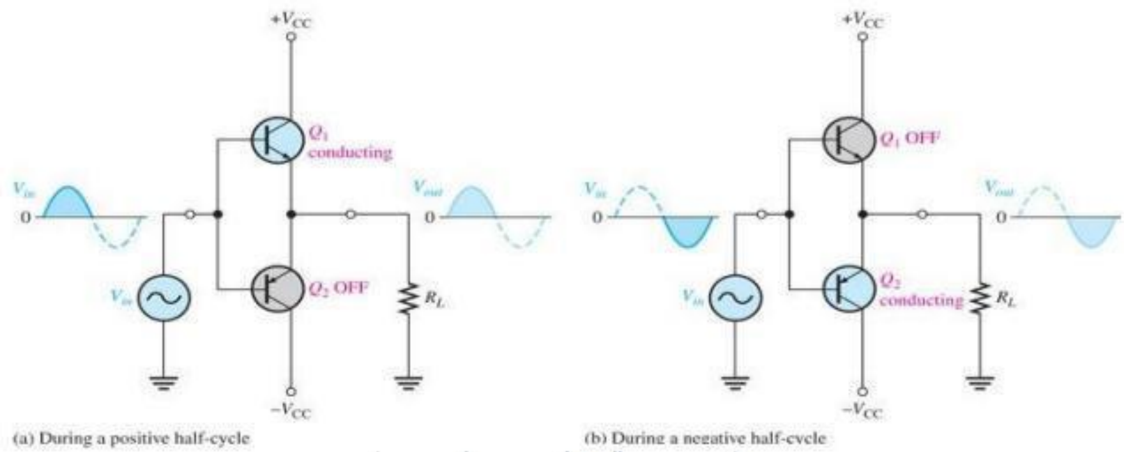

Fig.4: Class B push-pull ac operation.

CROSSOVER DISTORTION:

When the dc base voltage is zero, both transistors are off and the input signal voltage must exceed V_{BE} before a transistor conducts. Because of there is a time interval between the positive and negative alternations of the input when neither transistor is conducting as shown in fig.5. The resulting distortion in the output waveform is called crossover distortion.

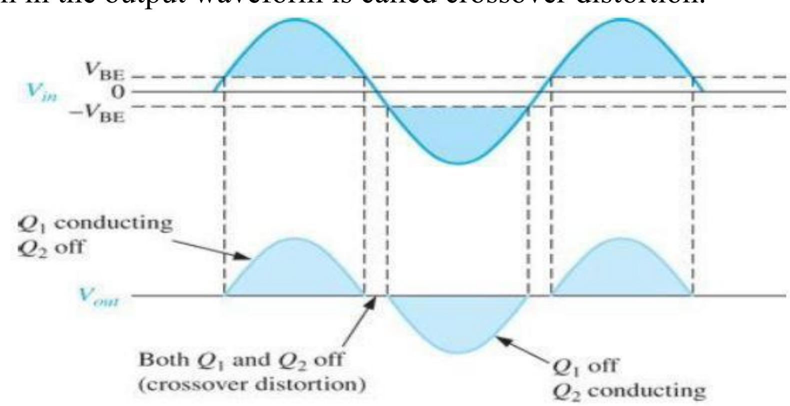

Fig.5: Crossover distortion in a class B push-pull amplifier

EFFICIENCY:

Efficiency is defined as the ratio of AC output power to DC input power .So

$$\eta = \frac{\pi * V_{out}\ (peak)}{4 * V_{cc}}$$

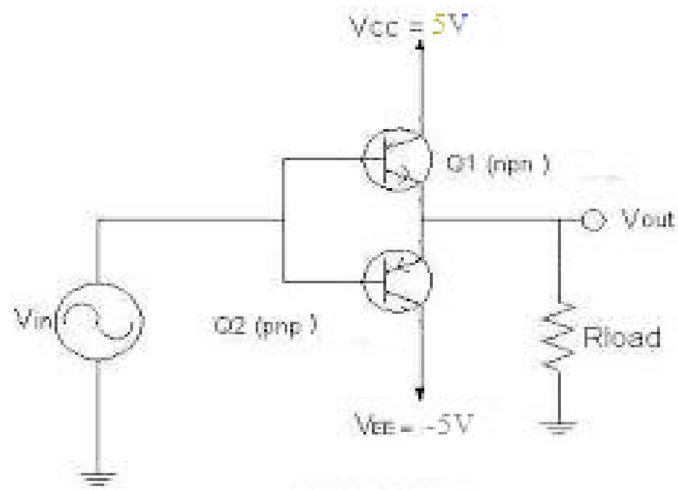

Fig. 6: Class B push-pull Power amplifier (practical circuit)

PROCEDURE:

1. Build the circuit as shown in figure 6.
2. Connect channel 1 of your oscilloscope at the input and channel 2 at the output.
3. Apply power to the bread board and adjust the sine the wave output level of the generator at 6 V peak-to-peaks at a frequency of 1 kHz.
4. Now carefully increase the peak-to-peak input signal so that the output peaks just clip off. Measure the peak to peak voltage across the 1kΩ load resistor .Record the observations in table 1.
5. Finally, compute the percent efficiency (%η) of your amplifier.

USEFUL FORMULA:

$$\eta = \frac{\pi * Vout\ (peak)}{4 * Vcc}$$

OBSERVATIONS:

Class B Amplifier Efficiency

Parameter	**Measured Value**
V_O(peak)	
Vcc	

CALCULATIONS:

RESULT:

The efficiency of class B amplifier is found to be: ……………….

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NED University of Engineering & Technology
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Course Code and Title: EL-201 Electronic Devices and Circuits

Psychomotor Domain Assessment Rubric-Level P3					
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Laboratory Session No. Date: _______________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 06

OBJECTIVE:
To IMITATE a class AB push-pull power amplifier

EQUIPMENT REQUIRED:
- Proto board
- Function Generator
- Digital Multi meter
- Power Supply
- Resistors
- Capacitors 2x10µF, 220uF
- Diodes: 2x 1N914 or 1N4148
- Transistors: 1xQ2N3904, 1xQ2N3906

THEORY:

CLASS AB PUSH-PULL AMPLIFIERS:
When an amplifier is biased at cut-off so that it operates in the linear region for 180^{o} of the input cycle and is in cutoff for 180^{o}, it is a class B amplifier. Class AB amplifiers are biased to conduct for slightly more than 180^{o}.The primary advantage of a class B or class AB amplifier over a class A amplifier is that either one is more efficient than a class A amplifier; you can get more output power for a given amount of input power. A disadvantage of class B or class AB is that it is more difficult to implement the circuit in order to get a linear reproduction of the input waveform.

CLASS B OPERATION:
The class B operation is illustrated in fig.1. Where the output is shown relative to the input in terms of time (t)

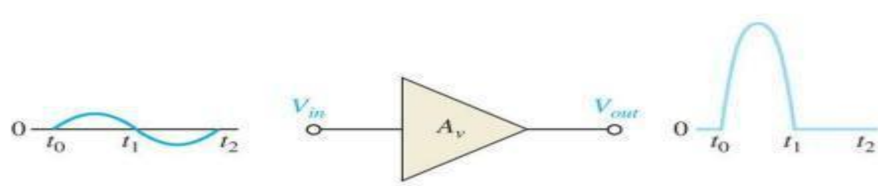

Fig. 1: Basic Class B Amplifier operation

THE Q-POINT IS AT CUTOFF:

The class B amplifier is biased at the cutoff point so that I_{CQ}= 0 and V_{CEQ} = $V_{CE\ (cutoff)}$. It is brought out of cutoff and operates in its linear region when the input signal drives the transistor into conduction. This is illustrated in fig.2 with an emitter-follower circuit where, the output is not replica of the input.

CROSSOVER DISTORTION:

When the dc base voltage is zero, both transistors are off and the input signal voltage must exceed V_{BE} before a transistor conducts. Because of there is a time interval between the positive and negative alternations of the input when neither transistor is conducting as shown in fig.2. The resulting distortion in the output waveform is called crossover distortion.

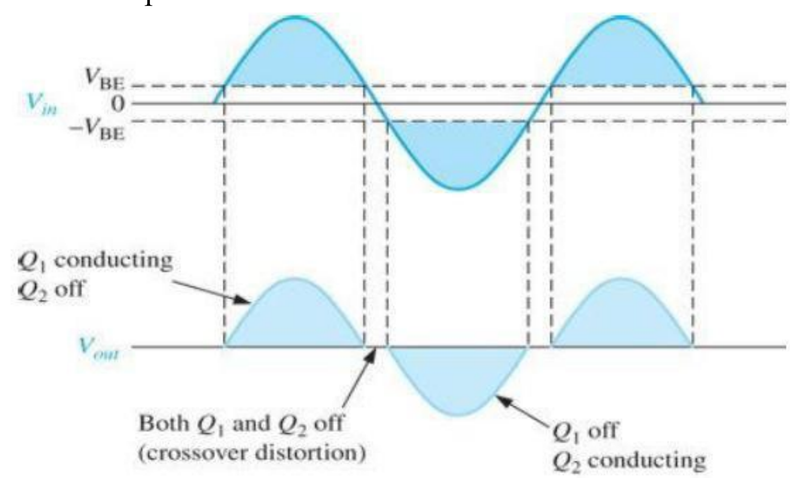

Fig.2: Crossover distortion in a class B push-pull amplifier

BIASING THE PUSH-PULL AMPLIFIER FOR CLASS AB OPERATION:

To overcome crossover distortion, the biasing is adjusted to overcome the V_{BE} of the transistors; this result in a modified form of operation called class AB. In class AB operation, the push-pull stages are biased into slight conduction, even when no input signal is present. This can be done with a voltage-divider and diode arrangement, as shown in fig.3.When the diode characteristics of both diodes are closely matched to the characteristics of the transistor emitter-base junctions, the current in the diodes and the current in the transistors are the same; this is a current mirror. In the bias path both the resistors are also of equal value.

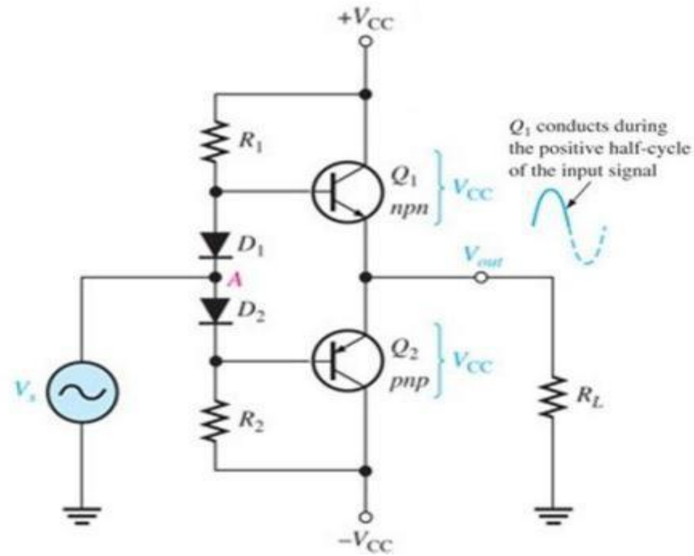

Fig.3: Biasing the push-pull amplifier to eliminate crossover distortion

The AC load line for the class AB amplifier is shown in fig.7

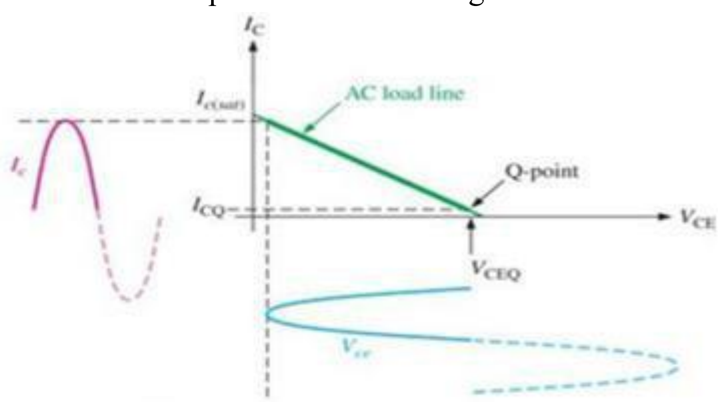

Fig.4: Load lines for a complementary symmetry push-pull amplifier. Only the load lines for the npn transistor are shown

Under maximum condition, $Q_1$and Q_2 is alternatively driven from near cutoff to near saturation that is for Q_1 from 0V to $+V_{CC}$ and for Q2 from 0V and to $-V_{CC}$. The main advantage of class B/AB amplifier over the class A is that there is very little current in the transistor when there is no input signal .This results in low power dissipation when there is no signal.

SINGLE-SUPPLY PUSH-PULL AMPLIFIER:

Push-Pull amplifiers using complementary symmetry transistors can be operated from a single voltage source as shown in fig.8.The circuit operation is the same as described previously, except the bias is set to force the output emitter voltage to be $V_{CC}/2$ instead of 0v used with two supplies. Because the output is not biased at 0V capacitive coupling for the input and output is necessary to block the bias voltage from the source and the load resistor .Ideally the output voltage can swing from zero to V_{CC}, but in practice it does not quite reach these ideal values.

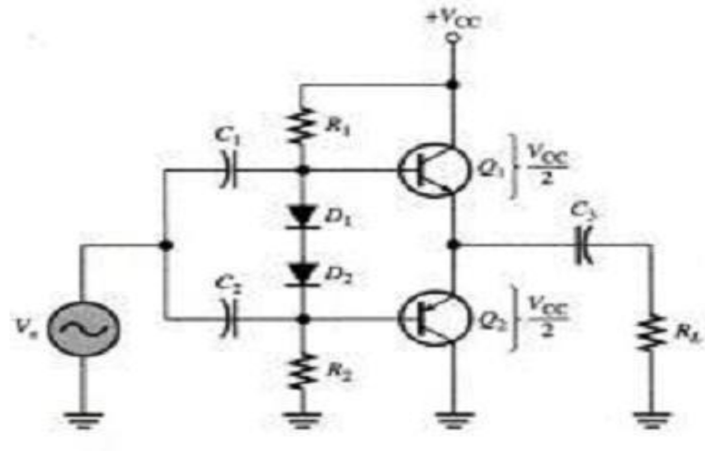

Fig.5:Single-ended push-pull Class B Power Amplifier

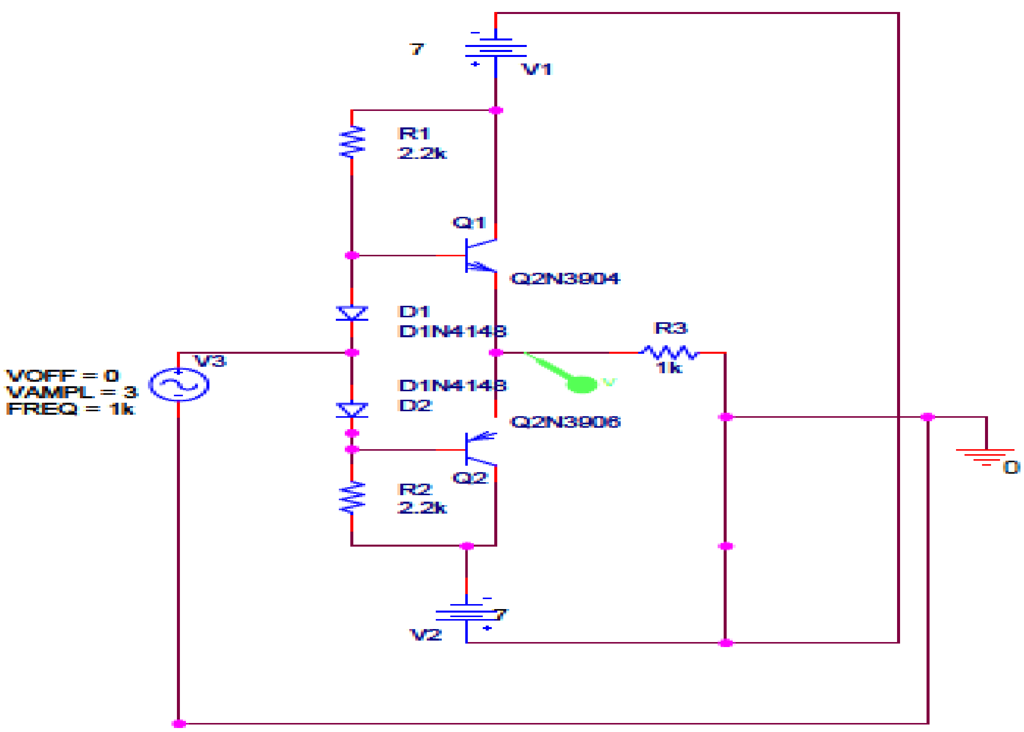

Fig. 6: Class B push-pull Power amplifier (practical circuit)

PROCEDURE

1. Build the circuit as shown in figure 6.
2. Connect channel 1 of your oscilloscope at the input and channel 2 at the output.
3. Apply power to the bread board and adjust the sine the wave output level of the generator at 6 V peak-to-peaks at a frequency of 1 kHz. Observe amplifier's input and output waveform. Measure the base-to-emitter voltages required for both transistor to become forward biased, recording these values in table .
4. Now carefully increase the peak-to-peak input signal so that the output peaks just clip off. Measure the peak output voltage just before the output clips off.
5. Finally, compute the percent efficiency (%η) of your amplifier, and compare it with the theoretical efficiency slightly less than 78.5% of a class B amplifier. If a value greater than 78.5% is calculated, then repeat the steps trying to determine the source of your error.

USEFUL FORMULA:

$$\eta = \frac{\pi * V_{out}\,(peak)}{4 * V_{cc}}$$

OBSERVATION:

Table : Voltage Divider Bias with no crossover distortion

Parameter	Measured Value
V_{BE1}	
V_{BE2}	

CALCULATION:

RESULT:

The efficiency of class AB amplifier is found to be: ………………

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Laboratory Session No. Date: ______________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 07

OBJECTIVE:
To IMITATE a class C power amplifier

EQUIPMENT REQUIRED:
- Proto board
- Function Generator
- Digital Multi meter
- Power Supply
- Resistors
- Capacitors 1x 0.02uF, 1x 0.01uF, 1x 0.1uF
- Inductor 1x 2mH
- Transistors: 1xQ2N3904,

THEORY:
CLASS C POWER AMPLIFIER:
Class C amplifiers are biased so that conduction occurs for much less than 180°. Class C amplifiers are more efficient than either class A or push-pull class B and class AB, which means that more output power can be obtained from class C operation. The output amplitude is a nonlinear function of the input, so class C amplifiers are not used for linear amplification. They are generally used in radio frequency (RF) applications, including circuits, such as oscillators, that have a constant output amplitude, and modulators, where a high-frequency signal is controlled by a low-frequency signal.

BASIC CLASS C OPERATION:
The basic concept of class C operation is illustrated in Figure 1.

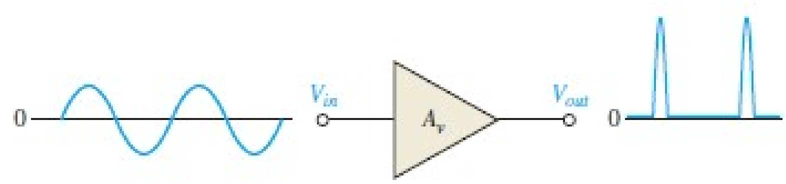

Fig.1 Basic class C amplifier operation (non-inverting).

A common-emitter class C amplifier with a resistive load is shown in Figure 2(a). A class C amplifier is normally operated with a resonant circuit load, so the resistive load is used only for the purpose of illustrating the concept. It is biased below cutoff with the negative V_{BB} supply.
The ac source voltage has a peak value that is slightly greater than $|V_{BB}| + V_{BE}$ so that the base voltage exceeds the barrier potential of the base-emitter junction for a short time near the positive peak of each cycle, as illustrated in Figure 2(b). During this short interval, the transistor is turned on. When the entire ac load line is used, as shown in Figure 2(c), the ideal maximum collector current is $I_{C(sat)}$, and the ideal minimum collector voltage is $V_{ce\,(sat)}$.

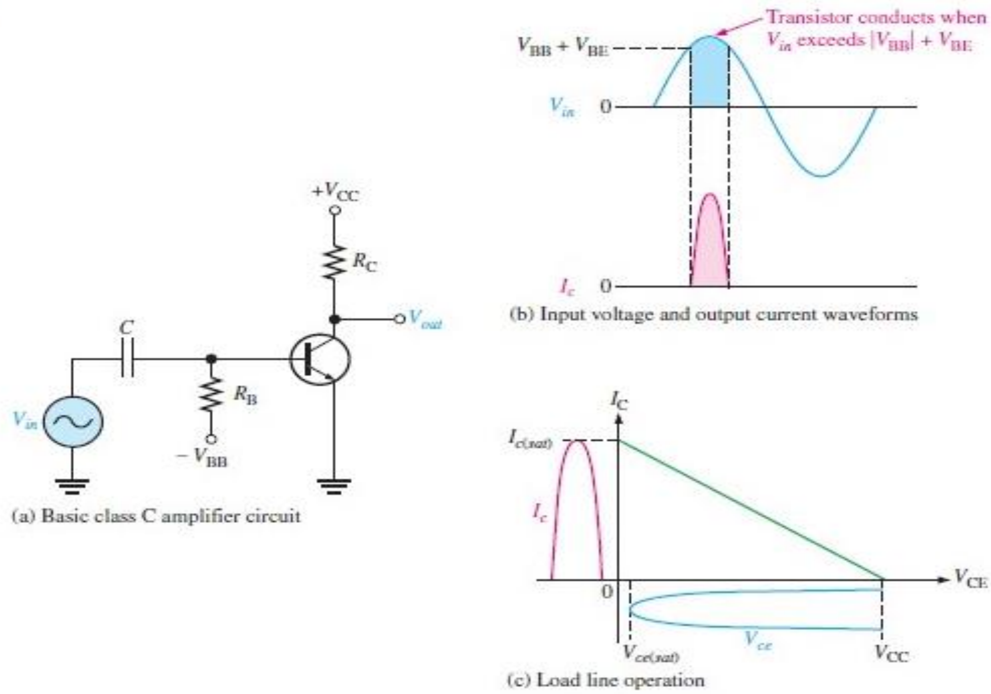

Fig.2: Basic class C operation.

POWER DISSIPATION:

The power dissipation of the transistor in a class C amplifier is low because it is on for only a small percentage of the input cycle. Figure 3(a) shows the collector current pulses. The time between the pulses is the period (*T)* of the ac input voltage. The collector current and the collector voltage during the *on* time of the transistor are shown in Figure 3(b). To avoid complex mathematics, we will assume ideal pulse approximations. Using this simplification, if the output swings over the entire load, the maximum current amplitude is $I_{C(sat)}$ and the minimum voltage amplitude is $V_{ce\,(sat)}$ during the time the transistor is on. The power dissipation during the *on* time is, therefore,

$$P_{D(on)} = I_{c\,(sat)} V_{ce\,(sat)}$$

The transistor is on for a short time, *t*on, and off for the rest of the input cycle. Therefore, assuming the entire load line is used, the power dissipation averaged over the entire cycle is:

$$P_{D(avg)} = \left(\frac{t_{on}}{T}\right) P_{D(on)} = \left(\frac{t_{on}}{T}\right) I_{c(sat)} V_{ce\,(sat)}$$

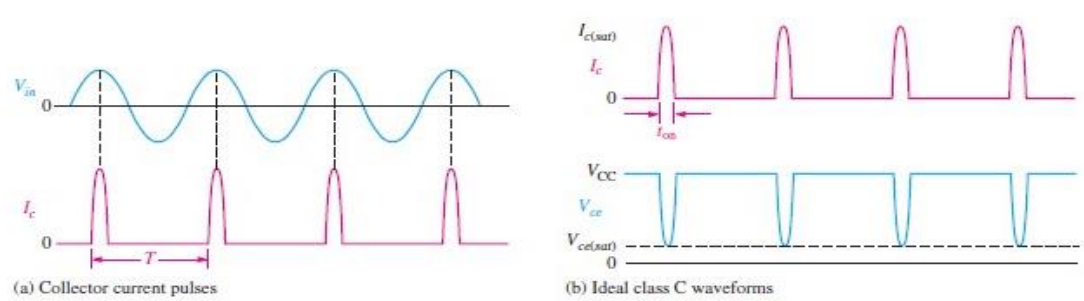

Fig. 3 : Class C waveforms.

TUNED OPERATION :

Because the collector voltage (output) is not a replica of the input, the resistively loaded class C amplifier alone is of no value in linear applications. It is therefore necessary to use a class C amplifier with a parallel resonant circuit (tank), as shown in Figure 4(a). The resonant frequency of the tank circuit is determined by the formula $f_r = {}^{1}/_{2\pi\sqrt{LC}}$. The short pulse of collector current on each cycle of the input initiates and sustains the oscillation of the tank circuit so that an output sinusoidal voltage is produced, as illustrated in Figure 4(b). The tank circuit has high impedance only near the resonant frequency, so the gain is large only at this frequency.

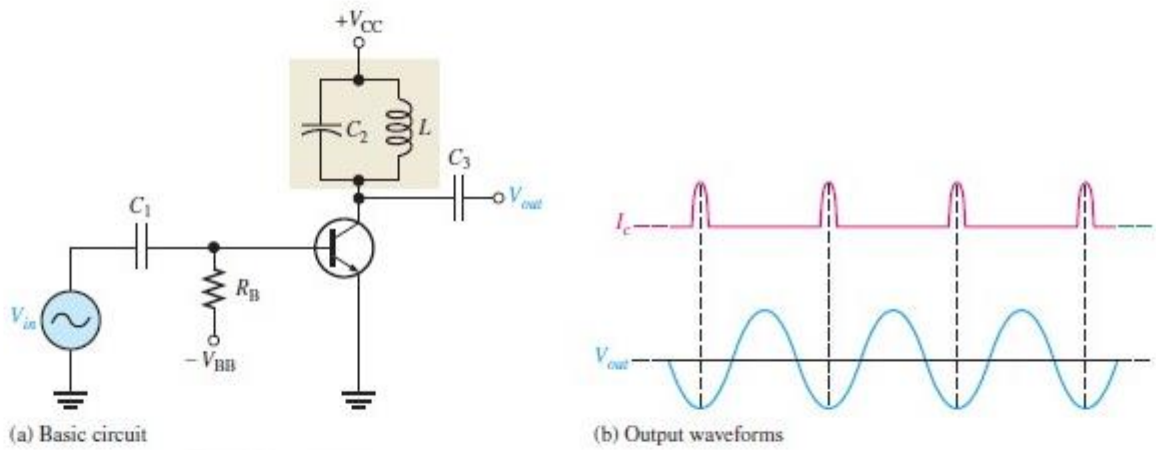

Fig.4 Tuned class C amplifier.

The current pulse charges the capacitor to approximately $+V_{CC}$, as shown in Figure 5(a). After the pulse, the capacitor quickly discharges, thus charging the inductor. Then, after the capacitor completely discharges, the inductor's magnetic field collapses and then quickly recharges C to near V_{CC} in a direction opposite to the previous charge. This completes one half-cycle of the oscillation, as shown in parts (b) and (c) of Figure 5. Next, the capacitor discharges again, increasing the inductor's magnetic field. The inductor then quickly recharges the capacitor back to a positive peak slightly less than the previous one, due to energy loss in the winding resistance. This completes one full cycle, as shown in parts (d) and (e) of Figure 5. The peak-to-peak output voltage is therefore approximately equal to $2V_{CC}$.

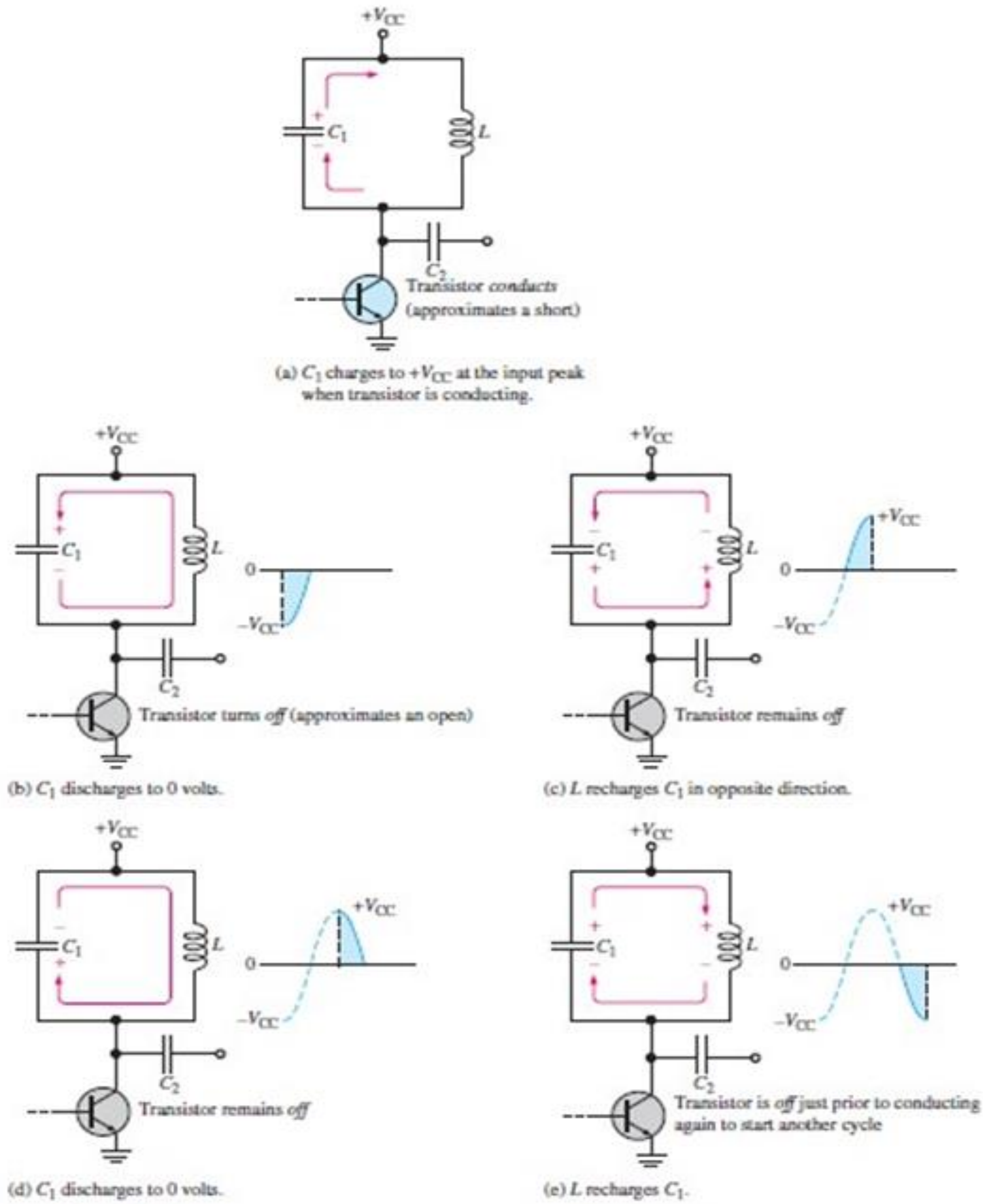

Fig. 5 : Resonant circuit action.

The amplitude of each successive cycle of the oscillation will be less than that of the previous cycle because of energy loss in the resistance of the tank circuit, as shown in Figure 6(a), and the oscillation will eventually die out. However, the regular recurrences of the collector current pulse re-energize the resonant circuit and sustain the oscillations at a constant amplitude. When the tank circuit is tuned to the frequency of the input signal (fundamental), reenergizing occurs on each cycle of the tank voltage, V_r , as shown in Figure 6(b).

When the tank circuit is tuned to the second harmonic of the input signal, re-energizing occurs on alternate cycles as shown in Figure 6(c). In this case, a class C amplifier operates as a frequency multiplier (x2). By tuning the resonant tank circuit to higher harmonics, further frequency multiplication factors are achieved.

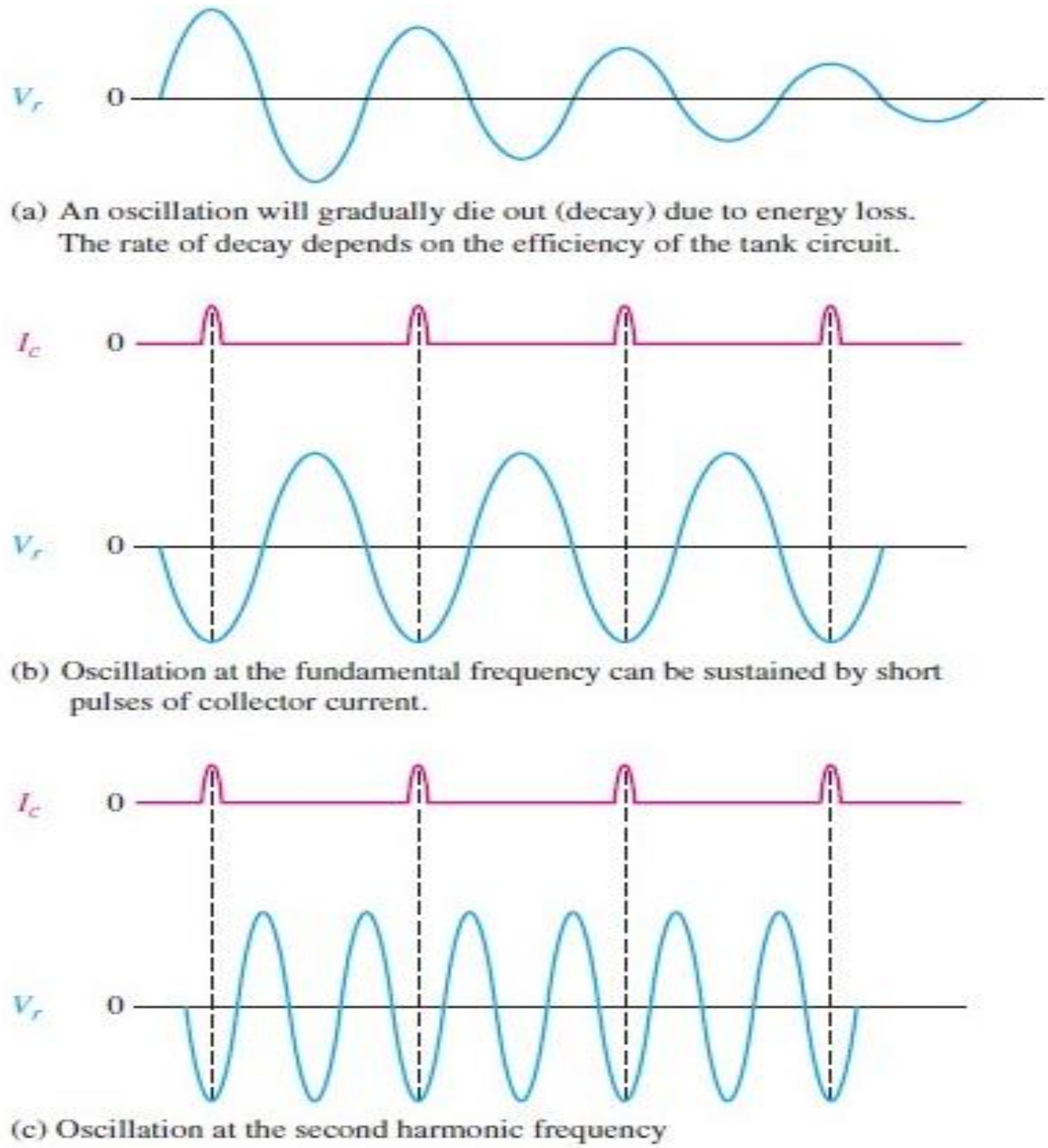

Fig. 6 :Tank circuit oscillations. $\boldsymbol{V_r}$ is the voltage across the tank circuit.

MAXIMUM OUTPUT POWER:

Since the voltage developed across the tank circuit has a peak-to-peak value of approximately $2V_{CC}$, the maximum output power can be expressed as

$$P_{out} = \frac{{V_{rms}}^2}{R_C} = \frac{(0.707\ V_{CC})^2}{R_C}$$

$$P_{out} = \frac{0.5V^2{}_{CC}}{R_C}$$

R_C is the equivalent parallel resistance of the collector tank circuit at resonance and represents the parallel combination of the coil resistance and the load resistance. It usually has a low value. The total power that must be supplied to the amplifier is

$$P_T = P_{out} + P_{D(avg)}$$

Therefore, the efficiency is

$$\eta = \frac{P_{out}}{P_{out} + P_{D(avg)}}$$

When $P_{out} > P_{D(avg)}$, the class C efficiency closely approaches 1 (100 percent).

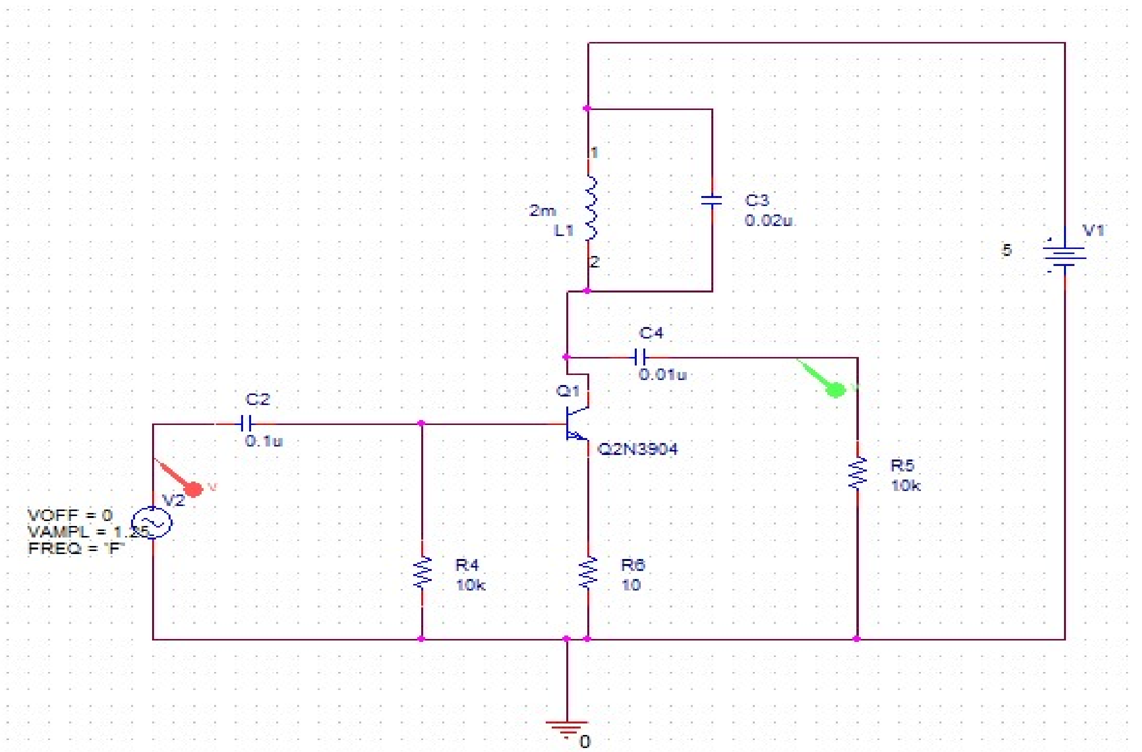

Fig.7: Class C Power Amplifier (Practical Circuit)

For the circuit in Fig 7.

- Simulate to find out resonant frequency. Give AC Sweep with $v_{in} = 1.25V$, showing waveform of Output voltage versus Frequency, with frequency range from 1Hz to 10GHz.The highest peak will give you the resonant frequency.
- Implement the hardware circuit as shown in figure 7. and apply the input signal voltage of amplitude 1.25 V and frequency equivalent to the resonant frequency calculated by the formula and observed by simulations.

OBSERVATIONS:

Parameter	Measured Value
f_r	
V_o(peak-peak)	

CALCULATIONS:

$$f_r = {}^{1}\!/_{2\pi\sqrt{LC}}$$

RESULTS:

The resonant frequency of Class C Power amplifier is found to be: ………………

The output peak to peak voltage is found out to be: ………………………………..

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Laboratory Session No. Date: ______________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 08

OBJECTIVE:

To OPERATE UNDER SUPERVISION Common Source Amplifier circuit

EQUIPMENT REQUIRED:

- Protoboard
- Function Generator
- Digital Multimeter
- Power Supply
- Resistors
- Transistors: 1 x 2N7000
- Capacitors

THEORY:

BACKGROUND:

MOS transistor is a voltage controlled device, where gate voltage modulates the channel resistance and voltage between drain and source determines current flow between the drain and source terminals. Like BJT, MOS transistor can perform as amplifier and as electronic switch. MOS comes in two different flavors, as NMOS and as PMOS.

SMALL-SIGNAL AMPLIFIER DESIGN AND BIASING:

If a small time-varying signal is superimposed on the DC bias at the input (gate or base terminal), then under the right circumstances the transistor circuit can act as a linear amplifier. Figure 1 illustrates the situation appropriate to a MOSFET common-source amplifier. The transistor is first biased at a certain DC gate bias to establish a desired drain current, shown as the "Q"-point (quiescent point) Figure 1a. A small AC signal of amplitude ΔV_{gs} is then superimposed on the gate bias, causing the drain current to fluctuate synchronously. If ΔV_{gs} is small enough, then we can approximate the I_d Vs V_{gs} curve by a straight line with a slope given by

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \text{ ……… (1)}$$

and then the drain current amplitude is $\Delta I_d = g_m \Delta V_{gs}$ With a drain resistor R_d as shown, the drain current is related to the output voltage by $V_{ds} = V_{dd} - I_d R_d$, so the AC output signal will be given by

$$\Delta V_{ds} = -\Delta I_d R_d = -g_m R_d \Delta V_{gs} \text{ ……….. (2)}$$

The voltage gain is therefore A_v = -g_m R_d . This can be appreciated graphically using a loadline approach as in Figure 1(b)

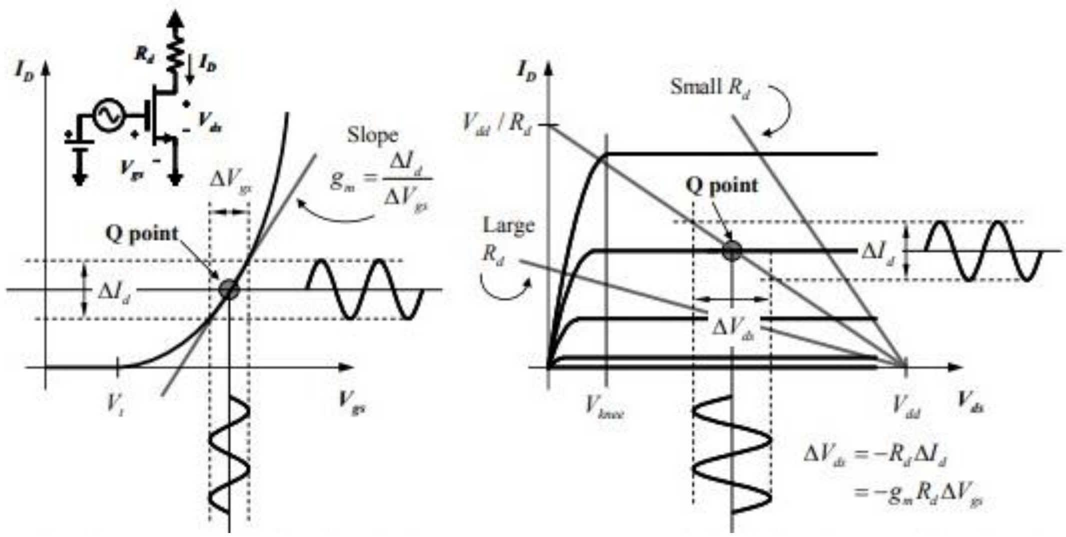


Figure 1 – Amplification in a MOSFET common-source configuration. (a) A small AC signal is superimposed on the DC gate bias, creating an AC drain current. (b) Same situation with a load-line superimposed on the output characteristic, showing how the AC drain current leads to an AC drain voltage and gain of -$g_m R_d$

Figure 1 also illustrates the importance of the bias point selection in the operation of transistor amplifiers. Figure 1a shows that the trans conductance (and hence the gain) will depend on the gate bias; this can be quantified using the I_d Vs V_{gs} characteristic

$$I_m = K_n(V_{gs} - V_t) \text{.........(3)}$$

Substituting (3) into (1) gives

$$g_m = 2K_n(V_{gs} - V_t) = 2\sqrt{K_n I_d} = \frac{2\, I_d}{V_{gs} - V_t} \text{........(4)}$$

To establish a large transconductance we must bias the device well above threshold. This is also important to insure that the transistor stays in saturation over the full AC cycle. However, there is a limit on gate bias and drain current imposed by the output characteristic and load resistor as shown in Figure 1(b). To allow for maximum output voltage swing the Q-point should lie approximately halfway between V_{dd} and the edge of the ohmic region, shown in the figure as V_{knee} . If the drain current or load resistor is too large, the device will swing into the ohmic region during operation leading to significant waveform distortion.

Another important consideration is the DC power dissipation in the device given by P=$V_{ds}I_d$. This power is dissipated as heat within the device so there is always a thermal limit on the dissipated power for every device and package. The datasheet will specify the maximum DC power P_{max} , maximum DC current I_{dmax}, and maximum DC voltage V_{dsmax} , to avoid destroying the device. These limits are superimposed on the output characteristic in Figure 2. The Q-point must be selected to lie below the shaded region in the figure.

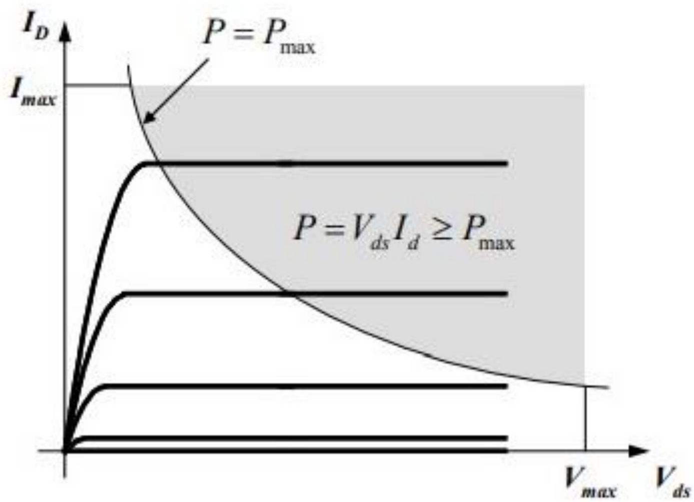


Figure 2 – Limitations on biasing imposed by maximum power considerations

Although the focus has been on MOSFETs in this discussion, it is important to recognize that the key conclusions above are largely independent of the choice of device. All transistors can be described by an output-current versus input-voltage characteristic like that in Figure 1a, and hence by a bias-dependent transconductance. Only the details of the voltage dependence will be different. For example, BJTs follow a diode-like exponential model; state-of-the-art short-channel MOSFETs have a nearly linear I_dVs V_{gs}characteristic and hence a constantg_m.

Lastly, note that the supply voltage is also an important variable. Generally a larger supply voltage is desirable for maximum voltage gain and maximum output voltage swing. This can be seen as follows: for a given drain current I_d , the drain resistor that is required for a drain bias of $V_{ds} \approx V_{dd}/2$

$$R_d = \frac{V_{dd}-V_{ds}}{I_d} \approx \frac{V_{dd}}{2I_d} \text{ …………(5)}$$

and thus the gain is given by

$$|A_v| = g_m R_d \approx \frac{g_m}{I_d}\frac{V_{dd}}{2} = V_{dd}\sqrt{\frac{K_n}{I_d}} \text{ ……………(6)}$$

The maximum gain scales with supply voltage for a specified device and current level.

MOSFET DESIGN PARAMETERS AND SUBTHRESHOLD CURRENTS :

For amplifier designs using any transistor (MOSFETs or BJTs) we need to know the transconductanceg_m. For MOSFETs, knowledge of the threshold voltage V_t and the current parameter K_n can be used to estimate g_m using (4), assuming the square-law device model (3) holds. A common method to estimate these parameters is to measure and plot the square-root of I_d Vs V_{gs}, which theoretically should yield a linear dependence,

$$\sqrt{I_d} = \sqrt{K_n}\,(V_{gs} - V_t)\ldots\ldots\ldots(7)$$

Thus the x-intercept if such a plot should yield the threshold voltage, and the slope should yield the current parameter.

The 2N7000, also in your parts kit, is at the other extreme: it is intended for larger currents and has an inherently larger transconductance. Consequently we need to operate this device closer to threshold in order to keep the DC currents low, an imperative from a DC power dissipation standpoint. The data sheet specifies a maximum DC power dissipation of 400mW; for drain voltages in the range of 2.5-5V (appropriate to supply voltages in the range of 5-10V) we would need to keep the currents below ~100mA.

Figure 3 shows a measured plot of $\sqrt{I_d}$ Vs V_{gs} for a 2N7000 for currents in this range; on this scale we can see a significant departure from the square-law characteristic. This device has gate lengths of around 2.5um.

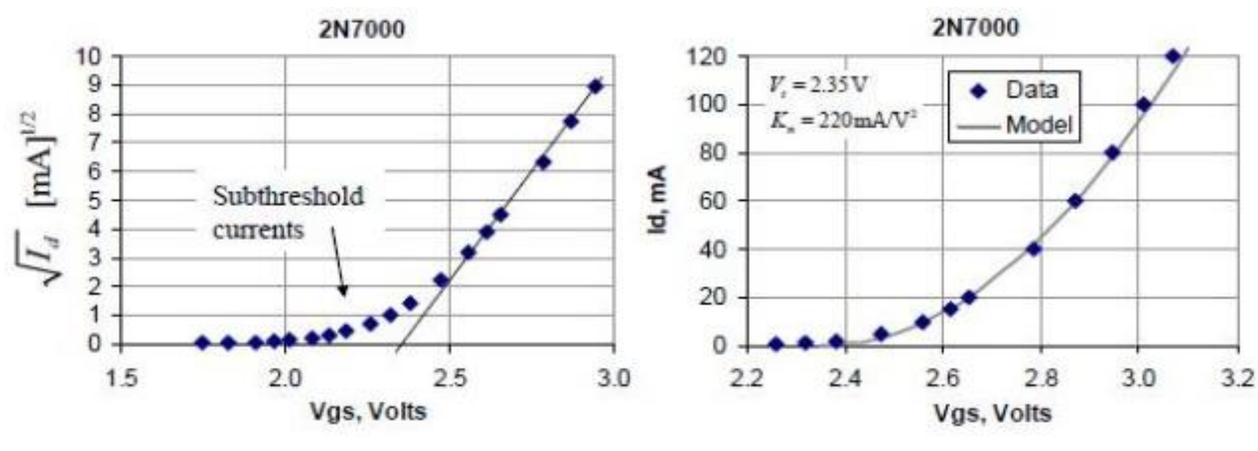


Figure 3 (a) Data for a 2N7000 device plotted as $\sqrt{I_d}$Vs V_{gs}, showing sub-threshold currents. (b) Same data set plotted as I_dVs V_{gs}, with comparison to the ideal model using given parameters (dashed line)

It means that we can't expect (3) to work well below currents of around 10mA. Above 10mA, the model seems to work reasonably well, and for the particular device shown in Figure 3 we find $V_t \approx$ 2.35V and $K_n \approx$ 220mA/V.
Remember, these parameters vary from device to device, and also may vary considerably from manufacturer to manufacturer. Figure 4 shows a comparison of characteristic from four different 2N7000 devices, two from one manufacturer, and two from another manufacturer, selected randomly. Not only does the threshold voltage vary, but it is apparent that the current parameter Kn also varies between manufacturers.

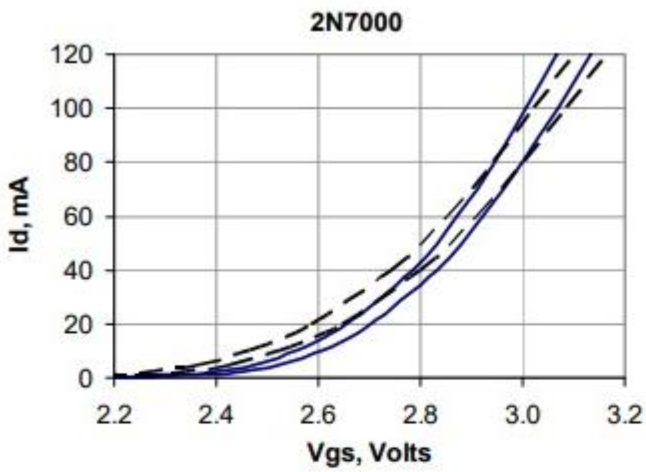


Figure 4 – Comparison of four different 2N7000 devices. Dashed lines and solid lines represent different manufacturers.

COMMON SOURCE AMPLIFIER:

In the circuit of Fig.5 the source terminal is connected to ground via a bypass capacitor, the input voltage signal is applied between the gate and ground, and the output voltage signal is taken between the drain and ground, across the resistance. This configuration, therefore, is called the grounded-source or common-source (CS) amplifier.

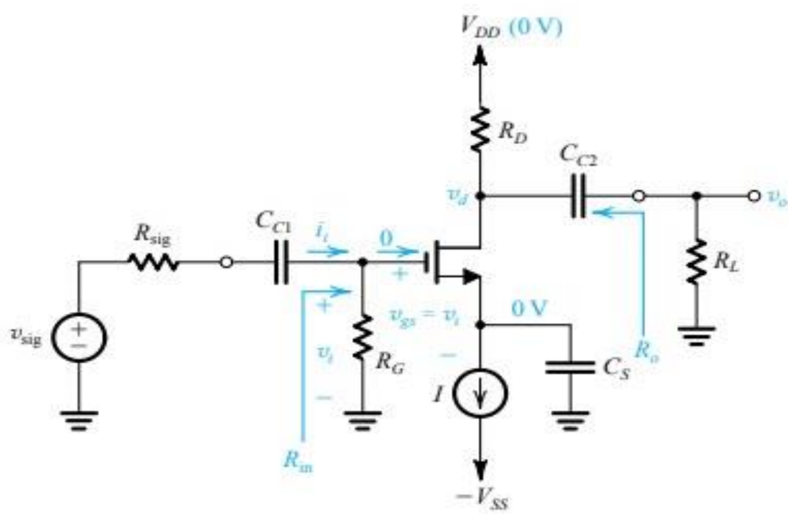


Fig.5: Common Source Amplifier

Hence the Common Source amplifiers have
1) a very high input resistance
2) a moderately high voltage gain
3) a relatively high output resistance.

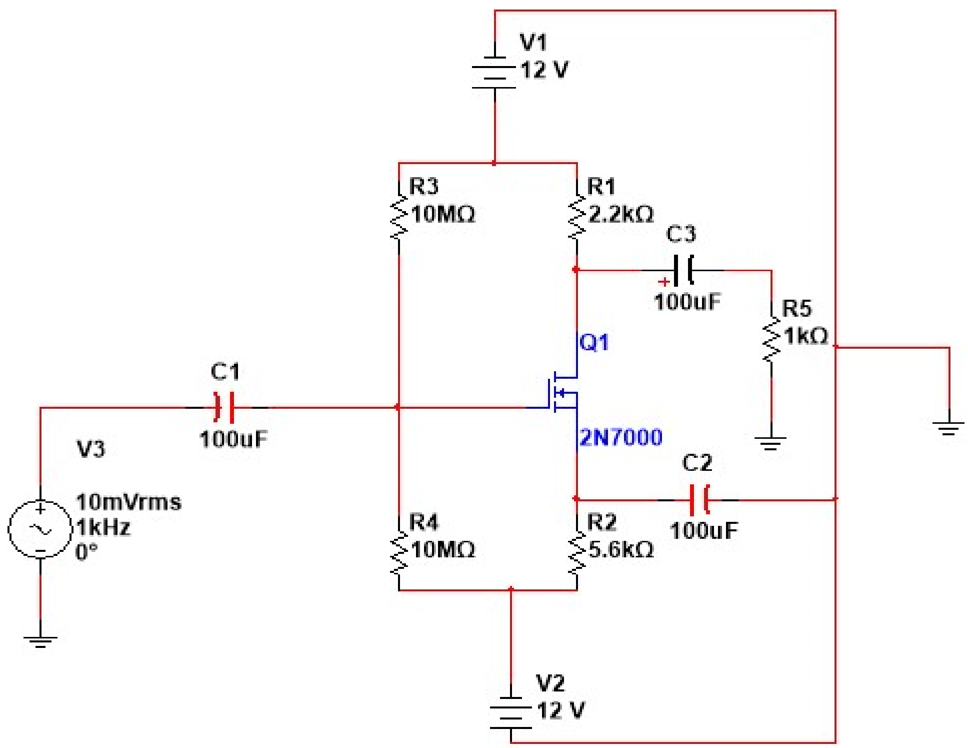


Fig 6: common source amplifier (practical circuit)

ANALYSIS:

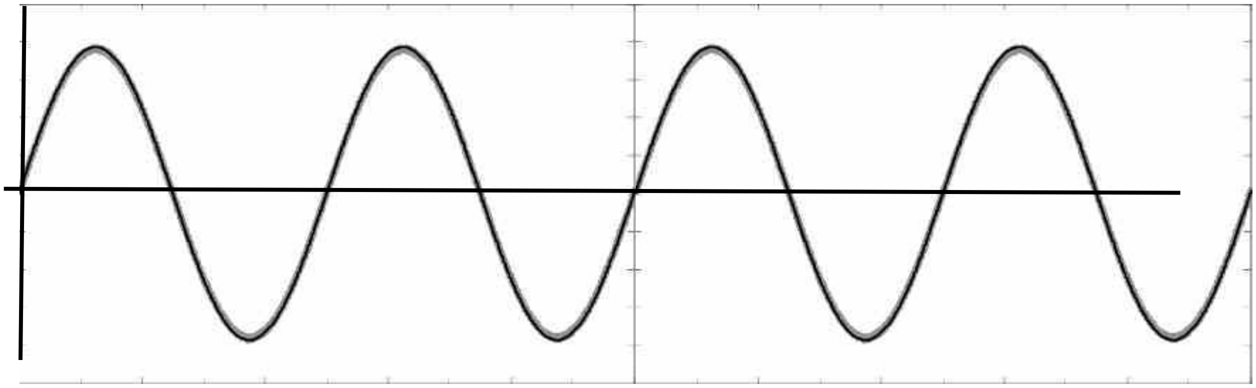
Implement the circuit of fig.6 on bread board. You are required to analyze a common source amplifier. Determine the gate, drain and source voltage. Justify that the circuit can be used as an amplifier and determine the gain of the circuit.

OBSERVATIONS:

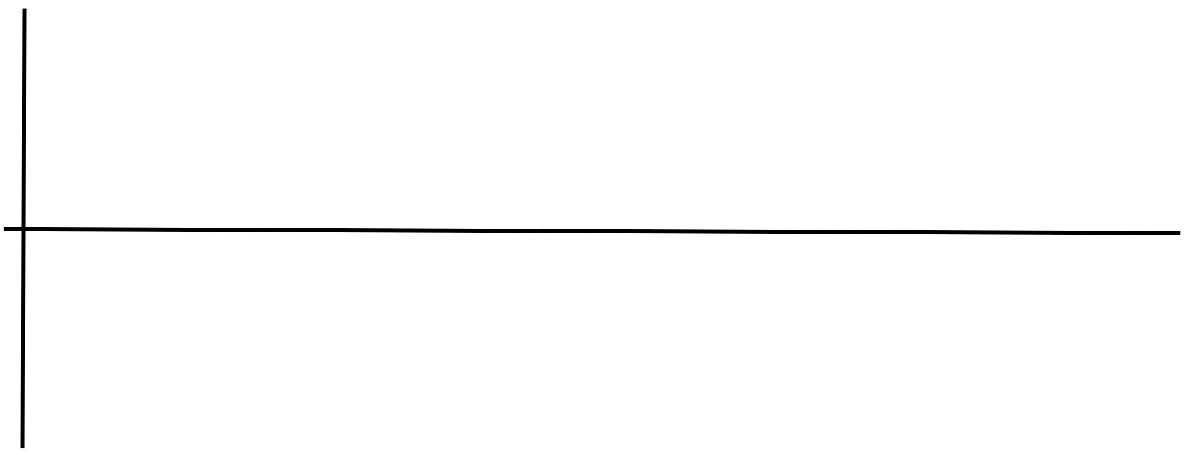
DC PARAMETERS:

Voltage readings	Calculated	Experimentally Measured
V_G (V)		
V_S (V)		
V_D (V)		
I_D (mA)		

Input Waveform:



Output Waveform:



v_{in} (at Source):

Calculated (theoretically)	Measured (Practically)

v_{out} (at Drain)

Calculated (theoretically)	Measured (Practically)

Gain Calculated:

Calculated (theoretically)	Measured (Practically)

CALCULATIONS:

$V_D = V_{DD} - I_D R_D$

RESULTS:

Phase Shift between input and output signal is: ……………………….

The gain of Common Source Amplifier is found to be: …………………

F/OBEM 01/05/00

NED University of Engineering & Technology
Department of Electronic Engineering
Course Code and Title: EL-201 Electronic Devices and Circuits

Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	Extent of Achievement				
	0	1	2	3	4
Equipment Identification Sensory skill to ***identify*** equipment and/or its component for a lab work.	Not able to identify the equipment.	--	--	--	Able to identify equipment as well as its components.
Equipment Use Sensory skills to ***demonstrate*** the use of the equipment for the lab work.	Doesn't demonstrate the use of equipment.	Slightly demonstrates the use of equipment.	Somewhat demonstrates the use of equipment.	Moderately demon strates the use of equipment.	Fully demonstrates the use of equipment.
Procedural Skills ***Displays*** skills to act upon sequence of steps in lab work.	Not able to either learn or perform lab work procedure.	Able to slightly understand lab work procedure and perform lab work.	Able to somewhat understand lab work procedure and perform lab work.	Able to moderately understand lab work procedure and perform lab work.	Able to fully understand lab work procedure and perform lab work.
Response Ability to ***imitate*** the lab work on his/her own.	Not able to imitate the lab work.	Able to slightly imitate the lab work.	Able to somewhat imitate the lab work.	Able to moderately imitate the lab work.	Able to fully imitate the lab work.
Observation's Use ***Displays*** skills to use the observations from lab work for experimental verifications and illustrations.	Not able to use the observations from lab work for experimental verifications and illustrations.	Slightly able to use the observations from lab work for experimental verifications and illustrations.	Somewhat able to use the observations from lab work for experimental verifications and illustrations.	Moderately able to use the observations from lab work for experimental verifications and illustrations.	Fully able to use the observations from lab work for experimental verifications and illustrations.
Safety Adherence Adherence to ***safety*** procedures.	Doesn't adhere to safety procedures.	Slightly adheres to safety procedures.	Somewhat adheres to safety procedures.	Moderately adheres to safety procedures.	Fully adheres to safety procedures.
Equipment Handling ***Equipment care*** during the use.	Doesn't handle equipment with required care.	Rarely handles equipment with required care.	Occasionally handles equipment with required care.	Often handles equipment with required care.	Handles equipment with required care.
Group Work ***Contributes*** in a group based lab work.	Doesn't participate and contribute.	Slightly participates and contributes.	Somewhat participates and contributes.	Moderately participates and contributes.	Fully participates and contributes.

Laboratory Session No. Date: ________________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 09

OBJECTIVE:
To IMITATE the frequency response of Common Source Amplifier

EQUIPMENT REQUIRED:
- Protoboard
- Function Generator
- Digital Multimeter
- Power Supply
- Resistors
- Capacitors
- Transistors: 1 x 2N7000

THEORY:

FREQUENCY RESPONSE :

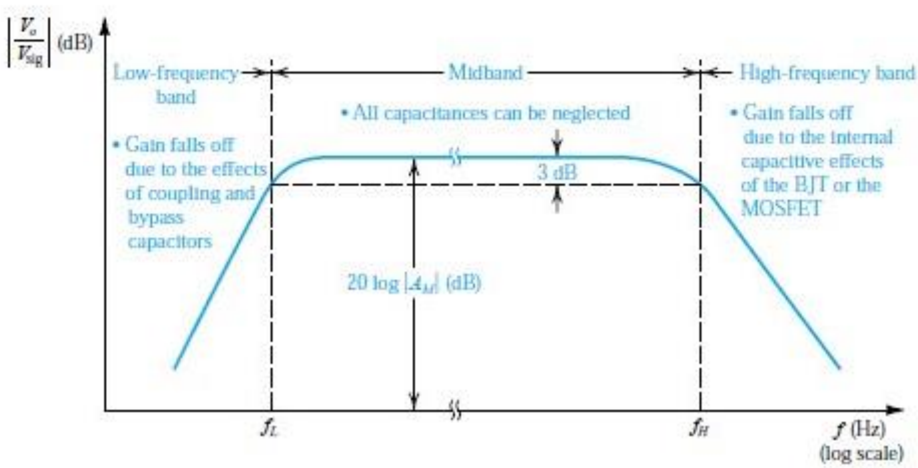


Fig 1. Sketch of the magnitude of the gain of a discrete-circuit MOS amplifier versus frequency. The graph delineates the three frequency bands relevant to frequency-response determination.

Fig. 1 indicates that at lower frequencies, the magnitude of the amplifier gain falls off. This occurs because the coupling and bypass capacitors no longer have low impedances. Although this can be true at midband frequencies, as the frequency of the input signal is lowered, the reactance $1/j\omega C$ of each of these capacitors becomes significant and this results in a decrease in the overall voltage gain of the amplifier.

In the analysis of the low-frequency response of discrete-circuit amplifiers the frequency f_L, which defines the lower end of the midband. It is usually defined as the frequency at which the gain drops by 3 dB below its value in midband. Integrated-circuit amplifiers do not utilize coupling and bypass capacitors, and thus their midband extends down to zero frequency (dc). In the analysis of the high-frequency response of discrete-circuit amplifiers the frequency f_H, which defines the upper end of the midband . This is due to internal capacitive effects in the MOSFET.. It is defined as the frequency at which the gain drops by 3 dB below its midband value. Thus, the amplifier bandwidth is defined by f_L and f_H (0 and f_H for IC amplifiers).

FREQUENCY RESPONSE OF CS AMPLIFIER:

LOW FREQUENCY RESPONSE :

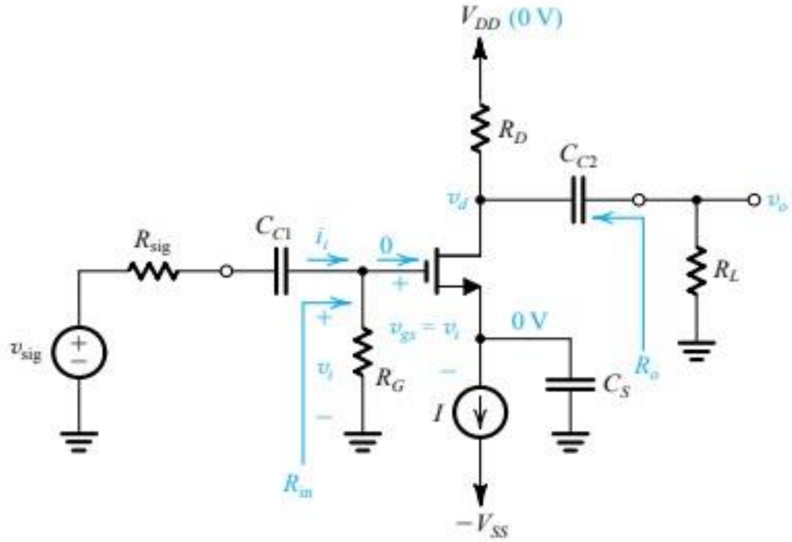


Fig.2: Common Source Amplifier

Fig.2 shows a discrete-circuit, common-source amplifier utilizing coupling capacitors and bypass capacitorC_S. We wish to determine the effect of these capacitances on the gain of the amplifier. As mentioned before, at midband frequencies, these capacitances have negligibly small impedances and can be assumed to be perfect short circuits for the purpose of calculating the midband gain. At low frequencies, however, the reactance $1/j\omega C$ of each of the three capacitances increases and the amplifier gain decreases.

HIGH FREQUENCY RESPONSE:

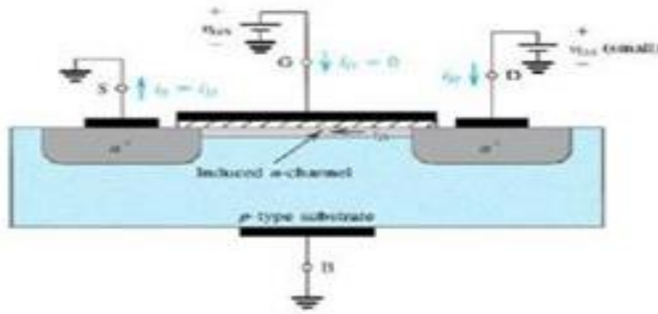
The current-voltage relationships for the MOSFET capture the behavior at low and moderate frequencies. However, similar to the diode, at high frequencies, there are a number of capacitive effects that come into play. These effects can be modeled by adding various capacitors to the MOSFET large and small signal models we have used thus far. For now, lets consider generic signals (could be large or small). First, there is some overlap between the gate and S/D. This overlap capacitance is given by

$$C_{ov} = W.L_{ov}.C_{ox}$$

With a self-aligned process, these overlap capacitances can be made very small (Lov ≈ 0.05 .. 0.1 L). The reason is that the gate itself serves as the mask when implanting the S and D regions.
In addition, there is a capacitance between the gate and the induced channel. The value of this gate capacitance is gate

$$C_{gate} = W.L.C_{ox}$$

How this gate capacitive effect manifests itself depends on the operation mode of the transistor.



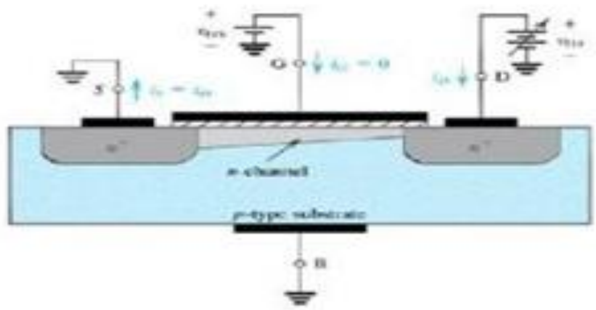


Fig .3 and Fig.4 MOSFET in triode region

For triode region:

$$C_{gs} = \frac{1}{2} . C_{gate} + C_{ov}$$

$$C_{gd} = \frac{1}{2} . C_{gate} + C_{ov}$$

For saturation region:

$$C_{gs} = \frac{2}{3} . C_{gate} + C_{ov}$$

$$C_{gd} = C_{ov}$$

(Due to tapered channel)

For cut off region:

$$C_{gs} = C_{gd} = C_{ov}$$

$$C_{gb} = C_{gate}$$

Finally, there is also the junction capacitance associated with the S-B and D-B diodes. These diodes are reverse biased. From our discussion of diodes, we know:

$$C_{sb} = C_j \; (V_{SB})$$

$$C_{sb} = C_j \; (V_{DB})$$

$$C_{gs} = \frac{2}{3} . C_{gate} + C_{ov}$$

$$C_{gd} = C_{ov}$$

$$C_{db} = \frac{C_{db-o}}{\sqrt{1 + \frac{V_{DS}}{V_O}}}$$

The equations above capture the capacitive effects for a MOSFET for a generic signal, large or small. We are mainly interested in the small signal behavior. For small signals, the capacitive effects manifest themselves as small signal capacitors that are added to the small signal model.For small signals, we will assume the MOSFET is biased in saturation. The resulting high-frequency small-signal model for the MOSFET in saturation now looks as follows:

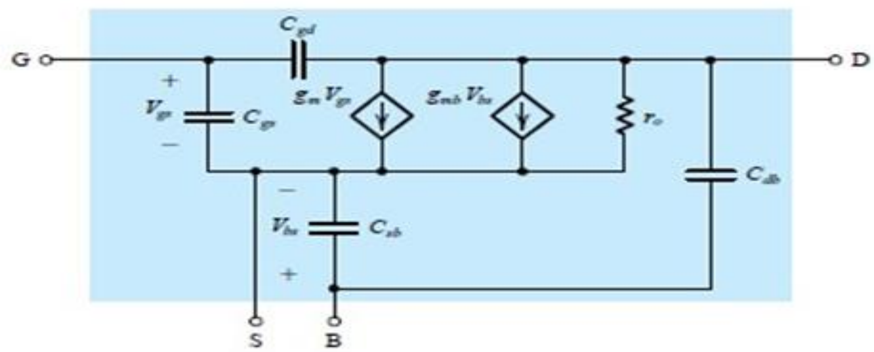


Fig.5 High-frequency, equivalent-circuit model for the MOSFET.

If S is connected to B (which is typically the case in this course), this simplifies to:

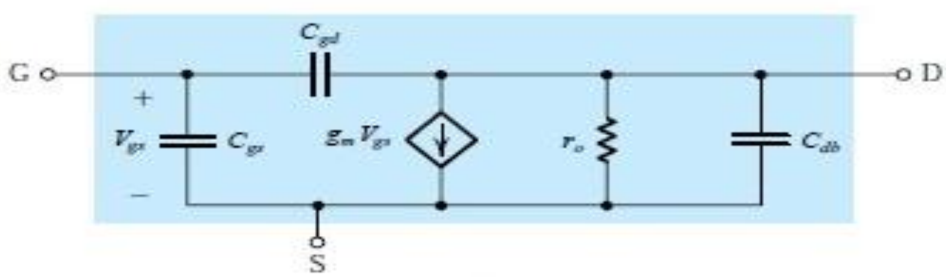


Fig. 6 The equivalent circuit for the case in which the source is connected to the substrate (body).

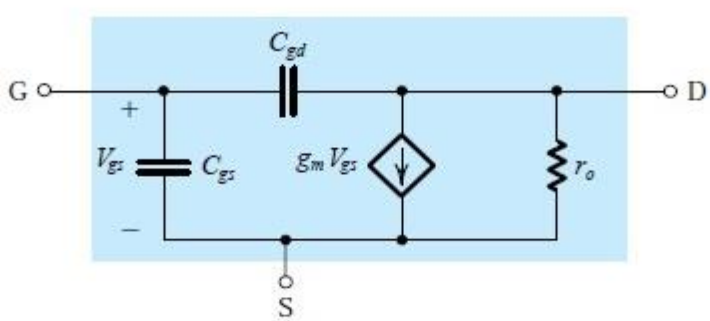


Fig.7. The equivalent-circuit model of Fig.4 with C_{db} neglected (to simplify analysis).

HIGH FREQUENCY RESPONSE FOR COMMON SOURCE AMPLIFIER:

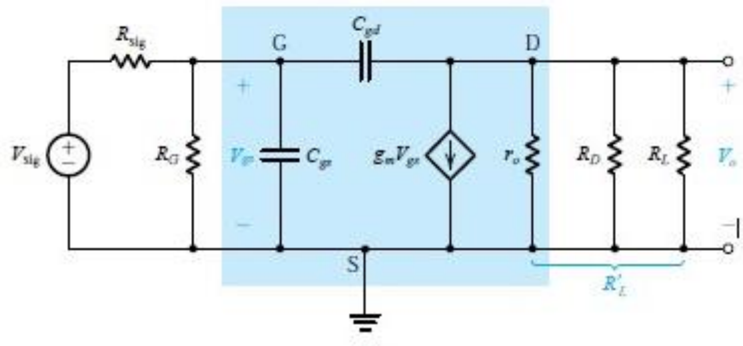


Fig 8: Equivalent circuit for high-frequency response of the CS amplifier

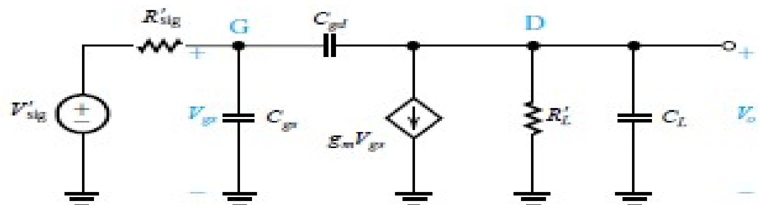


Fig 9: Generalized high-frequency equivalent circuit for the CS amplifier

ANALYSIS USING MILLER'S THEOREM

Miller's theorem allows us to replace the bridging capacitor by two capacitors:C_1 between the input node and ground and C_2 between the output node and ground as given in Fig.10 and is given by equation:

$$C_1 = C_{gd}(1 - K)$$

$$C_2 = C_{gd}(1 - \frac{1}{K})$$

Where

$$K = \frac{V_O}{V_{gs}}$$

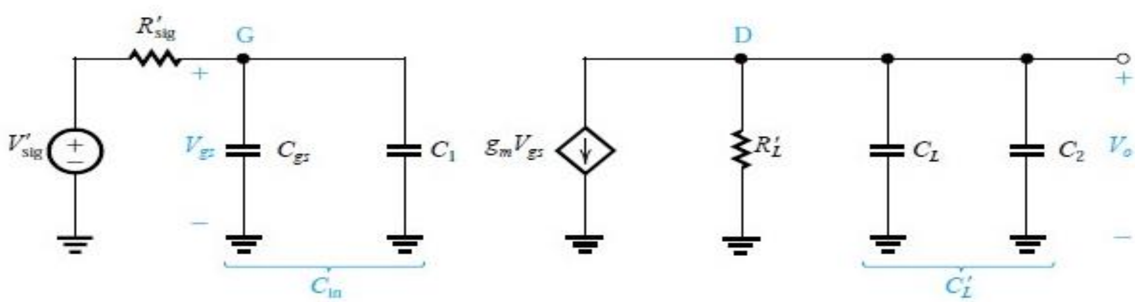


Fig. 10: The high-frequency equivalent circuit model of the CS amplifier after the application of Miller's theorem to replace the bridging capacitor C_{gd} by two capacitors C_1 and C_2. Hence the capacitance C_{gd} is effective at both input and output causing the output to decrease at high frequency.

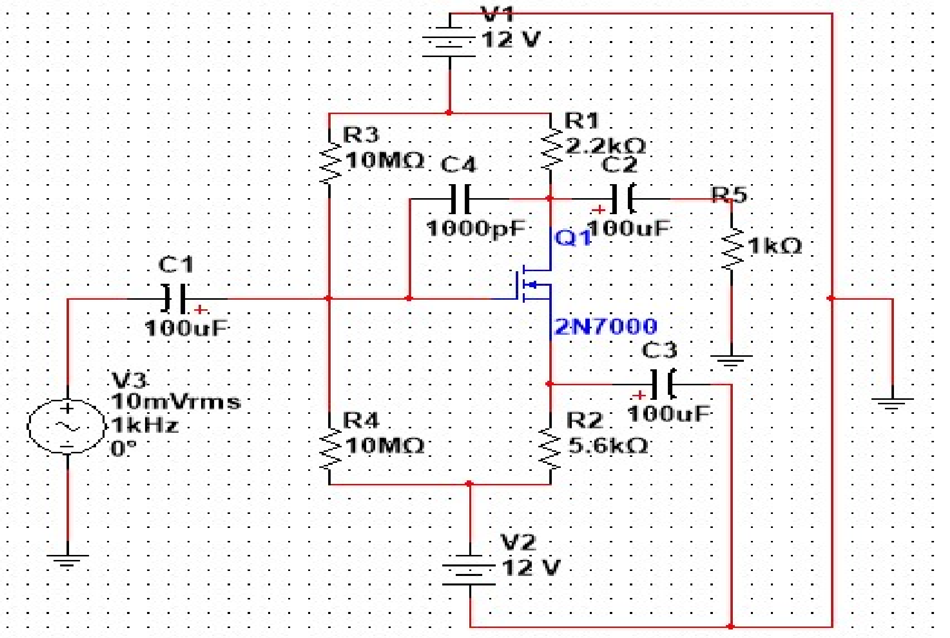
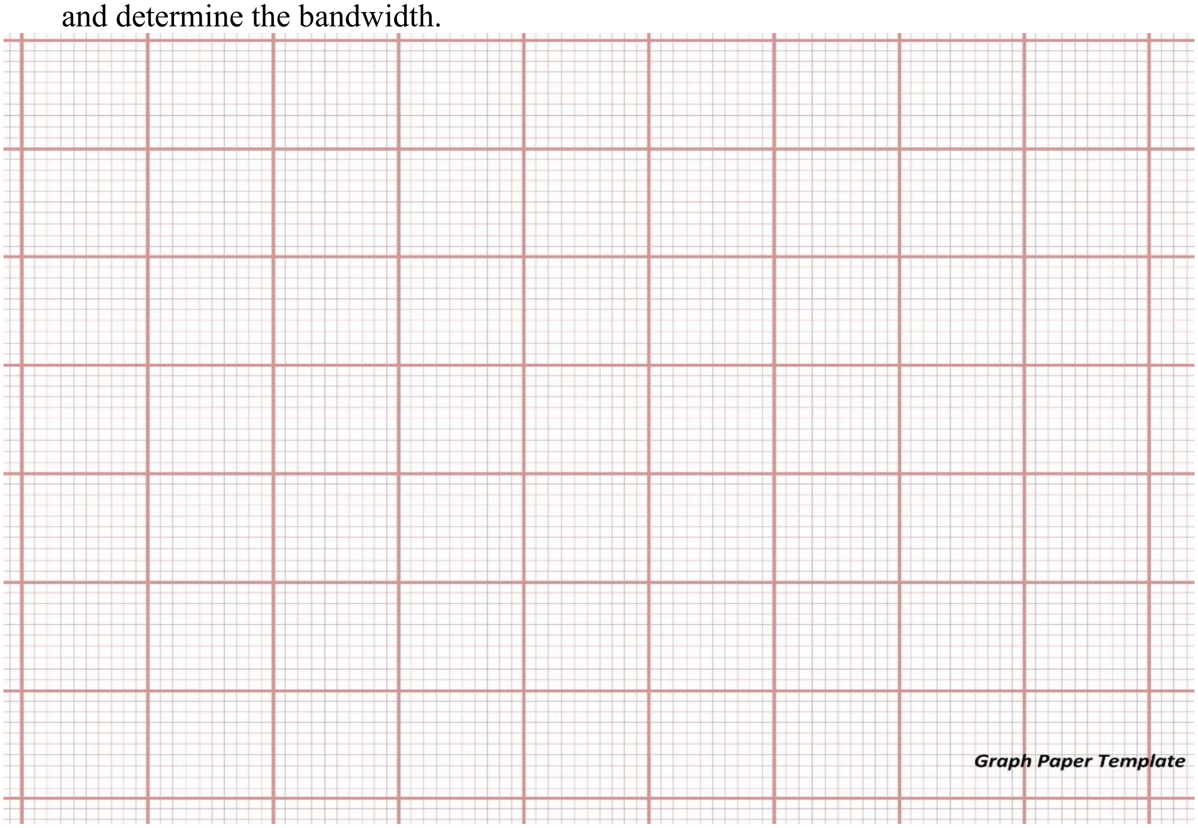


Fig 11. Common source amplifier frequency response (practical circuit)

ANALYSIS:

- Vary the frequency of the input signal from DC to 3 MHz and determine the output voltage.
- Plot the graph of output voltage Vs. frequency using semi log graph paper/computer software and determine the bandwidth.



OBSERVATIONS:

FREQUENCY RESPONSE:

Frequency	v_{out} (Measured)	Gain

CALCULATION:

RESULT:

The Bandwidth of common source amplifier as determined from the graph is -----------------------

F/OBEM 01/05/00

NED University of Engineering & Technology
Department of Electronic Engineering
Course Code and Title: EL-201 Electronic Devices and Circuits

Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	Extent of Achievement				
	0	1	2	3	4
Equipment Identification Sensory skill to ***identify*** equipment and/or its component for a lab work.	Not able to identify the equipment.	--	--	--	Able to identify equipment as well as its components.
Equipment Use Sensory skills to ***demonstrate*** the use of the equipment for the lab work.	Doesn't demonstrate the use of equipment.	Slightly demonstrates the use of equipment.	Somewhat demonstrates the use of equipment.	Moderately demon strates the use of equipment.	Fully demonstrates the use of equipment.
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Observation's Use ***Displays*** skills to use the observations from lab work for experimental verifications and illustrations.	Not able to use the observations from lab work for experimental verifications and illustrations.	Slightly able to use the observations from lab work for experimental verifications and illustrations.	Somewhat able to use the observations from lab work for experimental verifications and illustrations.	Moderately able to use the observations from lab work for experimental verifications and illustrations.	Fully able to use the observations from lab work for experimental verifications and illustrations.
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Equipment Handling ***Equipment care*** during the use.	Doesn't handle equipment with required care.	Rarely handles equipment with required care.	Occasionally handles equipment with required care.	Often handles equipment with required care.	Handles equipment with required care.
Group Work ***Contributes*** in a group based lab work.	Doesn't participate and contribute.	Slightly participates and contributes.	Somewhat participates and contributes.	Moderately participates and contributes.	Fully participates and contributes.

Laboratory Session No. Date: ____________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 10

OBJECTIVE:
To IMITATE Common Gate Amplifier circuit and its frequency response

EQUIPMENT REQUIRED:
- Protoboard
- Function Generator
- Digital Multimeter
- Power Supply
- Resistors
- Transistors: 1 x 2N7000
- Capacitors

THEORY:
As shown in figure 1 the common gate amplifier has a grounded gate terminal, a signal input at the source terminal and the output taken at the drain.

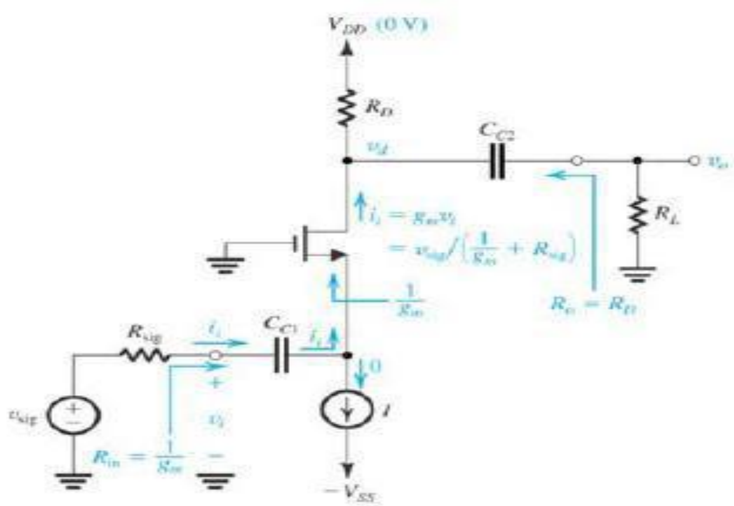


Fig 1: Common Gate Amplifier

Hence Common Gate amplifiers have

- Non-Inverting output
- Moderate input resistance
- Moderately large small signal voltage gain but smaller than common source amplifier.
- Small signal current gain less than one
- Potentially large output resistance (Dependent on R_D)

FREQUENCY RESPONSE OF CG AMPLIFIERS.

LOW FREQUENCY RESPONSE:

Fig.1 shows a discrete-circuit, common-gate amplifier utilizing coupling capacitors and bypass capacitor C_S. We wish to determine the effect of these capacitances on the gain of the amplifier. As mentioned before, at midband frequencies, these capacitances have negligibly small impedances and can be assumed to be perfect short circuits for the purpose of calculating the midband gain. At low frequencies, however, the reactance $1/j\omega C$ of each of the three capacitances increases and the amplifier gain decreases.

HIGH FREQUENCY RESPONSE:

Figure 2 shows the CG amplifier with the MOSFET internal capacitances and indicated. For generality, a capacitance is included at the output node to represent the combination of the output capacitance of a current-source load and the input capacitance of a succeeding amplifier stage. Capacitance also includes the MOSFET capacitance.

Note the appears in effect in parallel with ; therefore, in the following discussion we will lump the two capacitances together.

It is important to note at the outset that each of the three capacitances in the circuit of Fig. 9.26(a) has a grounded node. Therefore none of the capacitances undergoes the Miller multiplication effect observed in the CS stage. It follows that the CG circuit can be designed to have a much wider bandwidth than that of the CS circuit, especially when the resistance of the signal generator is large.

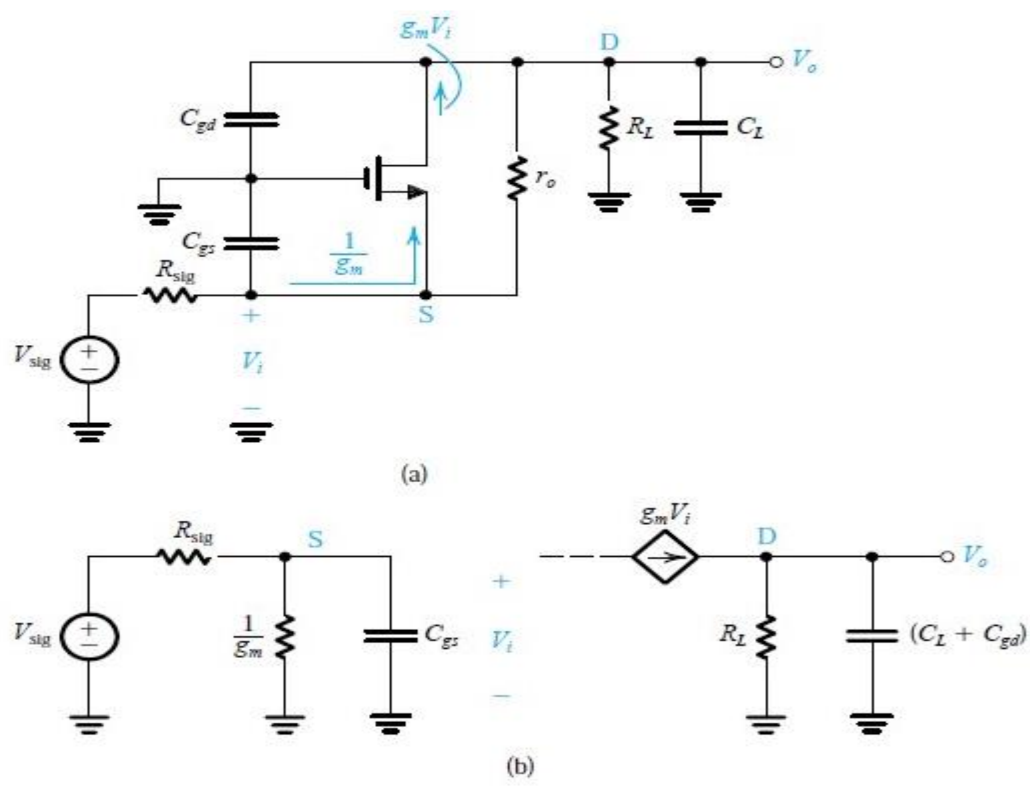


Fig.2 (a) The common-gate amplifier with the transistor internal capacitances shown. A load capacitance C_L is also included. (b) Equivalent circuit for the case in which r_o is neglected.

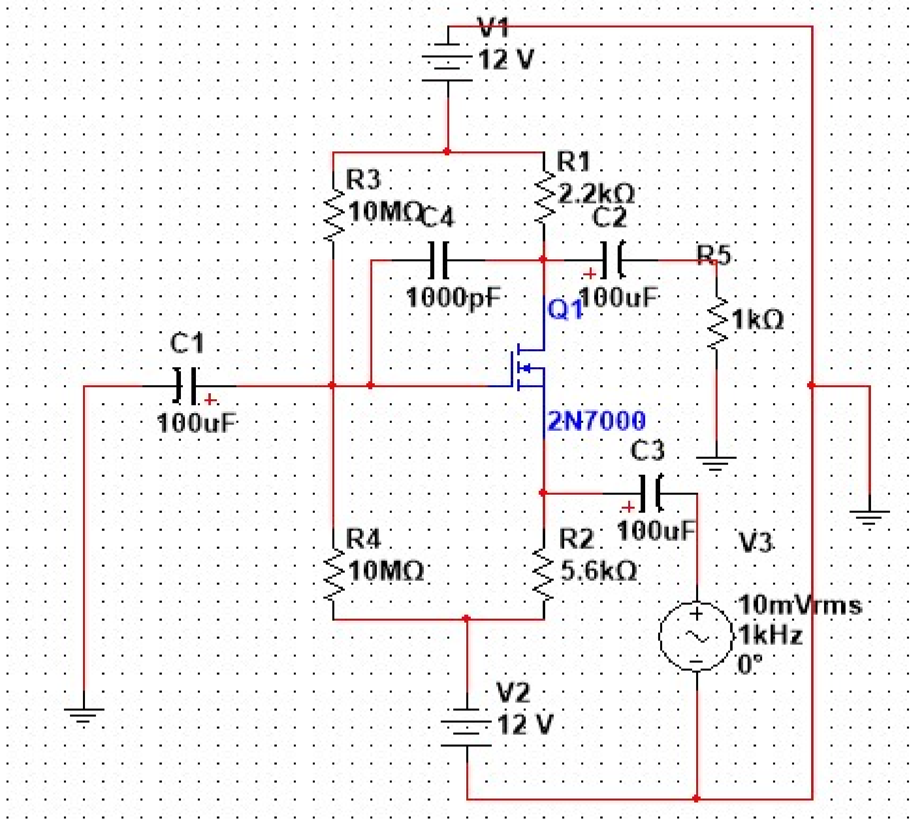


Fig. 3: common gate amplifier (practical circuit)

LAB TASK:

Implement the circuit of fig.3 on bread board. You are required to analyze a common gate amplifier. Determine the gate, drain and source voltage. Justify that the circuit can be used as an amplifier and determine the gain of the circuit.

OBSERVATION 1:

DC PARAMETERS:

	Measured	Calculated
V_G (V)		
V_S (V)		
V_D (V)		

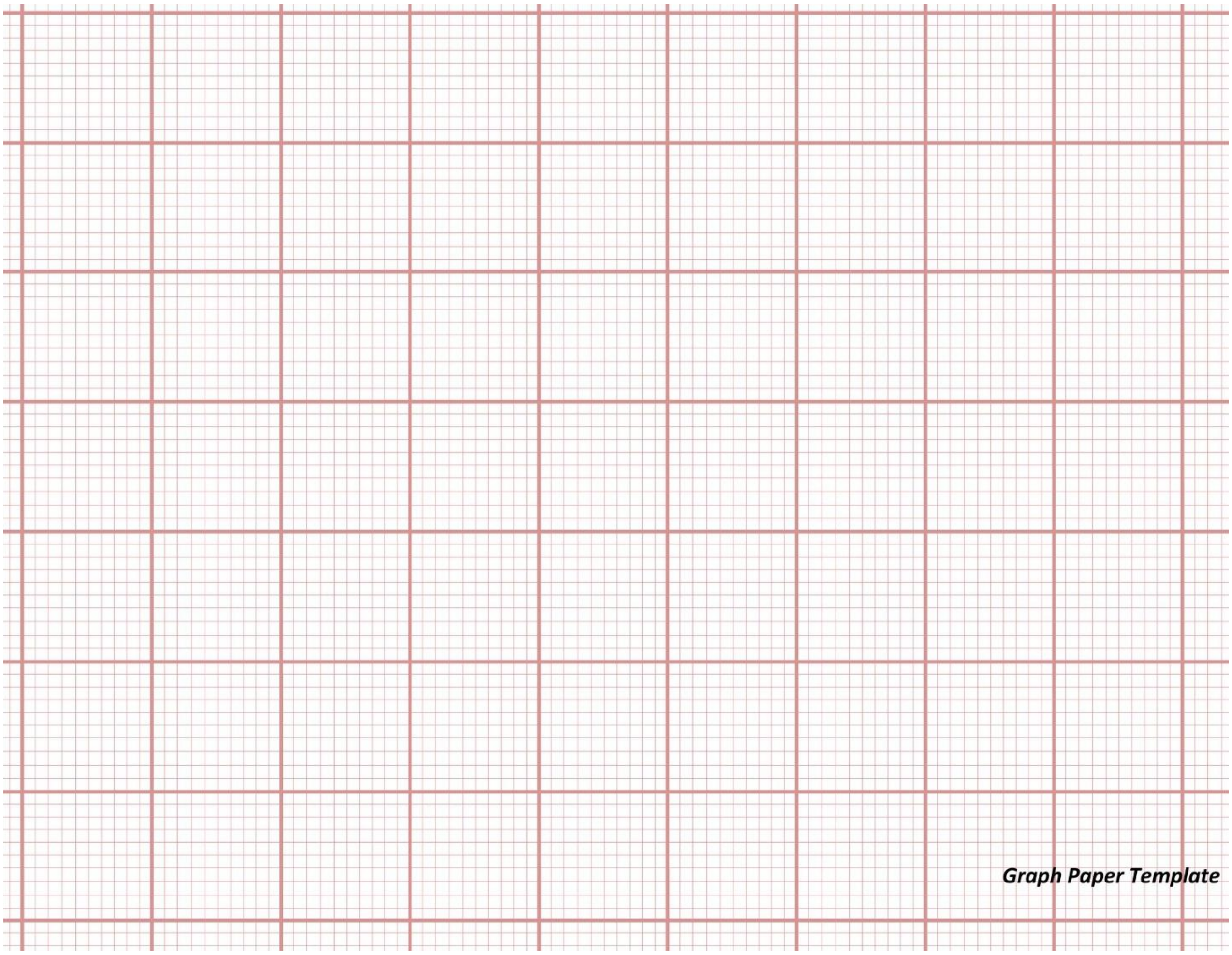
ANALYSIS:

- Vary the frequency of the input signal from DC to 3 MHz and determine the output voltage.
- Plot the graph of output voltage Vs. frequency using semi log graph paper/computer software and determine the bandwidth.

OBSERVATION 2:

FREQUENCY RESPONSE:

Frequency	v_{out} (Measured)	Gain



CALCULATIONS:

High cut off frequency =
Low cut off frequency =
Bandwidth =

RESULTS:

Phase Shift between input and output signal ___________________

The gain of Common Gate Amplifier is found to be: _______________________

The Bandwidth of common gate amplifier as determined from the graph is _____________

F/OBEM 01/05/00

NED University of Engineering & Technology
Department of Electronic Engineering
Course Code and Title: EL-201 Electronic Devices and Circuits

Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	Extent of Achievement				
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Laboratory Session No. Date: ______________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 11

OBJECTIVE:

To OPERATE UNDER SUPERVISION op-amp based Wien-Bridge oscillator

EQUIPMENT REQUIRED:

- Proto board
- Function Generator
- Digital Multi meter
- Power Supply
- Resistors
- Capacitors 2x1nF
- 741op-amp (8-pin mini DIP)

THEORY:

THE OSCILLATOR

Oscillators are electronic circuits that generate an output signal without the necessity of an input signal. It produces a periodic waveform on its output with only the DC supply voltage as an input. The output voltage can be either sinusoidal or non-sinusoidal, depending on the type of oscillator. Different types of oscillators produce various types of outputs including sine waves, square waves, triangular waves, and saw-tooth waves. A basic oscillator is shown in Figure 1.

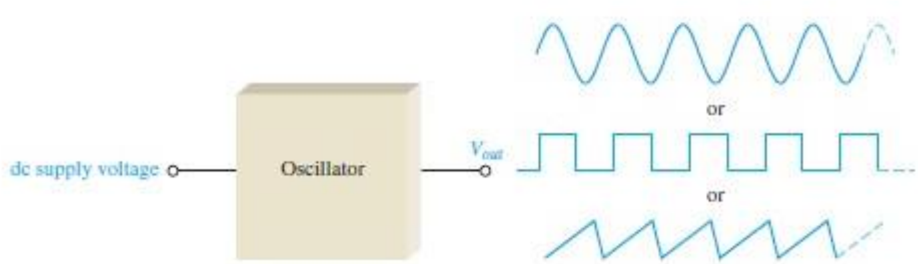


Fig1. The basic oscillator concept showing three common types of output waveforms:sine wave, square wave, and sawtooth.

TYPES OF OSCILLATOR:

Oscillators can be of 2 types.

1) Feedback Oscillators
2) Relaxation oscillators

FEEDBACK OSCILLATORS:

One type of oscillator is the feedback oscillator, which returns a fraction of the output signal to the input with no net phase shift, resulting in a reinforcement of the output signal. After oscillations are started, the loop gain is maintained at 1.0 to maintain oscillations.

A feedback oscillator consists of an amplifier for gain (either a discrete transistor or an op-amp) and a positive feedback circuit that produces phase shift and provides attenuation, as shown in Figure 2.

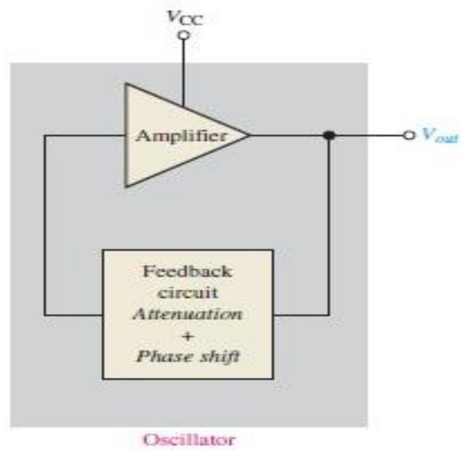


Fig.2 :Basic elements of a feedback oscillator.

RELAXATION OSCILLATORS:

A second type of oscillator is the relaxation oscillator. Instead of feedback, a relaxation oscillator uses an RC timing circuit to generate a waveform that is generally a square wave or other non-sinusoidal waveform. Typically, a relaxation oscillator uses a Schmitt trigger or other device that changes states to alternately charge and discharge a capacitor through a resistor.

FEEDBACK OSCILLATORS:

Feedback oscillator operation is based on the principle of positive feedback. Feedback oscillators are widely used to generate sinusoidal waveforms.

POSITIVE FEEDBACK:

In positive feedback, a portion of the output voltage of an amplifier is fed back to the input with no net phase shift, resulting in a strengthening of the output signal. This basic idea is illustrated in Figure 3(a).

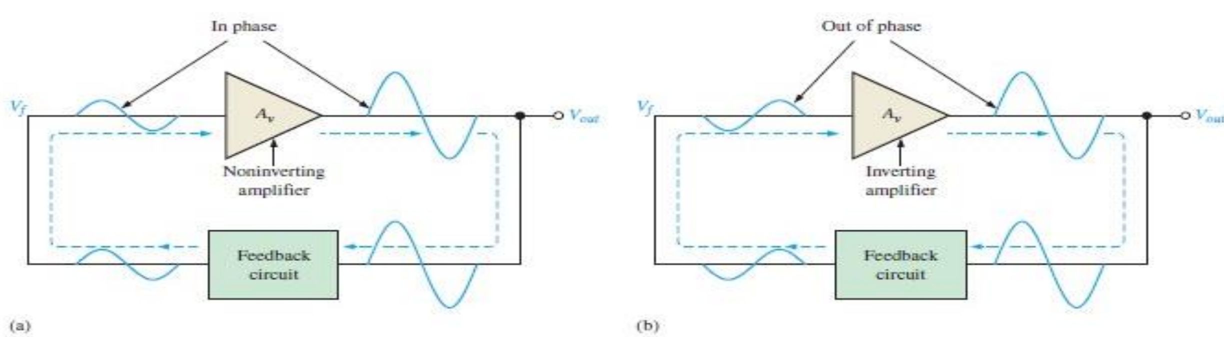


Fig.3 Positive feedback produces oscillation.

The in-phase feedback voltage is amplified to produce the output voltage, which in turn produces the feedback voltage. That is, a loop is created in which the signal maintains itself and a continuous sinusoidal output is produced. This phenomenon is called oscillation.

In some types of amplifiers, the feedback circuit shifts the phase and an inverting amplifier is required to provide another phase shift so that there is no net phase shift. This is illustrated in Figure 3(b).

CONDITIONS FOR OSCILLATION:

Two conditions, illustrated in Figure 4, are required for a sustained state of oscillation:

1. The phase shift around the feedback loop must be zero 0^o
2. The voltage gain, A_{cl}, around the closed feedback loop (loop gain) must equal 1 (unity).

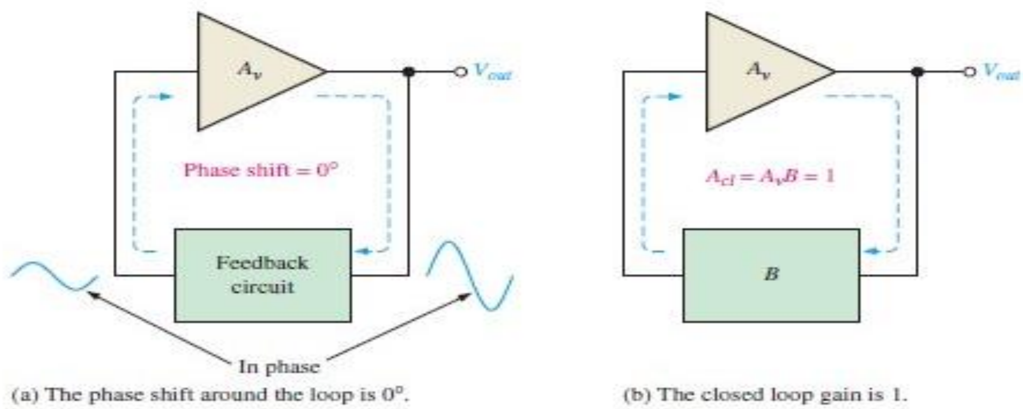


Fig.4 : General conditions to sustain oscillation.

The voltage gain around the closed feedback loop, A_{cl}, is the product of the amplifier gain, A_v, and the attenuation B, of the feedback circuit.

$$A_{cl} = A_V \times B$$

If a sinusoidal wave is the desired output, a loop gain greater than 1 will rapidly cause the output to saturate at both peaks of the waveform, producing unacceptable distortion. To avoid this, some form of gain control must be used to keep the loop gain at exactly 1 once oscillations have started.

For example, if the attenuation of the feedback circuit is 0.01, the amplifier must have a gain of exactly 100 to overcome this attenuation and not create unacceptable distortion (100 x0.01=1).

An amplifier gain of greater than 100 will cause the oscillator to limit both peaks of the waveform.

START-UP CONDITIONS:

The unity-gain condition must be met for oscillation to be maintained.For oscillation to begin, the voltage gain around the positive feedback loop must be greater than 1 so that the amplitude of the output can build up to a desired level. The gain must then decrease to 1 so that the output stays at the desired level and oscillation is sustained. The voltage gain conditions for both starting and sustaining oscillation are illustrated in Figure 5.

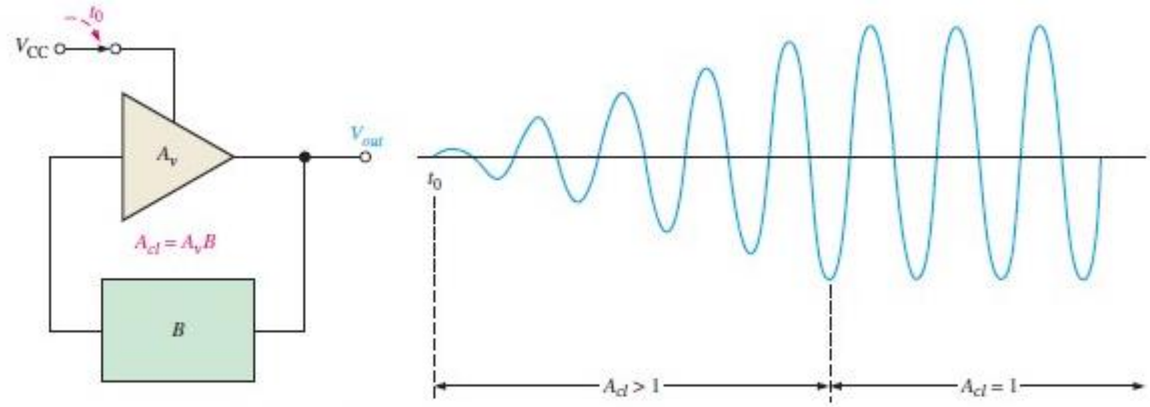


Fig.5 : When oscillation starts at t_o, the condition $A_{cl} > 1$ causes the sinusoidal output voltage amplitude to build up to a desired level. Then A_{cl} decreases to 1 and maintains the desired amplitude.

OSCILLATION WITH *RC* FEEDBACK CIRCUITS:

Three types of feedback oscillators that use RC circuits to produce sinusoidal outputs are the

- Wien-bridge oscillator
- Phase-shift oscillator
- Twin-T oscillator

Generally, RC feedback oscillators are used for frequencies up to about 1 MHz.

The Wien-bridge is by far the most widely used type of RC feedback oscillator for this range of frequencies.

WIEN-BRIDGE OSCILLATOR

One type of sinusoidal feedback oscillator is the Wien-bridge oscillator. A fundamental part of the Wien-bridge oscillator is a lead-lag circuit like that shown in Figure 6(a). R_1 and C_1 together form the lag portion of the circuit; R_2 and C_2 form the lead portion.

The operation of this lead-lag circuit is as follows.

- At lower frequencies, the lead circuit takes over due to the high reactance of C_2.
- As the frequency increases, X_{C2} decreases, thus allowing the output voltage to increase.
- At some specified frequency, the response of the lag circuit takes over, and the decreasing value of X_{C1}causes the output voltage to decrease,

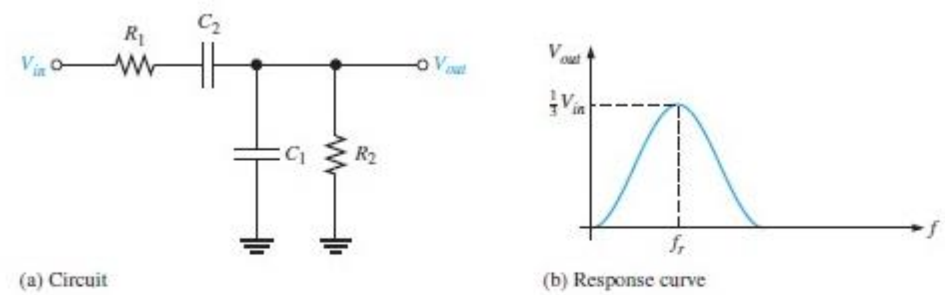


Fig.6 : A lead-lag circuit and its response curve.

The response curve for the lead-lag circuit shown in Figure 6(b) indicates that the output voltage peaks at a frequency called the resonant frequency, f_r. At this point, the attenuation (V_{out}/V_{in}) of the circuit is 1/3 if $R_1 = R_2$ and $X_{C1} = X_{C2}$ as stated by the following equation

$$\frac{V_{out}}{V_{in}} = \frac{1}{3}$$

The formula for the resonant frequency is

$$f_r \frac{1}{2\pi RC}$$

To summarize, the lead-lag circuit in the Wien-bridge oscillator has a resonant frequency, at which the phase shift through the circuit is 0^O and the attenuation is 1/3.

Below, f_r the lead circuit dominates and the output leads the input. Above, f_r the lag circuit dominates and the output lags the input.

THE BASIC CIRCUIT:

The lead-lag circuit is used in the positive feedback loop of an op-amp, as shown in Figure 7(a).

A voltage divider is used in the negative feedback loop. The Wien-bridge oscillator circuit can be viewed as a non-inverting amplifier configuration with the input signal fed back from the output through the lead-lag circuit. Recall that the voltage divider determines the closed-loop gain of the amplifier.

$$A_{cl} = \frac{1}{B} = \frac{1}{{R_2}/{R_1} + R_2}$$

The circuit is redrawn in Figure 7(b) to show that the op-amp is connected across the bridge circuit. One leg of the bridge is the lead-lag circuit, and the other is the voltage divider.

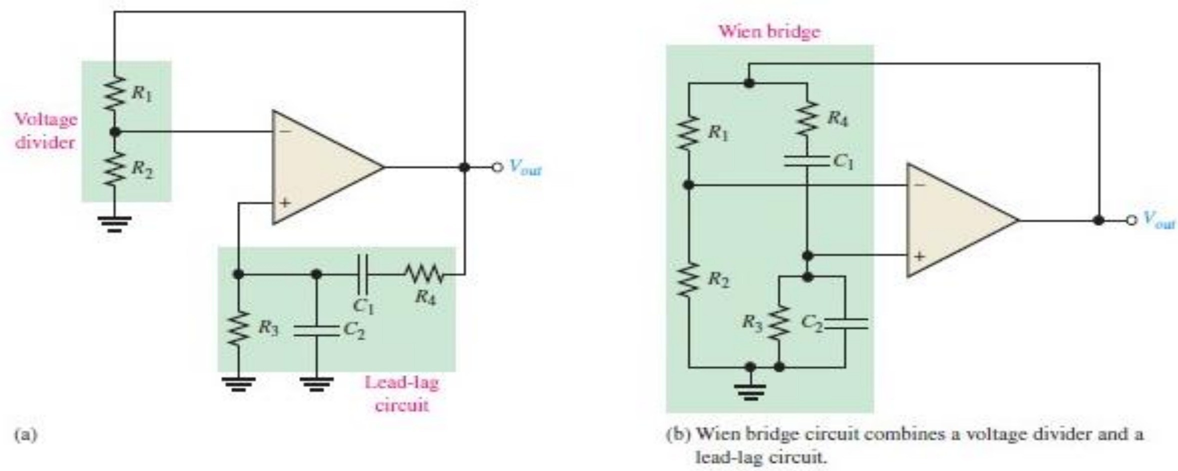


Fig.7 :The Wien-bridge oscillator schematic drawn in two different but equivalent ways.

POSITIVE FEEDBACK CONDITIONS FOR OSCILLATION:

As you know, for the circuit output to oscillate, the phase shift around the positive feedback loop must be 0° and the gain around the loop must equal unity (1). The 0° phase-shift condition is met when the frequency is f_r because the phase shift through the lead-lag circuit is 0° and there is no inversion from the non-inverting input of the op-amp to the output. This is shown in Figure 8(a).

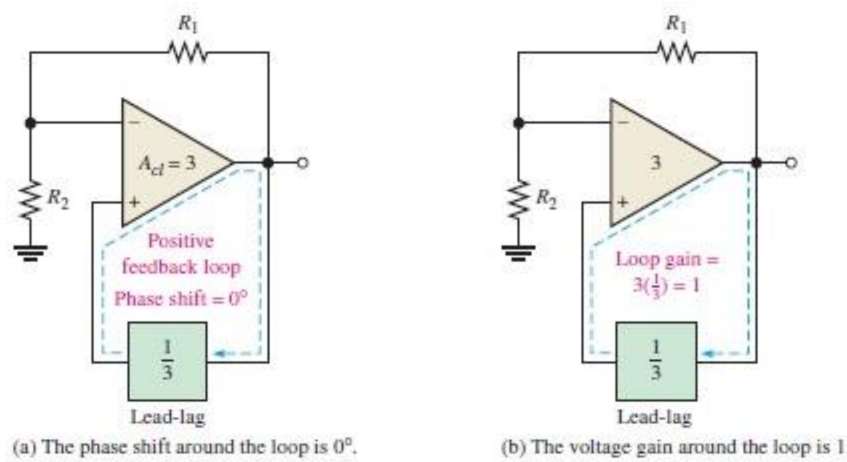


Fig.8 :Conditions for sustained oscillation.

The unity-gain condition in the feedback loop is met when

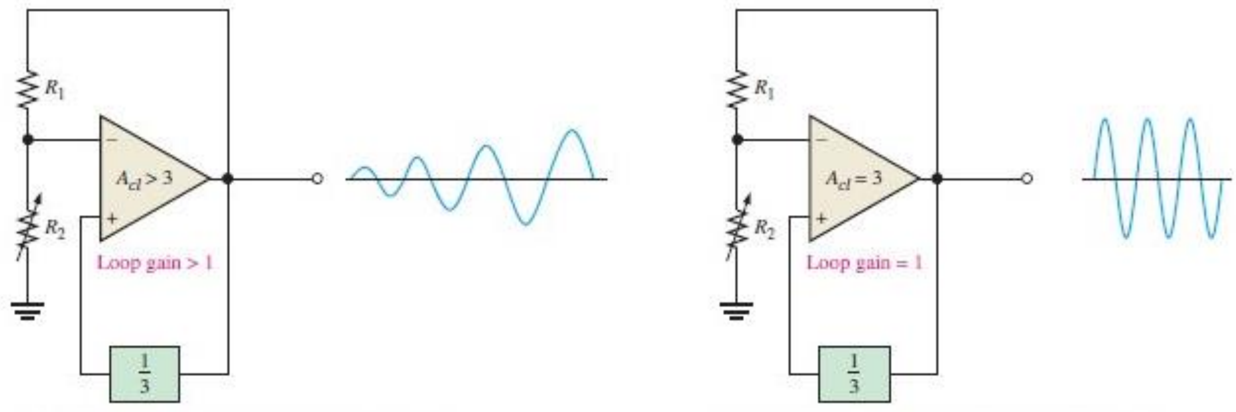
$$A_{cl}=3$$

This offsets the 1/3 attenuation of the lead-lag circuit, thus making the total gain around the positive feedback loop equal to 1, as shown in Figure 8(b). - To achieve a closed-loop gain of 3

$$R_1 = 2R_2$$

START-UP CONDITIONS

Initially, the closed-loop gain of the amplifier itself must be more than 3 ($A_{cl} > 3$) until the output signal builds up to a desired level. Ideally, the gain of the amplifier must then decrease to 3 so that the total gain around the loop is 1 and the output signal stays at the desired level, thus sustaining oscillation. This is illustrated in Figure 9.



(a) Loop gain greater than 1 causes output to build up. (b) Loop gain of 1 causes a sustained constant output.

Fig.9: Conditions for start-up and sustained oscillations.

Initially, a small positive feedback signal develops from noise. The lead-lag circuit permits only a signal with a frequency equal to appear in phase on the non-inverting input. This feedback signal is amplified and continually strengthened, resulting in a buildup of the output voltage. When the output signal reaches the zener breakdown voltage, the zeners conduct and effectively short out. This lowers the amplifier's closed-loop gain to 3. At this point, the total loop gain is 1 and the output signal levels off and the oscillation is sustained.

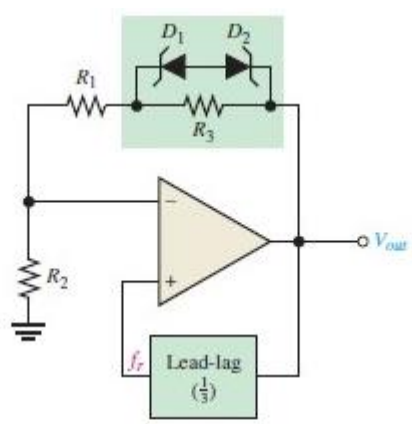


Fig. 10: Self-starting Wien-bridge oscillator using back-to-back zener diodes.

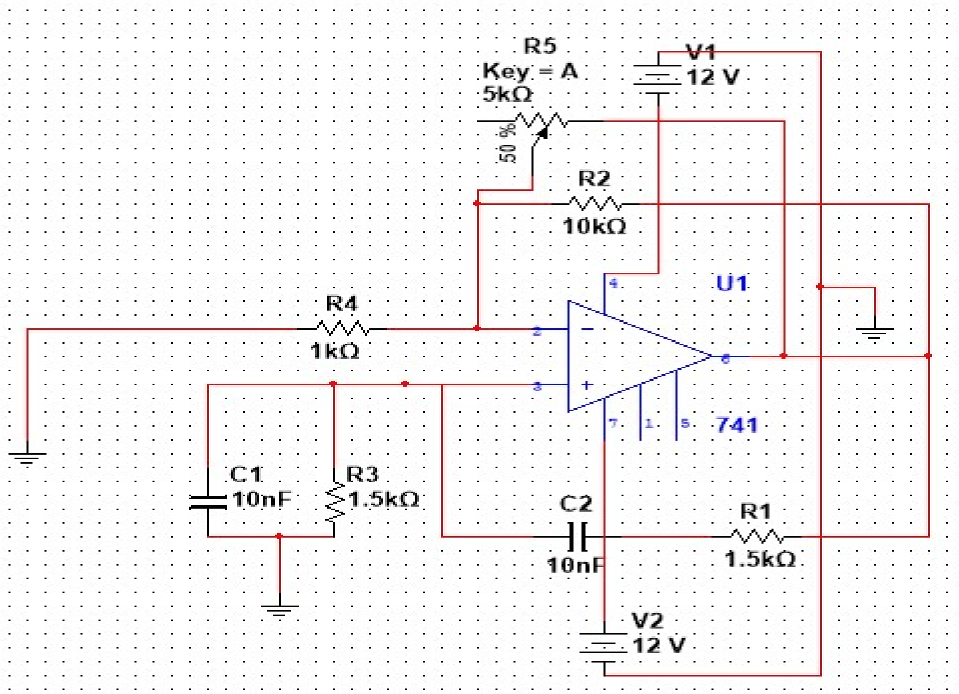


Fig. 11: Wien Bridge Oscillator (Practical circuit)

PROCEDURE:

1. Wire the circuit
2. Apply $\pm$ 12V supply connections to the bread board.
3. Turn 100kΩ potentiometer completely clock-wise
4. Connect one probe of the oscilloscope to the output of the circuit and the second probe to the positive pin of op-amp.
5. Adjust the potentiometer to obtain a sine wave across the output.
6. Calculate the theoretical value of the frequency at which the circuit should oscillate as given by the formula.
7. Measure the oscillation frequency with an oscilloscope.

USEFUL FORMULA:

$R_2 = 2R_4$ (as per simulation schematic fig 11)

$R_1 = 2R_2$ (as per shown in figure 8)

(in figure 11 its R2 in parallel with potentiometer)

$$f_r = \frac{1}{2\pi RC}$$

OBSERVATION:

Parameter	Theoretically calculated	Experimentally Measured
R1 (parallel combination of R2 and pot)		
f_r		

CALCULATIONS:

$f_R = 1 / 2\pi RC$

RESULTS:

The resonant frequency as measured comes out to be: ……………….

The resonant frequency as calculated comes out to be: ……………….

R_1 as measured comes out to be: …………………

R_1 as calculated comes out to be: …………………

F/OBEM 01/05/00

NED University of Engineering & Technology
Department of Electronic Engineering
Course Code and Title: EL-201 Electronic Devices and Circuit

Psychomotor Domain Assessment Rubric-Level P3					
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Laboratory Session No.10 Date: ______________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 12

OBJECTIVE:
To IMITATE op-amp based Phase-Shift oscillator

EQUIPMENT REQUIRED:
- Proto board
- Function Generator
- Digital Multi meter
- Power Supply
- Resistors
- 5kΩ potentiometer
- Capacitors 3x0.1uF
- 741op-amp (8-pin mini DIP)

THEORY:
THE PHASE-SHIFT OSCILLATOR:
Figure1 shows a sinusoidal feedback oscillator called the phase-shift oscillator.

Each of the three RC circuits in the feedback loop can provide a maximum phase shift approaching 60°.

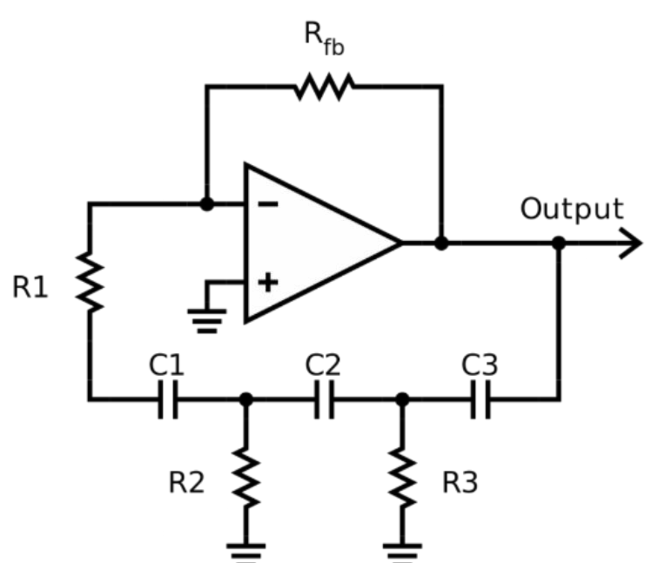

Fig. 1:Phase Shift Oscillator

Oscillation occurs at the frequency where the total phase shift through the three RC circuits is 180°. The inversion of the op-amp itself provides the additional 180° to meet the requirement for oscillation of a 360° (or 0°) phase shift around the feedback loop. The attenuation, , of the three-section RC feedback circuit is

$$B = \frac{1}{29}$$

$$B = R_1/R_{fb}$$

To meet the greater-than-unity loop gain requirement, the closed-loop voltage gain of the op-amp must be greater than 29 (set by $R_3$and R_f). The frequency of oscillation f_r is given as

$$f_r = \frac{1}{2\pi\sqrt{6}\ RC}$$

$$R_1 = R_2 = R_3 = R \quad \text{and } C_1 = C_2 = C_3 = C$$

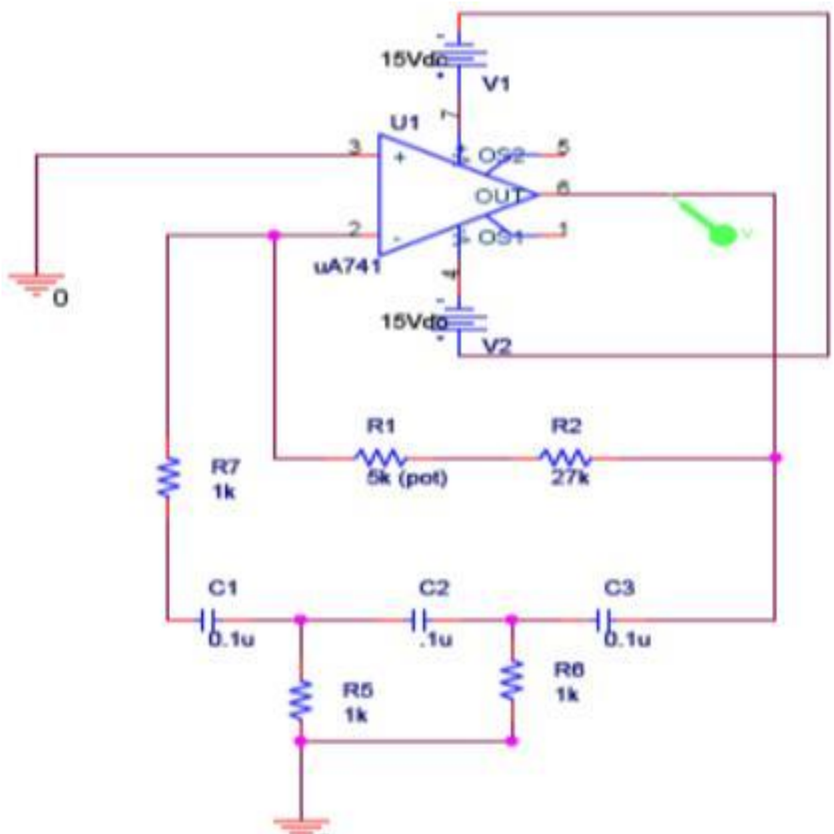

Fig. 2: Phase shift oscillator (practical circuit)

PROCEDURE:

1. Build the circuit in Fig.2
2. Apply ± 15V supply connections to the bread board.
3. Depending on the setting of the 5 kΩ potentiometer the circuit may or may not be oscillating when power is applied. If a sine wave is not displayed on the oscilloscope, carefully adjust the 5 kΩ potentiometer until a sine wave starts to appear on the oscilloscope's display.
4. On the other hand, if a sine wave is seen when power is applied on the bread board, carefully decrease the resistance of the potentiometer to obtain the best looking sine wave.
5. Measure the output frequency of the phase shift oscillator recording your result in table. Compare this value with the expected frequency found using equation.
6. Measure the value of the feedback resistance that produced maximum oscillation.

USEFUL FORMULA:

Output Frequency

$$f_r = \frac{1}{2\pi\sqrt{6}\ RC}$$

For oscillation

$$\frac{R_f}{R} = 29$$

OBSERVATION:

Parameter	Theoretically calculated	Experimentally Measured
Output Frequency, f_o		
R_f		

CALCULATIONS:

$$f_r = \frac{1}{2\pi\sqrt{6}\ RC}$$

RESULTS:

The output frequency as measured comes out to be: ____________

The output frequency as calculated comes out to be: _____________

R_f as measured comes out to be :_______________

R_f as calculated comes out to be :_______________

F/OBEM 01/05/00

NED University of Engineering & Technology
Department of Electronic Engineering
Course Code and Title: EL-201 Electronic Devices and Circuits

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Laboratory Session No. Date: ______________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

OPEN ENDED LAB

OBJECTIVE:

To IMITATE a cascode amplifier circuit

BACKGROUND:

Generally it is desired to have a circuit having good gain and bandwidth. A Common Source amplifier has high input resistance, a very good voltage gain, however it does not have a good frequency response . On the other hand a common gate amplifier has a good frequency response but has low input resistance which makes it unsuitable to be used as the first stage of any amplifier circuit. In order to get the benefit of having a high gain along with a good bandwidth a combination of common source and common gate amplifier is used when common source is placed at the input side to achieve high input resistance and good voltage gain and common gate is placed at the output side to achieve good bandwidth . Such a circuit is called cascode amplifier circuit

TASK:

- Maximize the gain bandwidth product of cascode amplifier circuit
- Perform its simulation
- Implement it on Vero board
- Show all necessary calculations

F/OBEM 01/05/00

NED University of Engineering & Technology
Department of Electronic Engineering
Course Code and Title: EL-239 and Analog Integrated Circuit

Psychomotor Domain Assessment Rubric-Level P3					
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Laboratory Session No. Open Ended Lab Date: ______________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	