

# **Department of Electronic Engineering**

# **NED University of Engineering & Technology**

# **PRACTICAL WORK BOOK**

For the course

# DIGITAL ELECTRONICS (EL-238) For S.E(AP)

Instructor name:		•
Student Name:		•
Roll no:	Batch:	•
Semester:	Year:	•
<b>Department:</b>		•

# LABORATORY WORK BOOK FOR THE COURSE

# EL-238 DIGITAL ELECTRONICS

Prepared by

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**Revised by** 

Saba Fakhar

Approved By

The Board of Studies of Department of Electronic Engineering

# Laboratory Manual

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	b) NMOS AND, OR gates with resistive load		
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	timer		
13.	Open ended Lab: To design a four input Multiplexer		
	using logic gates		

# Lab Session :01

## **Objective:**

Implement the following digital logic circuits:

- a. NMOS Inverter circuit with resistive load
- b. NMOS AND, OR gates with resistive load

### **Apparatus:**

- MOSFET transistors 2N7000
- Connecting Wires
- Digital Multimeter
- Protoboard

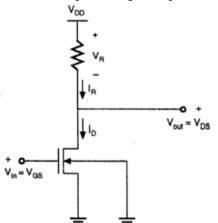
## **Theory:**

#### **Resistive Load Inverter**

The basic structure of a resistive load inverter is shown in the figure given below. Here, enhancement type nMOS acts as the driver transistor. The load consists of a simple linear resistor  $R_L$ . The power supply of the circuit is  $V_{DD}$ .

#### **Circuit Operation**

When the input of the driver transistor is less than threshold voltage  $V_{TH}$  ( $V_{in} < V_{TH}$ ), driver transistor is in the cut – off region and does not conduct any current. So, the voltage drop across the load resistor is ZERO and output voltage is equal to the  $V_{DD}$ .



#### Fig:01

#### Part a:

Connect the circuit on breadboard according to the given figure for implementing NMOS inverter.

#### **Observations:**

Vin	Vout
0V	
5V	

## Part b:

For implementing AND gate, connect two transistors in series and for OR gate, connect two transistors in parallel.

### **Observations:**

AND GATE			OR GATE		
	Vin	Vout	V	ïn	Vout
0V	0V		0V	0V	
5V	0V		5V	0V	
0V	5V		0V	5V	
5V	5V		5V	5V	

**Results:** 



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## NED University of Engineering & Technology Department of Electronic Engineering Course Code and Title: EL-238 Digital Electronics

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01.11.0		Η	Extent of Achievem	ent		
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## Lab Session.2

## **Objective:**

To analyze the operation and characteristics of the analog switch.

### Apparatus:

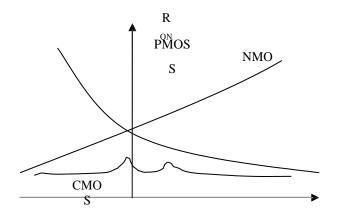
- Base unit for the IPES system
- Experiment module G33/EV
- Digital multimeter
- Function generator
- Oscilloscope

## Theory

#### **CMOS Switches**

MOSFETs are easily integrated into driver circuits on a single chip, and are therefore suitable for use as analog signal switches. The main disadvantage in switches featuring PMOS and NMOS transistors is there sensitivity to ON resistance at the analog signal voltage.

This problem can almost entirely eliminated by the use of CMOS switch consists of two parallel switches one featuring a channel-p MOSFET, the other with a channel-n MOSFET this parallel combination gives a relatively flat ON resistance/ analog signal voltage curve .



Analog Signal (V)

Fig:01

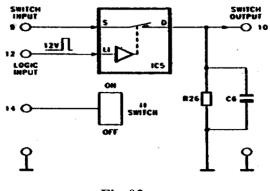
#### **DESCRIPTION OF THE MODULE**

#### ANALOG SWITCH

The section of the circuit denominated" ANALOG SWITCH" consists of the integrated analog switch ICs (DG 200 CJ).

The data sheet shows that this is a two-channel single-pole single-throw (SPST) analog switch which employs CMOS technology to ensure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in both directions with no offset voltage in the ON condition and block voltages up to 30 Vp-p in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With logic "0" at the input to the driver, the switch will be ON; logic "1" will turn the switch OFF. A voltage of between 0 and 0.8V is required for logic "0", while logic "1" is given by a voltage of between 2.4 and 15V. The input can therefore be directly interfaced with TTL, DTL, RTL and CMOS circuits.

The switch action is break-before-make, in order to prevent any shorting in the input signal. For the sake of convenience in the execution of the exercises, and as the switch is bidirectional, the two terminals of the analog switch are indicated on the trainer panel as SWITCH IN and SWITCH OUT. The driver logic input may be manual (ON/OFF operation via special switch) or external. This is selected by fitting a jumper between jack 12 and jack 14.





#### **Procedure:**

#### Measuring rDS (ON) without current

The purpose of this exercise is to measure the drain-source resistance present in the analog switch without current.

- Connect the ±12V and ground jacks on the panel to a corrected power supply. Connect jack 12 to jack 14.
- Connect the digital multimeter (set to measure ohms) between jacks 9 and 10.
- Set switch I<sub>1</sub> to ON; read the value of r<sub>DS</sub> (ON) indicated on the digital multimeter.

#### Measuring rDS (ON) with current

The purpose of this exercise is to measure the drain-source resistance present in the analog switch in the ON state as the current increases.

- Connect the ±12V and ground jacks on the panel to a corrected power supply. Connect jacks 12 and 14.
- Connect a variable 0 => + 12V DC power supply between jack 9 and ground. Set switch I<sub>1</sub> to ON.
- Increase the input voltage gradually until voltage can be measured at the terminals of R<sub>26</sub>, as shown in column 1 of table. For each R<sub>26</sub> voltage, measure the voltage between jacks 9 and 10 and list these voltages in column
- Care should be taken to avoid exceeding 12V, as this might damage the unit. Given  $R_{26}$  equivalent to  $1.2K\Omega$ .
- Calculate the current circulating between drain and source.
- From V<sub>DS</sub> and I<sub>DS</sub>, calculate the value of R<sub>DS</sub> and list in column 4.

## **Results:**

S.N.	V <sub>R26</sub> (volts)	V <sub>DS (mV)</sub>	I <sub>DS(mA)</sub>	$R_{DS(\Omega)}$
1				
2				
3				
4				
5				
6				



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## Lab Session:03

## **Objective:**

To analyze the switching time of the analog switch.

### <u>Apparatus:</u>

- Base unit for the IPES system
- Experiment module G33/EV
- Digital multimeter
- Function generator
- Oscilloscope

## **DESCRIPTION OF THE MODULE**

#### ANALOG SWITCH

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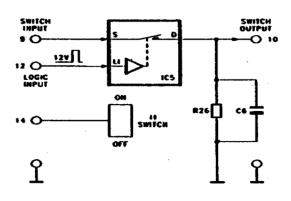
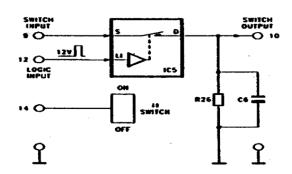


Fig:01

## **Theory**

One of the main specifications regarding the application of analog switches is the TURN ON TIME and the TURN OFF TIME. When a switch is commanded to change from ON to OFF, and vice-versa, a propagation delay occurs in the circuit driver. The TON and TOFF times may be used to determine when a switch begins operation and whether multiple switches connected in a multiplexer configuration will be "make- before-break" or "break-before-make", i.e. whether the switches are triggered and then pause, or whether the pause precedes their action. The propagation delay should not be confused with the settling time, which is also effected by the load impedance. Two transitions will therefore apply:

> OFF to ON  $t_{settling} = t_{ON} + t_l \uparrow$  where  $t_l \uparrow = f(R_{ON}, R_{LOAD}, C_D, C_{LOAD})$ ON to OFF  $t_{settling} = t_{OFF} + t_l \downarrow$  where  $t_l \downarrow = f(R_{LOAD}, C_{LOAD}, C_D)$

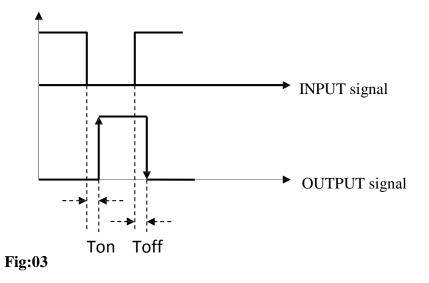


#### Fig:02

#### Measurement of the switching time

The purpose of this exercise is to determine the time required by the analog switch to open and close. **Procedure** 

- Connect the ±12V and ground jacks on the panel to a corrected power supply. Connect a + 10V DC power supply between jack 9 and ground.
- Send a rectangular signal from the function generator between jack 12 and ground (amplitude 5V positive, frequency 10 KHz).
- Connect one of the probes of the oscilloscope to the generator signal and the other to the output signal present between jack 10 and ground.
- Measure the switching times between the output signal and the control signal; i.e. the rise time which corresponds to the closing of the analog switch and the fall time which corresponds to its opening.



## Result:

The t<sub>ON</sub> (Turn ON time) of the analog switch comes out to be: \_\_\_\_\_\_ The t<sub>OFF</sub> (Turn OFF time) of the analog switch comes out to be: \_\_\_\_\_\_



### NED University of Engineering & Technology Department of Electronic Engineering Course Code and Title: EL-238 Digital Electronics

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## Lab Session 04

## **Objective:**

To analyze the operation and characteristics of the sample and hold circuit

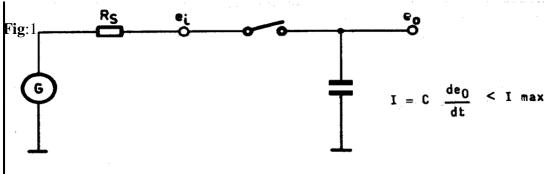
## **Apparatus:**

Base unit for the IPES system Experiment module G33/EV Function generator Oscilloscope

## **Theory:**

The most simple sample and hold circuit consists of a switch and a capacitance. Two important specifications may be easily illustrated using the basic circuit. These are the aperture time and the acquisition time. The aperture time is the delay (reaction time) between the moment in which the control logic instructs the switch to open and the moment in which the aperture actually occurs. When extremely long aperture times (in the order of milliseconds) are tolerated, a relay may be used for the switch. For aperture times of less than 100  $\mu$ s, FETs or BJTs are used as switches.

In variable-time systems, the input signal to the sample and hold circuit changes; the sample and hold circuit holds the last signal measured. The acquisition time is the time required by the sample and hold circuit to acquire the input signal value (within a predetermined degree of accuracy) when the control logic passes from hold to sample. Clearly, the most onerous condition is that in which the output must alter over its entire range (e.g. from + 10V to -10V and vice-versa).



#### **Module Description**

Sample and hold device featuring operational amplifiers and analog switches

This circuit represents a non-inverting sample and hold with four operational amplifiers and four analog switches.

Operational amplifiers IC8 and IC10, together with analog switches IC9a and IC9c, make up the classic sample and hold circuit.

As the two analog switches must operate in opposing modes:

HOLD phase:	IC9a = closed	IC9c = open
SAMPLE phase:	IC9a = open	IC9c = close

And as there is only one command, switch IC9b is used to carry out an inversion.

Capacitor C9 is the HOLD capacitor, and is also referred to as the "data storage capacitor".

Input amplifier IC8, configured as non-inverting, has a high input resistance and features a potentiometer for calibration of the offset voltage.

Operational IC10 is of the FET type, and therefore has a very high input resistance (being connected in a non-inve rting configuration). This means that the di scharge of capacitor C9 in the HOLD phase is minimal.

The circuit consisting of IC9d and IC11 is added in order to minimize the errors introduced by analog switch IC9c and operational amplifier IC10. The errors introduced by these two parts of the circuit are identical (also considering that R42 corresponds approximately to the output resistance of operational amplifier IC8) and are therefore cancelled when applied to the two differential inputs of a mplifier IC12 It is i mportant that capacitors IC9 and IC10 are almost identical.

By connecting jack 17 to jack 19, the SAMPL E/HOLD status may be controlled via the SAMPLE/HOLD switch. If jack 17 is conn ected to jack 18, the SAMP LFJHOLD status is controlled by the signal from the GENERATOR

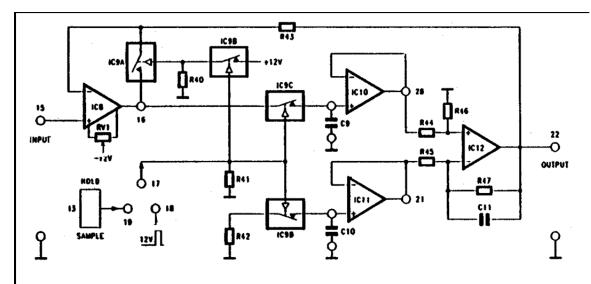


Fig 2

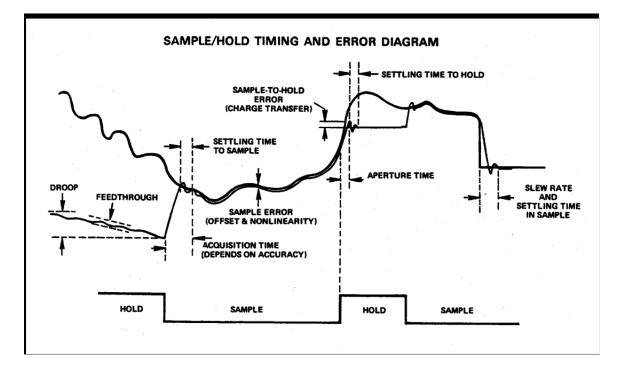


Fig. 3

#### **Procedure:**

The purpose of this exercise is to measure the time required for transformation of the input signal into an output signal (starting from the beginning of the sampling phase).

- Connect the ±12V and ground jacks of the panel to a corrected power supply. Connect jack 17 to jack 18.
- Connect jack 7 to jack 5. Set switch I2 to 10 KHz.
- Adjust the duty-cycle of the potentiometer so that the sample time is 60 µsec and the hold time 10 µsec (turn the knob completely counterclockwise).
- Connect jack 3 to jack 15.
- Connect one of the probes of the oscilloscope to the output signal between jack 22 and ground. The second probe should be connected first to the sample and hold signal and then to the input signal. Fig. 4 shows the behavior in time of the three signals.

Note the existence of a delay (acquisition time) is approximately 10 to 15µsec between the "start sampling" command signal and the settling of the output signal

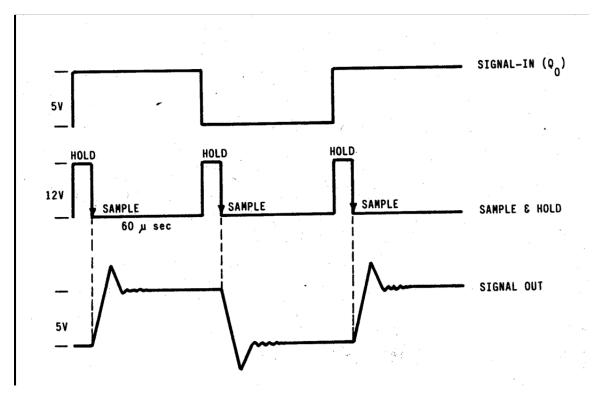


Fig 4

- Vary the duty cycle of controlling signal (connected to jack 17), and take observations.
- Connect the jack 15 and ground to function generator (sine wave of 5V positive with 5 KHz).
- Vary the duty cycle of controlling signal (connected to jack 17).
- Observe the acquisition times for different duty cycles of sample and hold signal. Repeat the procedure with triangular wave input

#### **Result:**

The time required for transformation of the square wave input signal into an output signal comes out to be as follows:

- 1. Aperture Time =
- 2. Acquisition Time



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## Lab Session :05

## **Objective:**

To analyze the operation of Digital-to-Analog and Analog-to-Digital Convertor.

### **Apparatus:**

- Base unit for the IPES system
- Experiment module F03A
- Digital multimeter
- Function generator
- Oscilloscope

## **Theory**

An analog-to-digital (A/D) conversion means quantizing the amplitude of a physical quantity (e.g. a voltage) into a discrete levels class. Thus obtaining a series of digits, forming a number of a proper code. Generally the binary code and, consequently, binary numbers are used. Analog data can be obtained again through digital-to-analog (D/A) conversion.

Due to the quantization, each value V of the analog signal included within the interval  $V_i$  to  $V_{i+1}$  is always quantized at the same level  $N_i$ .

The interval:  $V_{i+1}$  to  $V_1 = Q$ , is defined as "quantum level".

Another important parameter of A/D converters is the conversion time since it defines the capacity of the converter to operate the conversion of a variable signal; in fact, remember that the sequence of the quantized levels must allow the regeneration of the original analog signal.

A time-variable signal can be converted into a discrete values class carrying out the sampling and holding operations. The sampling and holding operations are carried out through proper circuits called "Sample and Hold".

#### Resolution

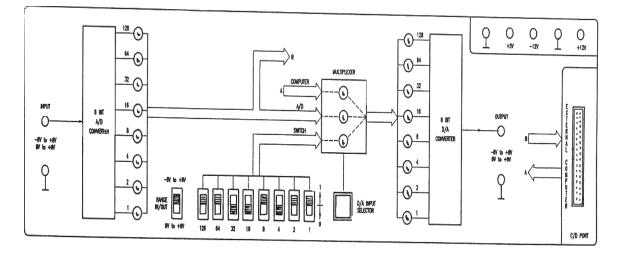
It defines the smallest standard incremental change in. the output voltage of a DAC or the amount of input voltage change required to increment the output of an ADC between a code change and the

next adjacent code change. A converter with "n" switches can divide the input in  $2^n$  parts: the least

significant increment is then 2<sup>-n</sup>, or one least significant bit (LSB). On the contrary the Most Significant Bit carries a weight of 2. Resolution is applied to DACs and ADCs and may be expressed in percent of full scale or in binary bits.

#### **DESCRIPTION OF THE MODULE F03A**

This module carries out an educational system of analog-to-digital and digital-to-analog conversion. This system consists of two 8-bit converters of large diffusion. A signal adapter is inserted before the A/D converter. This device permits the conversion of signals coming from conditioners with output range not coinciding with the converter output. The input range is chosen by acting on the IN/OUT selector and can be from 0 to +8V with the selector down and from -8 to +8V with the selector up. The input of the digital-to-analog converter can come from the analog-to-digital converter, from the computer or from a series of switches installed on the panel. The input connection is chosen through the pushbutton (D/A INPUT SELECTOR) and displayed on the LEDS of the multiplexer. The equipment must be power supplied with regulated D.C. voltages of +12,-12Vand +5V.



#### A/D converter

The A/D converter (ADCO804LCN) operates with an input range included from 0V to +5 V, that is, an input voltage of 0 V generates a digital output signal consisting of a sequence of all 0s, whereas an input voltage of +5volts generates a digital signal of all 1s. Therefore the input signal must be adapted so that the minimum value of its range can generate an output signal of all 0 and the maximum value of the range generates a digital signal of all 1.

#### **D/A Converter**

The digital signal (8 bits) which must be sent to the input of the D/A converter (DACO800) can come from the A/D converter, from the computer or from a set of the 8 switches. The operational amplifier IC1A has a gain of 0.5 and carries out a shift range of the input signal if the range -8 to +8 is selected, the operational amplifier IC1B makes the extreme range values coincide with 0v and 5v.

#### **Range:**

The range of module can be selected through Range IN/OUT switch. The range can be 0v to +8v, i.e.

	OV = 00000000 +8V = 11111111
Or -8v to +8v, i.e.	-8V = 00000000
Procedure:	+8V = 111111111

Set switch Range IN/OUT to 0V to 8'

## Resolution measurement:

- Connect  $\pm 12V$ ,  $\pm 5V$ .
- Select SWITCH option through D/A input selector.
- Set the switches (S128 to S1) to any position and note the analog voltage output through multimeter.
- Change the position of switch S1 (LSB), and note the analog voltage output through multimeter.
- The change in voltages is equal to one resolution.

Binary codes for different voltage levels:

- Connect the  $\pm 12V$ ,  $\pm 5V$  and ground jacks of the panel to a corrected power supply.
- Selec t A/D option through D/A input selector.
- Apply different voltage values to the analog input. Read the corresponding binary values on LEDs.
- Note the analog output values of the D/A converter corresponding to the different digital values and compare with the analog input value.

## **Observation:**

Input	Binary Code(0 V to	Output
Voltage	+8 V)	voltage
Input	Binary Code(-8 V to	Output
Voltage	+8 V)	voltage

## **Result:**

The resolution of the ADC and DAC, for the switch Range IN/OUT position 0 V to 8 V, is\_\_\_\_\_ The resolution of the ADC and DAC, for the switch Range IN/OUT position -8 V to +8 V, is\_\_\_\_\_



## NED University of Engineering & Technology Department of Electronic Engineering Course Code and Title: EL-238 Digital Electronics

	Psychomoto	r Domain Assessn	nent Rubric-Level	P3		
01.111.0	Extent of Achievement					
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<b>Equipment Identification</b> Sensory skill to <i>identify</i> equipment and/or its component for a lab work.	Not able to identify the equipment.				Able to identify equipment as well as its components.	
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Laboratory Session No.

Date: \_\_\_\_\_

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

# Lab Session: 06

## **Objective:** Implementation of Full Adder

### **Apparatus:**

- Base unit for the IPES system
- Experiment module E18/EV
- Digital multimeter
- Function generator
- Oscilloscope
- Bread Board
- 7408 (AND)
- 7432 (OR)
- 7486 (XOR)
- 7486 (XOR)

## **Theory:**

#### **DESCRIPTION OF THE MODULE**

The educational module E18 consists in a printed circuit on which digital logic circuits (TTL and CMOS) are mounted performing the following functions:

No. of circuits	Name of circuit	IC
-6	Inverters	74LS04
-4	2- input AND ports	74LS08
-4	2- input NAND ports	74LSOO
-4	2- input OR ports	74LS32
-4	2- input NOR ports	74LS02
-4	2-input EX-OR ports	74LS86
-2	TTL-CMOS and CMOS-TTL interfaces	MM74C906
-4	J-K Flip-Flops	74LS76
-1	4-bit full Adder	74LS83
-1	4-bit Shift-register	74LS95
-1	Synchronous BCD counter	74LS160

-1	BCD decoder and display driver	74LS247
-1	7-segment display	HDSP5301
-1	Sync up/down counter	74LS192
-1	9-bit parity generator	74LS280
-1	Monostable	74LS221
-1	Multiplexer	74LS153
-1	Demultiplexer	74LS155
-1	BCD to decimal decoder	74LS42
-1	Encoder	74LS147
-1	Three state buffer	74LS125
-1	Latch	74LS75
-1	4-bit comparator	74LS85
-1	4-bit preselector	PICO-D-137-AK-1
-1	Clock generator (1 Hz, 10 kHz)	74LS14
-2	Push- buttons	4/6417
-8	Switches	4/7201
-10	LEDs	TIL210
-4	NAND ports with two CMOS inputs	CD4011
-2	20-pin terminals	

The components are mounted to carry out the experiments more quickly especially more complex circuits.

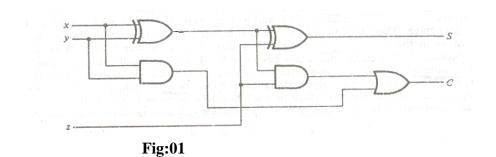
The connections between terminals of the devices are carried out by means of electrical cables and proper tubes present on the module and, electrically connected to the terminals of the integrated circuits. Each integrated circuit shows the silk screen printed logical diagram. The functions related to the IC are shown and terminals (In-Out) are indicated. Implementation of full-adder circuit is done using module E18/EV.

#### Full- Adder

A full-adder is a combinational circuit that forms the arithmetic sum of three input bits. It Consists of three inputs and two outputs. Two of the input variables, denoted by x and y, represent two significant bits to be added. The third input z, represents the carry from the previous lower significant position. Two outputs are necessary because the arithmetic sum of three binary digits ranges in value from 0 to3 and binary 2or 3 needs two digits. The binary variable S indicates the sum and C the carry. The binary variable S gives the value if the least significant bit of the sum. The binary variable C gives the output carry.

## **Procedure:**

- Implement the circuit of full adder on bread board or on module.
- Supply the required power (5V) to ICs AND OR and XOR
- Check the output using logic probe. And fill in the truth table.



## **Result:**

The resulting truth table of the adder circuit is as follows:

x	У	Z.	С	S
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		



## NED University of Engineering & Technology Department of Electronic Engineering Course Code and Title: EL-238 Digital Electronics

	Psychomoto	r Domain Assessn	nent Rubric-Level	P3	
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Laboratory Session				e:	l

Weighted CLO (Psychomotor Score) Remarks Instructor's Signature with Date: 28

## Lab Session :07

## **Objective:**

To implement all types of Flip-Flops

## Apparatus:

- Base unit for the IPES system
- Experiment module E18/EV

## **Theory:**

The bistable multivibrator, commonly called flip- flops, are the most common form of digital memory elements. A memory element is generally a device which can store the logic state 0 or 1, called information "bit". The memory elements enable the storing of digital information for further uses. They permit to carry out complex sequential digital circuits, which took to the construction of modern calculators.

## 1.<u>R-S Flip-flop (latch)</u>

RESET

1

a)

A main memory circuit can be carried out with the crossed coupling of two NAND ports: this kind of connection is called R-S flip- flop. Fig. 1 shows the diagram carried out with NAND ports. Similarly, to carry out the same flip- flop, it is also possible to use some NOR ports.

TRUTH TABLE OF THE R-S FLIP FLOP	S O	R	Q X	Q` X			
X=Last state	0	1	0	1			
?= indefinite state	1	0	1	0			
	1	1	?	?			
SET 1 P	*	<b>}</b> ⁰ ]		_	S	R-S	



Q

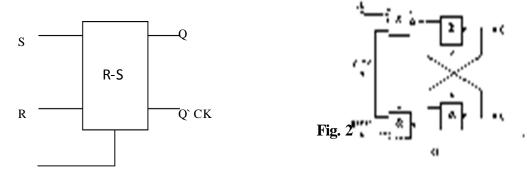
Q`

Suppose a data is to be inserted in the flip-flop; the input levels are: SET = 1 and RESET = 0. The output level of the port 1 is low (0) and this determines a high state across the output of port 3 (Q = 1). The output of port 2 is instead at 1, so port 4 finds two high levels (port 2 and 3) across its inputs, and takes its output to a low level (Q = 0).

The flip-flop is now on SET, with memorized information. Now, applying a high level across the RESET terminal, keeping the SET to a low level (s = 0 and R = 1), the flip- flop switches, i.e. it changes state, and the output becomes Q = 0 and Q = 1. In this case we say that the flip-flop is in RESET state. If the inputs SET and RESET are simultaneously applied to a high logic level (S = R = 1), you obtain an indeterminate state: Q=Q<sup>\*</sup>=1. When the still state (R=S=O) is reset, the output having the lower transition time is taken high.

#### **R-S Flip-flop with Clock**

In sequential systems, the change of state in the flip-flops is often required to occur in synchronism with the clock pulse. This is carried out by modifying the diagram of fig.5.1 into the one of fig.5.2.

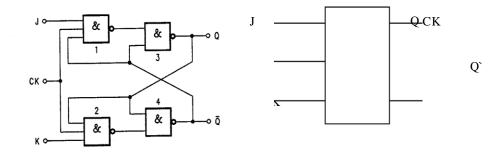


#### Fig:02

While no input pulse is applied, the flip-flop keeps as it is, independently from the value of Rand S. Applying a clock pulse, if the inputs are R=S=O, the flip-flop keeps stable with the last output (Qn+1 = Qn). If instead we have: R = 0 and S = 1 the output of port 1 goes to 0 enabling the switching. In correspondence to a new clock pulse, if: R=1 and S=O, the latch changes state again and its outputs are: Q=O and Q=1. In the case in which: R=S=1 on arrival of the clock pulse, the outputs of the flip-flops should both go to 1.

#### 2.J-K flip-flop

The J-K flip-flop is formed by the R-S with clock, in which the outputs are taken back to the input, as in fig.



#### Fig:03

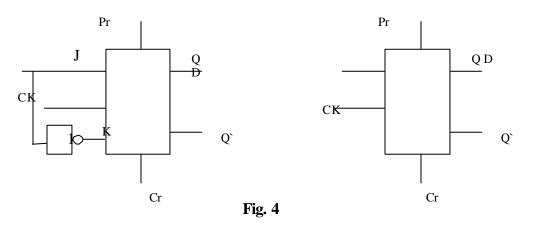
Suppose that the flip-flop is in the state: Q = 0; Q' = 1. If the data input J is at the level 1 in correspondence to the clock pulse, the output of port 1 gets to 0, and the memory cell composed by ports 3-4 changes state: Q = 1 and Q' = 0

This flip-flop enables the removal of the uncertainty there was in the flip-flops R-S with

clock, when the inputs were both at level 1. In fact, if: Q=1 Q'=O J=K=1 on arrival of the clock pulse, only port 2 enables the passage of the input data, while port 1 blocks them. The level 0 obtained across the output of port 2 makes the memory element switch (port 3 and 4). So, we have seen that when the inputs are both high there is no uncertainty, but the output state changes.

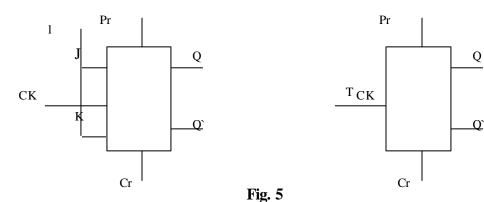
#### 3.D Flip-flop

If a J-K flip-flop is modified by adding an inverter, so that the input K is complement of J, the set is known as flip-flop type D, in which D=DATA. Its operation is simple: when a clock pulse arrives, the data present across the input is transferred and kept across the output.



#### **4.T Flip-flop**

If the inputs J and K are set always at logic level 1 on a flip-flop J-K, so this is a flip-flop commonly called type T (T means TOGGLE). It inverts the state of the outputs each time the input pulse applied to line T passes from the state 1 to the state O. Fig.5 shows the diagram (a) and the logic symbol (b) of a flip-flop type T.





- Carry out a flip-flop type R-S using NAND and NOT ports
- Connect the SET and RESET inputs to two switches.
- Connect the outputs Q and Q to two LEDs.
- Power the module.
- Turn the SET input, with the switch, to 1 and then to 0.

- Analyze the behavior of the outputs.
- Set the RESET line to 1, and then to 0.
- Analyze the behavior of the outputs again.
- Repeat sometimes the operations with the switches and check the carried out memorizations.

Now, try to set both inputs to 1 and explain what the reason of the uncertain state is.

S	R	Q	Q`
0	0		
0	1		
1	0		
1	1		

#### 2. Implementation and Analysis of a J-K Flip-flop

- Carry out the circuit of a J-K flip-flop.
- Connect the inputs J and K to two switches, and the outputs to two LEDs.
- Connect the terminal of the cbck at the bottom on the left to the input CK of the built up flip-flop, as well as to a led, to display the behavior. Power the module.
- Set the switches connected to the inputs alternatively high.
- Analyze the behavior of the LEDs.
- Now, set both switches to the logic level 1, and explain the behavior of the flip-flop.

J	Κ	Q	Q`
0	0		
0	1		
1	0		
1	1		

#### 3. Implementation of D-Flip-flop

- Carry out the circuit of a flip-flop type D by means of J-K flip-flops.
- Connect the inputs P and R to 1.
- Check the operation of the fip-flop D by means of switches 0-1 of the input D and the Clock.

D	Q

## 4. Implementation of T- Flip-flop

- Carry out the circuit of a flip-flop type T by means of J-K flip-flop
- Connect the inputs P and R to 1.
- Check the operation of the flip-flop T by means of switches 0-1 to the Clock input.

Т	Q



## NED University of Engineering & Technology Department of Electronic Engineering Course Code and Title: EL-238 Digital Electronics

	Psychomoto		nent Rubric-Level		
Skill Sets	Extent of Achievement				
	0	1	2	3	4
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Laboratory Session N	lo		Date:		
Weighted CLO (Psyc	homotor Score)				
Remarks					
Instructor's Signature	with Date:				

# Lab Session.08

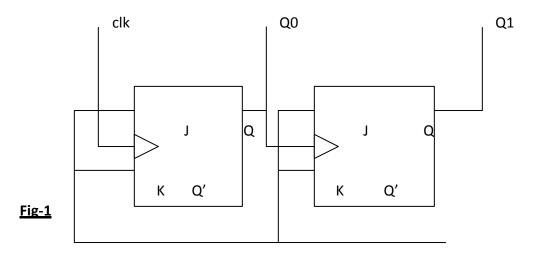
**Objective:** To implement 2-bit counter circuit

## Apparatus:

- Base unit for the IPES system
- Experiment module E18/EV

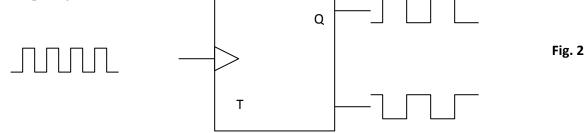
### **Theory**

Counters are digital integrated devices which can state in a well-defined sequence, applying a train pulse across the input. They are carried out with flip-flop and logic port stages, where each stage supplies an output which, together with the others, indicate the number of pulses received in binary form.



These counters are also called 'BINARY COUNTERS' and can be used apart as counters as frequency dividers, supplying the o/p with a pulse after 'n' input pulses.

If we apply a fixed frequency pulse train to a counter, rather than individual pulses coming at random intervals, we begin to notice some interesting characteristics and useful relationships between the input clock signal and the output signal.



Consider a single flip flop with a continuous succession of clock pulses at a fixed frequency, such as the one shown above. We note three useful facts about the output signals seen at Q and Q' :

- a) They are exactly inverted to each other
- b) They are perfect square waves (50% duty cycle)
- c) They have a frequency just half that of the clock pulse train

The duty cycle of any rectangular waveform refers to the percentage of the full cycle that the signal remains at logic 1. If the signal spends half its time at logic 1 and the other half at logic 0, we have a waveform with a 50% duty cycle. This describes a perfect, symmetrical square wave.

## **Procedure**:

#### 2-bit Asynchronous Counter:

- Carry out the circuit of a 2-stage asynchronous counter
- Connect all inputs, J and K to logic 1 (i.e +5V)
- Connect 1Hz clock to input CK of first flip-flop
- Connect Q0 to CK of second flip-flop
- Connect the two outputs, Q0 and Q1, to oscilloscope
- Power the module and analyze the operation of complete system

## Result:



## NED University of Engineering & Technology Department of Electronic Engineering Course Code and Title: EL-238 Digital Electronics

	Psychomoto	r Domain Assessn	nent Rubric-Level	P3	
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Laboratory Session 1	No	_	Date	2:	

Weighted CLO (Psychomotor Score)	
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Remarks	
Instructor's Signature with Date:	

# **Objective:**

To verify dynamic inverter logic using transistors

## **Apparatus**

Bread board NMOS and PMOS transistors Power supply

# **Theory:**

Dynamic logic is distinguished from so-called *static logic* in that dynamic logic uses a <u>clock signal</u> in its implementation of <u>combinational logic</u> circuits. The usual use of a clock signal is to synchronize transitions in <u>sequential logic</u> circuits.

The dynamic logic circuit requires two phases. The first phase, when *Clock* is low, is called the *setup phase* or the *precharge phase* and the second phase, when *Clock* is high, is called the *evaluation phase*. In the setup phase, the output is driven high unconditionally (no matter the values of the inputs *A* and *B*). The <u>capacitor</u>, which represents the load capacitance of this gate, becomes charged. Because the transistor at the bottom is turned off, it is impossible for the output to be driven low during this phase.

During the *evaluation phase*, *Clock* is high. If *A* and *B* are also high, the output will be pulled low. Otherwise, the output stays high (due to the load capacitance).

Dynamic logic has a few potential problems that static logic does not. For example, if the clock speed is too slow, the output will decay too quickly to be of use. Also, the output is only valid for part of each clock cycle, so the device connected to it must sample it synchronously during the time that it is valid.

Also, when both *A* and *B* are high, so that the output is low, the circuit will pump one capacitor-load of charge from Vdd to ground for each clock cycle, by first charging and then discharging the capacitor in each clock cycle. This makes the circuit (with its output connected to a high impedance) less efficient than the static version (which theoretically should not allow any current to flow except through the output), and when the *A* and *B* inputs are constant and both high, the dynamic NAND gate uses power in proportion to the <u>clock</u> rate, as long as it functions correctly

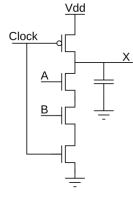


Fig:01

# **Procedure & Result:**

- a) Take frequency of clock signal in comparison to frequency of square wave input signal. Observe and describe the results.
- b) Take frequency of clock signal much smaller than frequency of square wave input signal. Observe and describe the results.

c) Take frequency of clock signal much greater than frequency of square wave input signal. Observe and describe the results.



# NED University of Engineering & Technology Department of Electronic Engineering Course Code and Title: EL-238 Digital Electronics

Psychomotor Domain Assessment Rubric-Level P3					
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Laboratory Session No.

Date: \_\_\_\_\_

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

### **Objective:**

To produce an astable multivibrator with Symmetrical square wave output

#### Apparatus:

- Bread Board
- Resistors (1/4 Watt), Capacitor
- Digital multimeter
- Function generator
- Oscilloscope

### **Theory:**

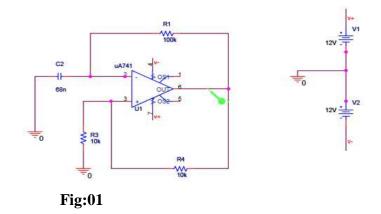
With an astable multivibrator, the op amp operates only in the non-linear region. So its output has only two voltage levels,  $V_{min}$  and  $V_{max}$ . The astable continually switches from one state to the other, staying in each state for a fixed length of time. The circuit of an astable multivibrator is shown in figure. Note that this circuit does not need an input signal. To find out the relations governing the operation of the astable, we start with the usual hypothesis that the operational amplifier has an ideal behavior. Suppose the output is in the state Vo = Vmax. When Vo takes this value the voltage VAI of the non inverting input is:

$$VAl = V_{max} \cdot R_1 / (R_1 + R_2)$$

The capacitor C starts charging through resistor R towards the value  $V_{max}$ . This charging continues until the voltage VB of the inverting input reaches the value VAI. At this point, as the inverting input voltage is more than the non-inverting input, the output switches low, to  $V_{min}$ . The voltage VA2 is now given by:

$$VA2 = V_{min} . R_1 / (R_1 + R_2)$$

At this point, the capacitor C starts discharging through R towards the voltage  $V_{min}$  until it reaches the value VA2, at which point the output switches to  $V_{max}$ . The cycle then starts again.



**Procedure:** 

- Implement the circuit.
- Connect the first probe of the oscilloscope to the output Vo of the amplifier and the second probe to the inverting input VB.
- Measure the frequency with the oscilloscope.
- Observe and record the capacitor voltage .
- Observe and record output voltage waveform.

## **Observations:**

VB (P-P)	
Vo (P-P)	
Capacitor voltage	
Frequency	

# Results!

- The approximate frequency of the oscillation of the astable multivibrator (Symmetrical square wave), when R1=R2=10k and R=100K, C = 68nf and Vmin= -Vmax comes out to be: 1 / T1+T2 =
- Draw output voltage waveform:



F/OBEM 01/05/00

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Laboratory Session No.

Date: \_\_\_\_\_

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

#### **Objective**

To determine the frequency & output amplitude of a triangular wave generator

#### **Apparatus:**

- Bread Board
- Resistors (1/4 Watt), Capacitor
- Digital multimeter
- Function generator
- Oscilloscope

#### **Theory:**

Among the waveforms that can be generated with op amps, the most common are the triangular, the ramp and the square-wave. A triangular wave can be generated with the circuit of figure F8.01.in which two operational amplifiers are used. The first operates as a comparator, while the second as an integrator. VO is the output voltage of the integrator, Vr the output voltage of the comparator. The saturation voltages Vmax and Vmin are equal in amplitude, and so can be called +Vr and -Vr respectively. Suppose the output of the comparator is +Vr. The voltage  $V_o$  will be a negative ramp which will continue to grow until the voltage of the non-inverting input of the comparator rises above zero. The minimum value of the output voltage  $V_o$  applying the superposition principle, will be given by:

$$V_o = (Vr^* R_3 + V_o * R_1)/R_1 + R_3$$
  
 $V_o = -Vr^* R_3/R_1$ 

From which we get:

The same principles apply for the maximum voltage the output reaches, with the only difference that the ramp is raising and the voltage Vr is negative: defining this voltage as  $V_0$ ' we have:

$$Vo' = Vr * R_3 / R_1$$

To calculate the time T taken to rise from Vo to VO' remember that the capacitor C charges

with a constant current given by:

$$I = Vr / (P + R_2)$$

So, from:

$$I = - C * dVo / dt$$

We find that:

$$Vr / (P+R_2) = - C*dVo / dt$$

From which:

V o' -Vo = -  $Vr^{*}T/C^{*}(P+R_{2})$ 

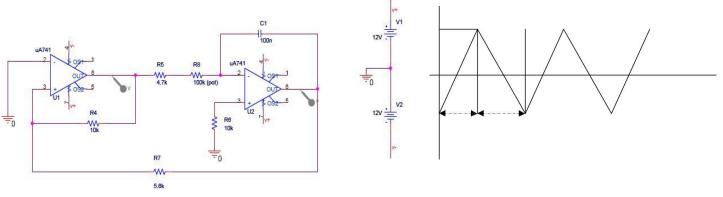
Vo' -Vo = 
$$2*Vr*R_3 / R_1$$

we have:

 $T = 2*R3*(P + R_2)*C / R_1$ 

The time T is equal to half period, so the output frequency F will be the inverse of twiceT:

 $F = \frac{R1}{[4*R3*(R2+P)*C]}$ 





### **Procedure:**

- Adjust 100kΩ potentiometer completely CCW to obtain zero resistance and measure the output voltage value of the comparator (1<sup>st</sup> op-amp) using oscilloscope.
- Adjust the potentiometer to half value.
- Calculate the amplitude of the output voltage (2<sup>nd</sup> op-amp).
- Measure the amplitude of the output voltage with the oscilloscope.
- Calculate the output voltage frequency according to the formulae.
- Measure the output frequency with the oscilloscope.
- Check the presence of a square wave at the output of the comparator (1<sup>st</sup> op-amp)

#### **Observations:**

Vout (triangular)	
Frequency	

# **Results:**

The approximate frequency of the oscillation of the astable multivibrator comes out to be:

The output voltage of the oscillation of the astable multivibrator comes out to be:



F/OBEM 01/05/00

# NED University of Engineering & Technology Department of Electronic Engineering Course Code and Title: EL-238 Digital Electronics

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Q1-111 Q - ( -		Extent of Achievement			
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Laboratory Session No.	Date:
Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

## **Objective:**

Implementation of Bistable Multivibrator using 555 timer

## Apparatus:

- Breadboard
- Oscilloscope
- 555 timer IC
- Capacitor 10 nF, 1uF
- Resistor sheet
- LEDs
- Push button switch

# **Theory:**

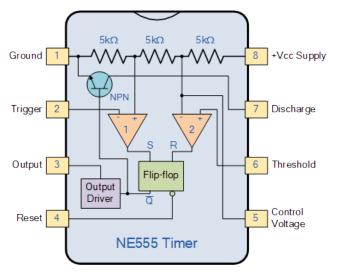
Multivibrators and CMOS Oscillators can be easily constructed from discrete components to produce relaxation oscillators for generating basic square wave output waveforms. But there are also dedicated IC's especially designed to accurately produce the required output waveform with the addition of just a few extra timing components. One such device that has been around since the early days of IC's and has itself become something of an industry "standard" is the **555 Timer Oscillator** which is more commonly called the "**555 Timer'**.

The **555 Timer** which gets its name from the three  $5k\Omega$  resistors it uses to generate the two comparators reference voltage, is a very cheap, popular and useful precision timing device that can act as either a simple timer to generate single pulses or long time delays, or as a relaxation oscillator producing stabilized waveforms of varying duty cycles from 50 to 100%.

The 555 timer chip is extremely robust and stable 8-pin device that can be operated either as a very accurate *Monostable*, *Bistable* or *Astable* Multivibrator to produce a variety of applications such as one -shot or delay timers, pulse generation, LED and lamp flashers, alarms and tone generation, logic clocks, frequency division, power supplies and converters etc, in fact any circuit that requires some form of time control as the list is endless.

The single 555 Timer chip in its basic form is a Bipolar 8-pin mini Dual-in-line Package (DIP) device consisting of some 25 transistors, 2 diodes and about 16 resistors arranged to form two comparators, a flip - flop and a high current output stage as shown below. As well as the 555 Timer there is also available the NE556 Timer Oscillator which combines TWO individual 555's within a single 14-pin DIP package and low power CMOS versions of the single 555 timer such as the 7555 and LMC555 which use MOSFET transistors instead.

A simplified "block diagram" representing the internal circuitry of the **555 timer** is given below with a brief explanation of each of its connecting pins to help provide a clearer understanding of how it works.



## Fig:01

- Pin 1. Ground, The ground pin connects the 555 timer to the negative (0v) supply rail.
- Pin 2. Trigger, The negative input to comparator No 1. A negative pulse on this pin "sets" the internal Flip-flop when the voltage drops below 1/3Vcc causing the output to switch from a "LOW" to a "HIGH" state.
- Pin 3. Output, The output pin can drive any TTL circuit and is capable of sourcing or sinking up to 200mA of current at an output voltage equal to approximately Vcc -1.5V so small speakers, LEDs or motors can be connected directly to the output.
- Pin 4. **Reset**, This pin is used to "reset" the internal Flip-flop controlling the state of the output, pin 3. This is an active-low input and is generally connected to a logic "1" level when not used to prevent any unwanted resetting of the output.
- Pin 5. **Control Voltage**, This pin controls the timing of the by overriding the 2/3Vcc level of the voltage divider network. By applying a voltage to this pin the width of the output signal can be varied independently of the RC timing network. When not used it is connected to ground via a 10nF capacitor to eliminate any noise.
- Pin 6. **Threshold**, The positive input to comparator No 2. This pin is used to reset the Flipflop when the voltage applied to it exceeds 2/3Vcc causing the output to switch from "HIGH" to "LOW" state. This pin connects directly to the RC timing circuit.
- Pin 7. **Discharge**, The discharge pin is connected directly to the Collector of an internal NPN transistor which is used to "discharge" the timing capacitor to ground when the output at pin 3 switches "LOW".
- Pin 8. **Supply** +**Vcc**, This is the power supply pin and for general purpose TTL 555 timers is between 4.5V and 15V.

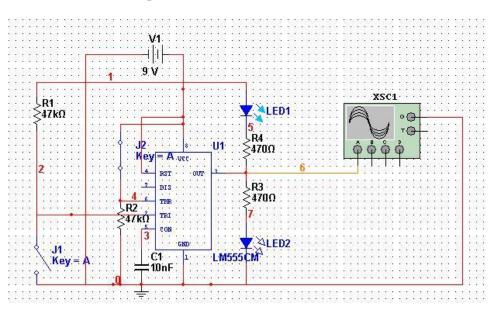
The **555 Timers** name comes from the fact that there are three  $5k\Omega$  resistors connected together internally producing a voltage divider network between the supply voltage at pin 8 and ground at pin 1. The voltage across this series resistive network holds the positive input of comparator two at 2/3Vcc and the positive input to comparator one at 1/3Vcc.

The two comparators produce an output voltage dependent upon the voltage difference at their inputs which is determined by the charging and discharging action of the externally connected RC network. The outputs from both comparators are connected to the two inputs of the flip-flop which in turn produces either a "HIGH" or "LOW" level output at Q based on the states of its inputs. The output from the flip-flop is used to control a high current output switching stage to drive the connected load producing either a "HIGH" or "LOW" voltage level at the output pin.

The most common use of the 555 timer oscillator is as a simple astable oscillator by connecting two resistors and a capacitor across its terminals to generate a fixed pulse train with a time period determined by the time constant of the RC network. But the 555 timer oscillator chip can also be connected in a variety of different ways to produce Monostable or Bistable multivibrators as well as the more common Astable Multivibrator.

### **Bistable 555 Timer**

The **555 Bistable** is one of the simplest circuits we can build using the 555 timer oscillator chip. This bistable configuration does not use any RC timing network to produce an output waveform so no equations are required to calculate the time period of the circuit. Consider the Bistable 555 Timer circuit below.



## Fig:02

### **Procedure:**

- Implement the circuit and change the switch position each time to observe the working of bistable multivibrator on oscilloscope.
- Note down the maximum output voltage.

### **Results:**

The output turns high when \_\_\_\_\_\_ is closed and turns low when \_\_\_\_\_\_ is closed.



### F/OBEM 01/05/00

Date: \_\_\_\_\_

## NED University of Engineering & Technology Department of Electronic Engineering Course Code and Title: EL-238 Digital Electronics

Psychomotor Domain Assessment Rubric-Level P3					
G1-11 G - ( -		Extent of Achievement			
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## Laboratory Session No.

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Remarks	
Instructor's Signature with Date:	

# OPEN ENDED LAB

## **Objective:** To design and implement a 4 input Multiplexer circuit using logic gates.

**Background:** A multiplexer is a combinational circuit that takes multiple inputs and delivers Only a single output. It consists of input data lines, selection lines and a single output. It is a data selector that provides the mechanism to select single binary information from many input lines and passes it to output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2<sup>n</sup> input lines and n selection lines.

# **OEL Details:**

- Understand the concept of multiplexing in the context of digital logic circuits.
- To learn about the internal logic of digital multiplexers.
- Using background knowledge, understand and analyze the function and logic circuit of 4 to 1 multiplexer.
- Make a logic diagram/circuit for the implementation.
- Choose suitable components/ logic gates for the design and implement it using breadboard.
- Check your designed circuit for various combinations of input.
- Observe and record the output/results and verify the truth table.

# **Deliverables:**

- A functional circuit of 4 to 1 multiplexer.
- Project report should include the following:
  - Open ended lab problem/statement
  - Details of components used
  - Logic diagram /circuit diagram
  - Procedure/Explanation of the circuit constructed
  - Troubleshooting /problem faced during implementation/ experiential learning experience
  - Truth table verification and circuit output
  - > Any other findings
  - Investigate and record the applications of Multiplexer and describe any one application in detail.
  - Result/conclusion

## Note:

- 1. Assessment shall be carried out on the basis of Rubrics [Psychomotor level-P3] and in the  $11^{\text{th}}$  week of semester.
- 2. OEL has to be done in groups. Each group can have a maximum of three students.



# NED University of Engineering & Technology Department of Electronic Engineering Course Code and Title: EL-238 Digital Electronics

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