Department of Electronic Engineering

N.E.D. University of Engineering & Technology,

PRACTICAL WORK BOOK

For the course

ELECTRONICS DEVICES & CIRCUITS (EDC)

(EL - 236) For S.E (EL)

Instructors name:______________________________
Student Name: ______________________________
Roll no.:________________ Batch: _____________
Semester :_____________ Year:_______________
Department: _________________________________

LABORATORY WORK BOOK

FOR THE COURSE

Electronics Devices & Circuit (EDC) (EL-236)

Prepared By:
Ayesha Akhtar (Lecturer)
Revised By:
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Reviewed By:
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Approved By:
The Board of Studies of Department of Electronic Engineering

Electronics Devices & Circuits laboratory
CONTENTS

LAB SESSION 01

Objective:

A. Identify the type of transistor.

B. Implement the voltage divider bias circuit and find DC voltages and current values. Also determine its mode of operation**.**

Equipment Required:

- Protoboard
- DC supply
- Resistors
- BJT (Q2N2222)
- Digital Multimeter
- Connecting Wires

Theory:

A transistor is a solid state device made from semiconductor material with connections made at three or more points where the electrical characteristics are different. The term transistor comes from the words transfer and resistor. The term was adopted because it best describes the actual operation of transistor, the transfer of an input signal current from a low resistance circuit to a high resistance output circuit.

A transistor must be properly biased in order to operate as an amplifier. DC biasing is used to establish a steady level of transistor current and voltage called the dc operating point (Q-Point).Voltage divider bias provides good Q-point stability with a single polarity supply voltage. It is the most common bias circuit, as mentioned in Figure 1.

Circuit Diagram:

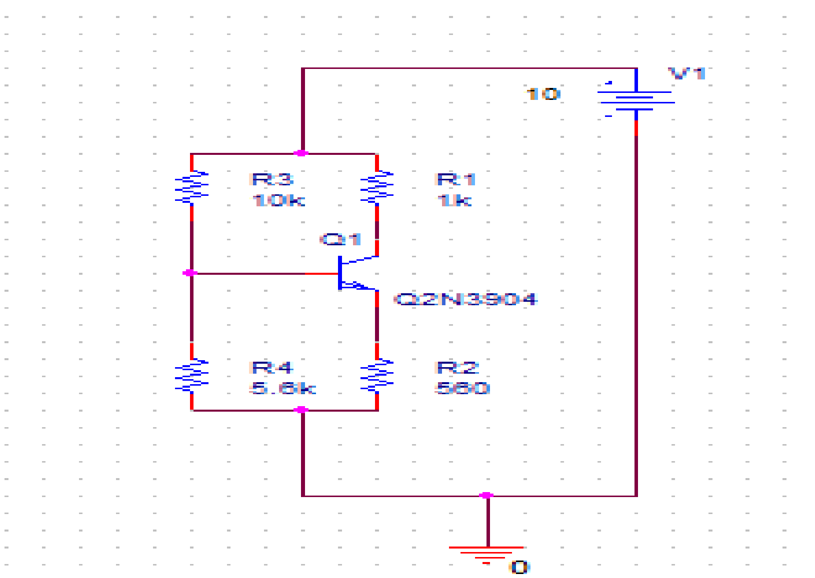

Figure 1: DC Analysis Of BJT using voltage divider circuit

Observations:

Parameters	Measured value	Calculated value
I_C		
V_E		
V_B		
V_C		
V_{CE}		
V_{BE}		

Mode of operation: ______________________________

Calculations:

Results:

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NED University of Engineering & Technology
Department of **ELECTRONIC** Engineering
Course Code and Title: **EL-236 ELECTRONIC DEVICES & CIRCUITS**

Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	Extent of Achievement				
	0	1	2	3	4
Equipment Identification Sensory skill to ***identify*** equipment and/or its component for a lab work.	Not able to identify the equipment.	--	--	--	Able to identify equipment as well as its components.
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Laboratory Session No. ___________ Date: ____________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 02

Objectives:

A. To investigate the operation of Common Emitter Amplifier
B. To describe the purpose of components present in Common Emitter Amplifier

Equipment Required:

- Protoboard
- 0-15 V dc power supply
- Resistors , Capacitors
- BJT
- Digital Multimeter
- Oscilloscope
- Function generator

Theory:

The CE Amplifier is one of the three basic transistor amplifier circuit used in electronic industry. In this configuration input is applied at the base lead while its output is taken at collector, which is in 180^ophase shift. The CE Amplifier exhibits high voltage and current gain.

The term "common emitter "comes from the fact that the emitter node of the transistor is connected to a "common" power rail, usually the ground. The collector node goes to the output of the circuit and the base node is an input here is design of the circuit as shown in figure. The resistor R_C is used to load the circuit via Vcc, other elements are used to bias the transistor.R_E and R_C seems to break the term "common emitter" because the emitter is not connected anymore directly to the ground but the point is that for all the frequencies we used, C_E acts as a low impedance capacitor so the transistor emitter is decoupled to the ground .Re does a negative feedback which increases the stability of the transistor; this is called the emitter degeneration.in order to ensure the common emitter transistor amplifier configuration, the transistor has to be in active mode otherwise, the output is distorted due to a clipping in the negative part of the input signal.to do so ,R_1& R_2 must be chosen to have a base emitter voltage of around 0.7v, the "on" voltage of a transistor. The common emitter circuit which will be implemented in Figure 1.

Circuit Diagram:

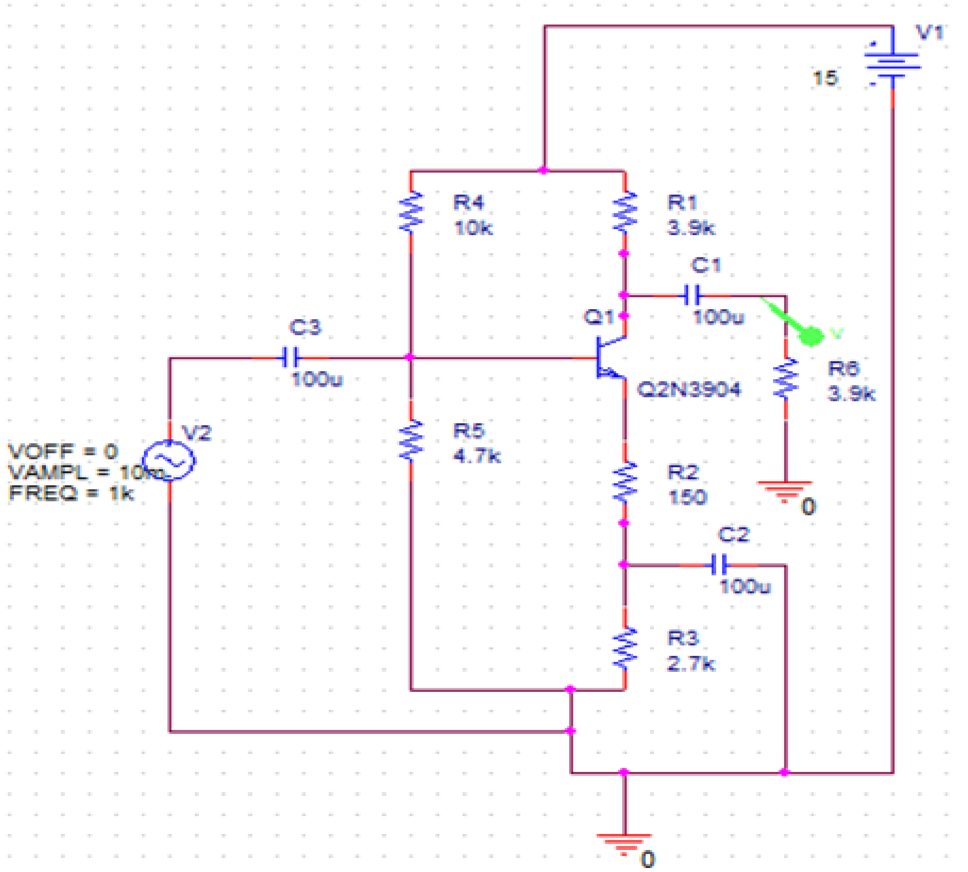

Figure 1: Common Emitter Amplifier

Observations:

1. DC analysis

Parameters	Measured value	Calculated value
V_E		
V_B		
V_C		

Mode Of Transistor:___________

2. AC Analysis

S.No	Vamp	V_{out} (with by-pass capacitor)	Voltage Gain
1			

2			
3			

S.No	**Vamp**	**V_{out} (without by-pass capacitor)**	**Voltage Gain**
1			
2			
3			

4. Draw input and output voltage waveform (from AC Analysis)

(For any one observation) (Without Using Output By-Pass Capacitor)

(For any one observation) (Without Using Output By-Pass Capacitor)

Calculations:

(Show formulas for calculating voltage gain, for any one observation)

Result:

The gain of the common emitter amplifier with load is: _________________
The gain of the common emitter amplifier without load is: _______________
The phase shift between input and output signal of common emitter amplifier is ____________.

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NED University of Engineering & Technology
Department of ELECTRONIC Engineering
Course Code and Title: **EL-236 ELECTRONIC DEVICES & CIRCUITS**

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Laboratory Session No. ___________ Date: ____________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 03

Objective:
To analyse the frequency response of Common Emitter Amplifier

Equipment Required:
- Protoboard
- 0-15 V dc power supply
- Resistors , Capacitors
- BJT
- Digital Multimeter
- Oscilloscope
- Function generator

Theory:
A Common-Emitter amplifier is one of three basic single-stage bipolar-junction-transistor (BJT) amplifier topologies, typically used as a voltage amplifier. In this circuit the base terminal of the transistor serves as the input, the collector is the output, and the emitter is common to both (for example, it may be tied to ground reference or a power supply rail), hence its name.

EMITTER DEGENERATION RESISTANCE RE introduces negative feedback in the amplifier circuit. C3 is coupling capacitors. Since $X_C=1/2\pi fC$, hence at low frequencies the reactance is greater and it decreases as the frequency increases. At low frequencies the reactance of coupling capacitance is high (The coupling and bypass capacitances are usually in microfarads) , hence they act as almost open circuit .Therefore at low frequencies the coupling capacitances act as nearly as open circuit The bypass capacitance also acts as nearly open circuit at low frequency.

In mid range frequency the coupling and by-pass capacitance act as nearly short circuit. At high frequencies, the coupling and bypass capacitors become effective ac shorts and do not effect amplifier's response.

For measuring frequency response, common emitter circuit which is to be implemented in mentioned in Figure 1.

Circuit Diagram:

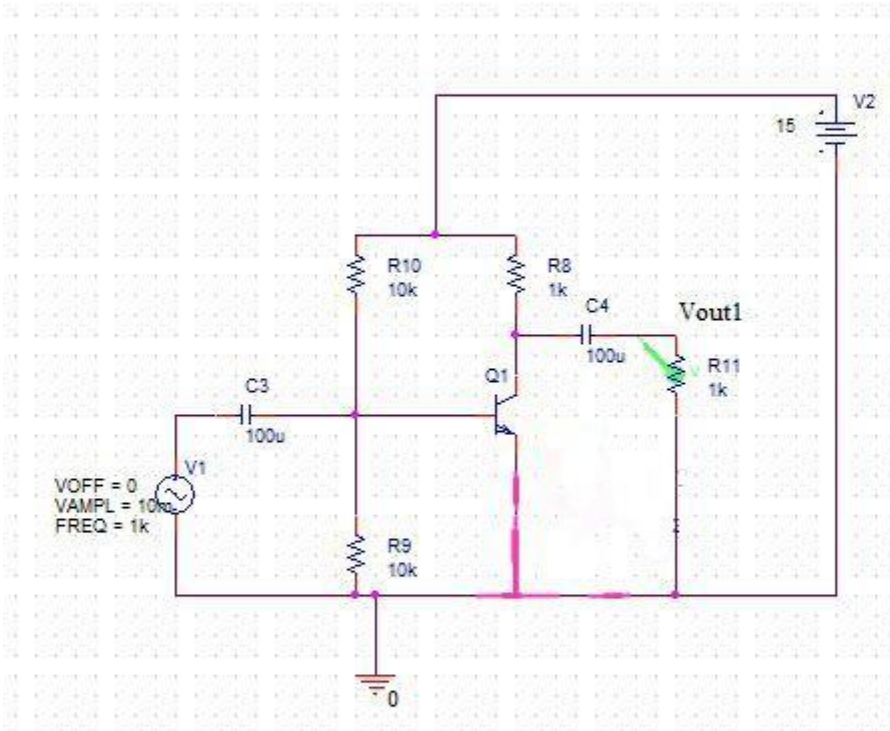

Figure 1: Common Source Amplifier

Observations:

FREQUENCY RESPONSE

S.NO	FREQUENCY	V2	OUTPUT VOLATGE	Voltage Gain
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

Calculations:
(Show calculations for any one observation)

Result:

The bandwidth of the common emitter amplifier as measured comes out to be: ____________

Plotting:

Plot the curve between output voltage versus frequency.

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NED University of Engineering & Technology
Department of ELECTRONIC Engineering
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Laboratory Session No. ___________ Date: ____________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 04

Objective:

A. To investigate the operation of Common Collector Amplifier
B. To describe the purpose of components present in Common Collector Amplifier

Equipment Required:

- Protoboard
- 0-15 V dc power supply
- Resistors , Capacitors
- BJT
- Digital Multimeter
- Oscilloscope
- Function generator

Theory:

The Common Collector amplifier is also known as 'Emitter Follower'. In CC Amplifier input is taken at base while output at emitter. In this configuration output follows input. The input impedance of CC amplifier is much higher than bipolar transistor amplifier. The common collector amplifier which is to implemented is mentioned in Figure 1.

Circuit Diagram:

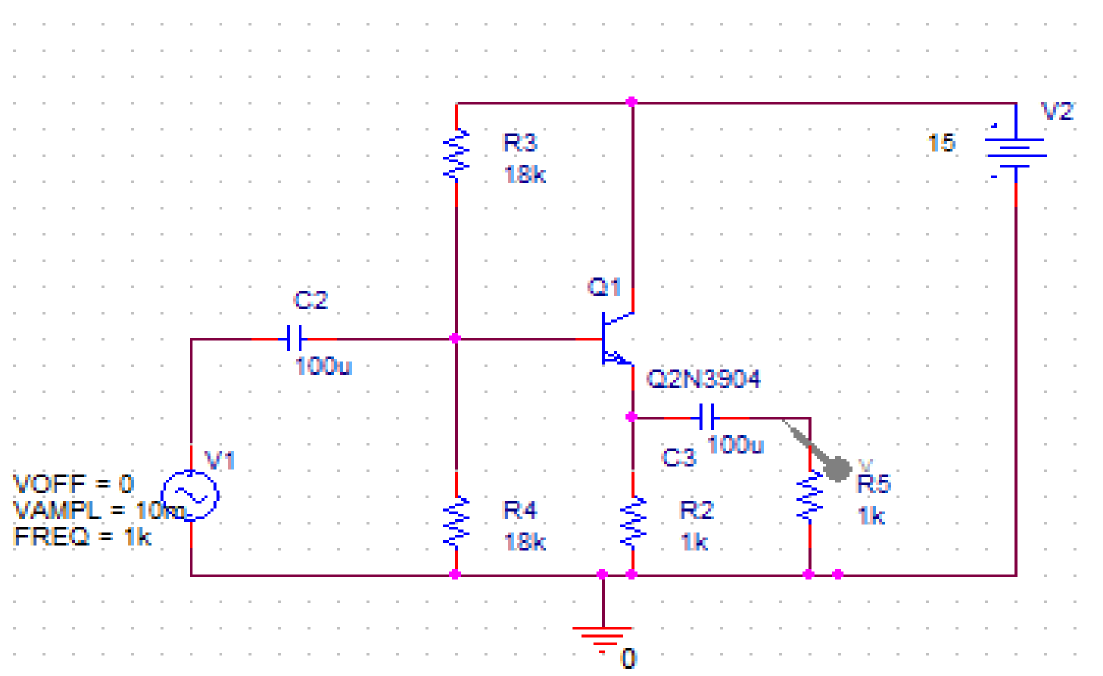

Figure 1: Common Collector Amplifier

Observations:

1. **DC Analysis**

Parameters	**Measured value**	**Calculated` value**
V_E		
V_B		
V_C		

Mode Of Transistor: ______________

2. AC analysis: (Apply different peak to peak sinusoidal input from function generator, measure output voltage)

V1	**V_{out} (with load resistor)**	**V_{out} (without load resistor)**	**Voltage Gain**

3. Calculate voltage gain (for any one obersavation):

Without Load Resistors

With Load Resistor

4. Draw input and output voltage waveform

Without Load Resistors:

With Load Resistor:

Results:

The gain of the common collector amplifier with load is: ________________
The gain of the common collector amplifier without load is: ______________
The phase shift between input and output signal of common collector amplifier is __________.

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Laboratory Session No. ___________ Date: ____________________

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Remarks	
Instructor's Signature with Date:	

LAB SESSION 05

Objective:
To demonstrate the operation of Combination of CE Amplifier and Emitter Follower (CC) Amplifier

Equipment Required:
- Protoboard
- 0-15 V dc power supply
- Resistors , Capacitors
- BJT
- Digital Multimeter
- Oscilloscope
- Function generator

Theory:
Combination of CE and CC Amplifier is known as phase-splitter or paraphase amplifier which is capable of producing two identical output signals to identical loads except that they are 180^o out-of-phase with each other. The output signal from the collector is simply a CE amplifier having unity voltage gain and also 180^{o}out-of-phase with the input signal. Output is from the emitter-follower and is in-phase with the input signal. Circuit diagram for practical analysis is presented in Figure 1.

Circuit Diagram:

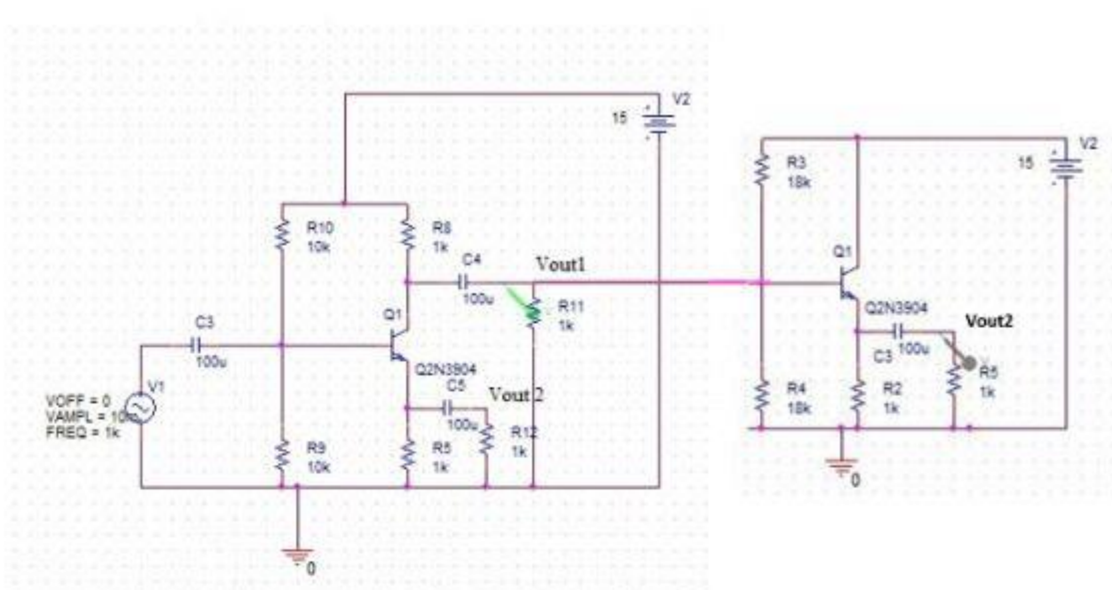

Figure 1 : Common Emitter Amplifier cascaded with common collector amplifier

Observations:

1. DC analysis

Parameters	Measured value	Calculated value	Mode of transistor
V_{E1}			
V_{B1}			
V_{C1}			
V_{E2}			
V_{B2}			
V_{C2}			

2. AC analysis

S.No	Vin	Frequency	Vout1	Vout2	Voltage Gain (1st stage)	Voltage Gain 2nd Stage	Overall Voltage Gain
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							

3. Draw input and output voltage waveform. (For Any one frequency point)

Calculations: (For Any one frequency point)

Volatge Gain Calculation:

1st Stage:

2nd Stage

Overall Gain

Result :

Vout1 with load resistor is: _____________
Vout1 without load resistor is: __________
Vout2 with load resistor is: _____________
Vout2 without load resistor is: __________

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NED University of Engineering & Technology
Department of ____**ELECTRONIC**__ Engineering
Course Code and Title: ____**EL-236 ELECTRONIC DEVICES & CIRCUITS**_____

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Laboratory Session No. ___________ Date: _____________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 06

Objective:
To demonstrate the operation of BJT as a Switch

Equipment Required:
- Protoboard
- 0-15 V dc power supply
- Resistors
- BJT
- Digital Multimeter
- Oscilloscope
- Function generator
- LED

Theory:
Switches are needed in electronics to turn-on a voltage or current of sufficient power to operate a circuit. A bipolar junction transistor (BJT) can be used in many circuit configurations such as an amplifier, oscillator, filter, and rectifier or just used as an on-off switch. If the transistor is biased into the linear region, it will operate as an amplifier or other linear circuit, if biased alternately in the saturation and cut-off regions, then it is being used as a switch, allowing current to flow or not to flow in other parts of the circuit.

A switch consists of a BJT transistor that is alternately driven between the saturation and cut-off regions. A simple version of the switch is shown in figure. When the input equals $-V_{in}$, the base-emitter junction is reverse biased or off so no current flows in the collector. This is illustrated by the load line shown in the figure.

This state is similar to an open switch.

When the input equals $+V_{in}$, the transistor is driven into saturation and the following conditions occur:

This state is similar to a closed switch connecting the bottom of R_C to ground. BJT circuit which is to be implemented as a digital logic inverter is presented in Figure 1.

Circuit Diagram:

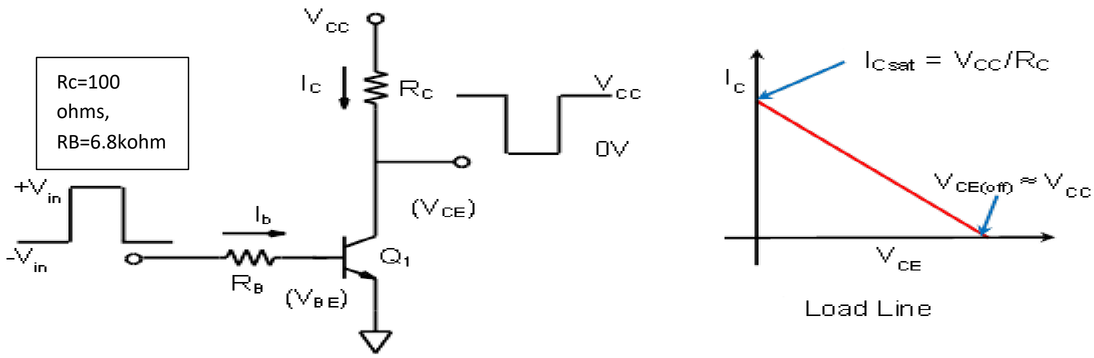

Figure 1: BJT operated as a switch operating as a digital logic inverter

Observations:

Take R_B = 6.8kohm, R_C= 100ohm, LED (any colour), Vcc = 5V
Connect an LED at the collector terminal such that its cathode should be connected to collector terminal. Observe the LED as the input goes low and high. Also measure voltages and current in the given circuit and write below:

S.No	Vin	Vout(VCE)
1		
2		
3		
4		
5		

Result :

When logic input is 0 the switch is: _________
When logic input is 1 the switch is: _________

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NED University of Engineering & Technology
Department of ____**ELECTRONIC**__ Engineering
Course Code and Title: ____**EL-236 ELECTRONIC DEVICES & CIRCUITS**_____

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Laboratory Session No. ___________ Date: ______________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 07

Objective:
To investigate the Operation of BJT Current Mirror

Equipment Required:
- Protoboard
- Q2N3904 BJT npn transistors
- Resistors, Capacitors
- Digital Multimeter
- Function Generator
- Oscilloscope
- Connecting wires

Theory:
The basic BJT Current Mirror is shown in figure. Neglecting base current, the reference Current I_{ref} is passes through the diode connected transistor Q1, & thus produces corresponding voltage V_{be}, which in turn is applied between base & emitter of Q2. If Q2 is matched to Q1, then the collector current of Q1 is equal to that of Q1. Circuit Digaram for implemtation of basic current source is illustrated in Figure 1.

Circuit Diagram:

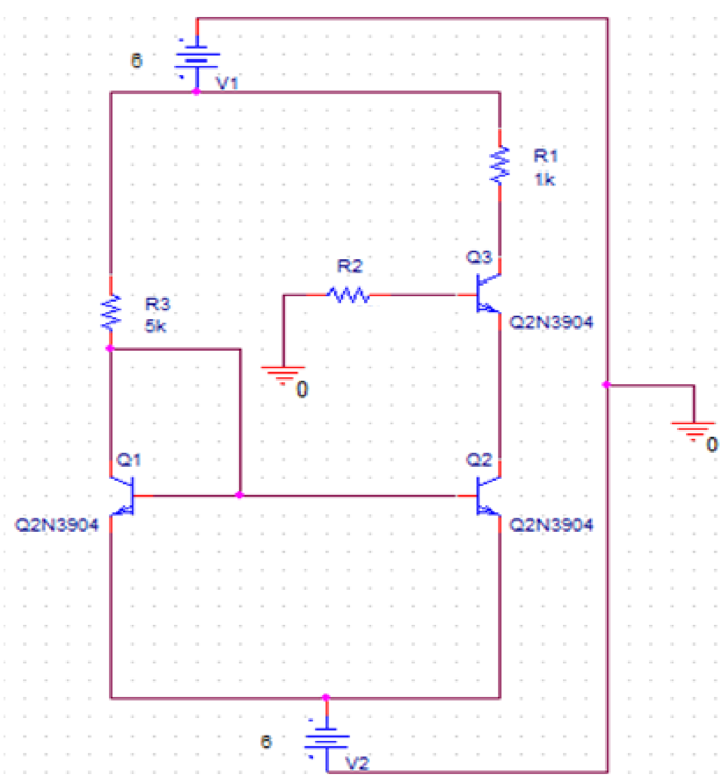

Figure 1: Basic Current Source

Procedure:

- Implement the circuit given in figure 3.
- Vary the potentiometer and observe changes in I_{ref} and I_o

Observations:

S.No	Ref	Iref	Io
1			
2			
3			
4			
5			

Calculations:

Make calculation of Io for the observed value of Iref. Also calculate the percentage error.

Result:

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Department of ____ELECTRONIC__ Engineering
Course Code and Title: ____EL-236 ELECTRONIC DEVICES & CIRCUITS_____

Psychomotor Domain Assessment Rubric-Level P3					
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Laboratory Session No. ___________ Date: ______________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 08

Objective:
To illustrate the operation of current source implemented using BJT, with Base-Current Compensation.

Equipment Required:
- Protoboard
- Q2N3904 BJT npn transistors
- Resistors, Capacitors
- Digital Multimeter
- Function Generator
- Oscilloscope
- Connecting wires

THEORY:
Figure shows a bipolar current mirror with a current transfer ratio that is much less dependent on β than that of simple current mirror. The reduced dependence is achieved by using transistor Q3. Figure 1 shows the practical circuit for base current compensated current source.

Circuit Diagram:

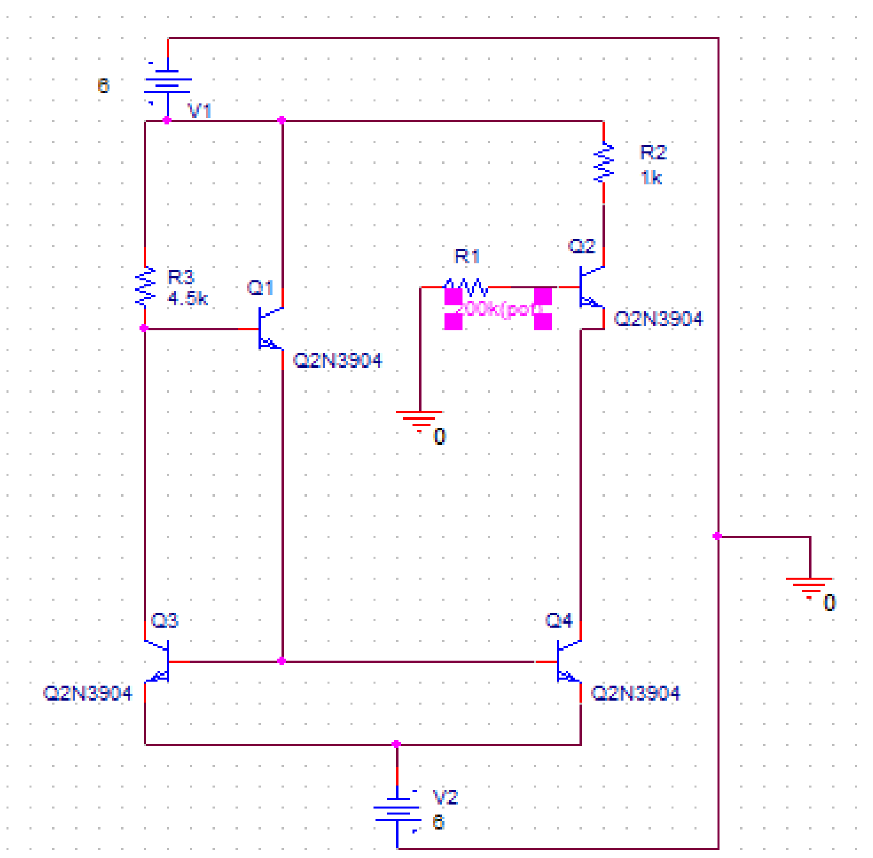

Figure 1 : Current Source With Base Current Compensation

Procedure:

- Implement the circuit in figure 2 .
- Vary potentiometer & observe readings for I_{ref} & I_o

Observations:

S. No	Iref	Io
1		
2		
3		
4		
5		
6		
7		
8		

Calculations:

Make calculation of Io for the observed value of Iref. Also calculate the percentage error.

Result:

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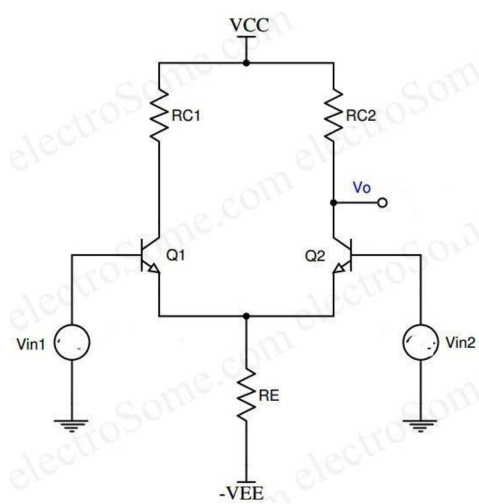
LAB SESSION 9

Objective:
To illustrate the operation of BJT Differential Pair

Equipment Required:
- Protoboard
- Q2N2222 BJT npn transistors
- Resistors, Capacitors
- Digital Multimeter
- Function Generator
- Oscilloscope
- Connecting wires

Theory:
It consists of two matched transistors, Q1 & Q2, whose emitters are joined together and biased by constant current source I. It is essential that, collector circuits be such that Q1 & Q2 never enter saturation. BJT Differential Pair circuit diagram is presented in Figure 1.

Circuit Diagram:



RC1=RC2=4k ohms

RE=1k ohms

VCC=15V

VEE=-15V

Vin1=VB1, Vin2=VB2

Figure 1: BJT Differential Pair

Observations:

S.No	V_{B1}	V_{B2}	$V_{B1}-V_{B2}$	V_{C1}	V_{C2}	$V_{C1}-V_{C2}$
1						
2						
3						

Result :

Differential pair responds to _________________ inputs.
Differential pair rejects ______________________ inputs.

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Laboratory Session No. ___________ Date: _____________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 10

Objective:
To investigate the characteristics curves for Field Effect Transistor.

Equipment Required:
- D.C power supply
- Oscilloscope
- Multimeter
- MOSFET 2N7000
- Resistors

Basic Theory:

The acronym 'FET' stands for field effect transistor. It is a three-terminal unipolar solid state device in which current is controlled by an electric field as is done in vacuum tubes.
Broadly speaking, there are two types of FETs:
(a) Junction field effect transistor (JFET)
(b) metal-oxide semiconductor FET (MOSFET)

MOSFET with V_{GS}=0 and V_{DS}=0
With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source. One diode is formed by the pn junction between the n^+ drain region and the p-type substrate, and the other diode is formed by the pn junction between the p-type substrate and the n^+ source region. These back-to-back diodes prevent current conduction from drain to source when a voltage v_{DS} is applied. In fact, the path between drain and source has a very high resistance (of the order of $10^{12}\,\Omega$).

MOSFET with small V_{GS} and V_{DS}=0
Consider next the situation depicted in Fig. 4.2. Here we have grounded the source and the drain and applied a positive voltage to the gate. Since the source is grounded, the gate voltage appears in effect between gate and source and thus is denoted v_{GS}. The positive voltage on the gate causes, in the first instance, the free holes (which are positively charged) to be repelled from the region of the substrate under the gate (the channel region). These holes are pushed downward into the substrate, leaving behind a carrier-depletion region. The depletion region is populated by the bound negative charge associated with the acceptor atoms. These charges are "uncovered" because the neutralizing holes have been pushed downward into the substrate. As well, the positive gate voltage attracts electrons from the n^+ source and drain regions (where they are in abundance) into the channel region. When a sufficient number of electrons accumulate near the surface of the substrate under the gate, an n region is in effect created, connecting the source and drain regions. Now if a voltage is applied between drain and source, current flows through this induced n region, carried by the mobile electrons. The induced n region thus forms a channel for current flow from drain to source and is aptly called so. Correspondingly, the MOSFET is called an n-channel MOSFET or, alternatively, an NMOS transistor. Note that an n-channel MOSFET is formed on a p-type

substrate: The channel is created by inverting the substrate surface from p type to n type. Hence the induced channel is also called an inversion. The value of vGS at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the **threshold voltage** and is denoted V_t Obviously, for an n-channel FET is positive. The value of V_t is controlled during device fabrication and typically lies in the range of 0.5 V to 1.0 V.

MOSFET with small V_{GS} and small V_{DS}:

Having induced a channel, we now apply a positive voltage V_{DS} between drain and source. We first consider the case where V_{DS} is small (i.e., 5 0 mV or so). The voltage V_{DS} causes a current i_D to flow through the induced n channel. Current is carried by free electrons traveling from source to drain (hence the names source and drain). By convention, the direction of current flow is opposite to that of the flow of negative charge. Thus the current in the channel, i_D, will be from drain to source. The magnitude of i_D depends on the density of electrons in the channel, which in turn depends on the magnitude of V_{DS} . Specifically, for V_{GS} = V, the channel is just induced and the current conducted is still negligibly small. As V_{GS} exceeds V_t, more electrons are attracted into the channel. We may visualize the increase in charge carriers in the channel as an increase in the channel depth. The result is a channel of increased conductance or, equivalently, reduced resistance. In fact, the conductance of the channel is proportional to the **excess gate voltage** (V_{GS} - V_t), also known as t h e **effective voltage** or the **overdrive voltage.** It follows that the current i_D will be proportional to **V_{GS} - V_t,** and, of course, to the voltage V_{DS} that causes i_D to flow.

MOSFET with small V_{GS} and large V_{DS}:

We next consider the situation as V_{DS} is increased. For this purpose let V_{GS} be held constant at a value greater than V,. V_{DS} appears as a voltage drop across the length of the channel. That is, as we travel along the channel from source to drain, the voltage (measured relative to the source) increases from 0 to V_{DS}. Thus the voltage between the gate and points along the channel decreases from V_{GS} at the source end to V_{GS} - V_{DS} at the drain end. Since the channel depth depends on this voltage, we find that the channel is no longer of uniform depth; rather, the channel will take the tapered form being deepest at the source end and shallowest at the drain end. As V_{DS} is increased, the channel becomes more tapered and its resistance increases correspondingly. Thus the i_D-V_{DS} curve does not continue as a straight line but bends

Eventually, when V_{DS} is increased to the value that reduces the voltage between gate and channel at the drain end to V_t—that is, $V_{GD} = V_t$ or $V_{GS} - V_{DS} = V_t$ or $V_{DS} = V_{GS} - V_t$— the channel depth at the drain end decreases to almost zero, and the channel is said to be **pinched off.** Increasing V_{DS} beyond this value has little effect (theoretically, no effect) on the channel shape, and the current through the channel remains constant at the value reached for V_{DS} - V_{GS} - V,. The drain current thus **saturates** at this value, and the MOSFET is said to have entered the **saturation region** of operation. The voltage V_{DS} at which saturation occurs is denoted by V_{DSsat}

$$V_{DSsat} = V_{GS} - V_t$$

Obviously, for every value of V_{GS} > V,, there is a corresponding value of V_{DSsat} The device operates in the saturation region if V_{DSsat}. The region of the i_D-V_{DS} characteristic obtained for $V_{DS} < V_{Dsat}$ is called the **triode region,** a carryover from the days of vacuum-tube devices whose operation a F E T resembles. Circuit diagram to be implemented is presented in Figure 1.

Procedure & Circuit Diagram:

1. Connect the circuit as shown in fig 3.
2. Let V_{DS} = (0, 0.5, 1, 1.5, 2, 2.5, 3, 4, 5, 5, 5.5, 6, 6.5, 7) V measure I_D.
3. Repeat step 2 for V_{GS} in the range of 0-3 V.

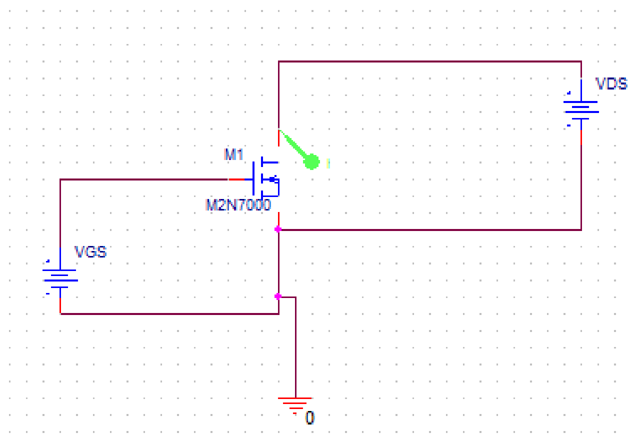

Figure 1: MOSFET DC Analysis & Characteristic Curves

Observations & Calculations

A. Draw I_D Vs V_{GS}

a) *For V_{DS}=10V*

V_{GS}															
I_D															

B. Draw (drain characteristics) between I_D & V_{DS} for different values of V_{GS}.

a. *For* V_{GS} *=0.5V*

V_{DS}															
I_D															

b. *For* V_{GS} *=1.5V*

V_{DS}															
I_D															

c. *For* V_{GS} *=2V*

V_{DS}															
I_D															

Results:

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Laboratory Session No. ___________ Date: _____________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 11

Objective:

To illustrate the operation of Common Gate Amplifier and also determine phase shift between input and output

Equipment Required:

• Protoboard

- Protoboard
- Function Generator
- Digital Multimeter
- Power Supply
- Resistors
- Transistors: 1 x 2N7000
- Capacitors

Theory:

MOS transistor is a voltage controlled device, where gate voltage modulates the channel resistance and voltage between drain and source determines current flow between the drain and source terminals. Like BJT, MOS transistor can perform as amplifier and as electronic switch. MOS comes in two different flavors, as NMOS and as PMOS.

Common Gate Amplifier:

As shown in figure, the common gate amplifier has a grounded gate terminal , a signal input at the source terminal and the output taken at the drain.

Circuit Diagram:

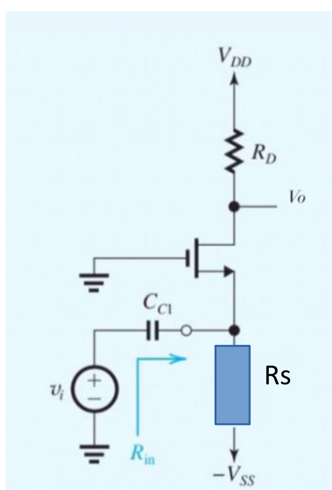

Figure 1: Common Gate Amplifier

Rs=1kohms, Rd=2.2kohms VDD=15V. VSS=-15V

Hence Common Gate amplifiers have

- Non-Inverting output
- Moderate input resistance
- Moderately large small signal voltage gain but smaller than common source amplifier.
- Small signal current gain less than one.
- Potentially large output resistance (Dependent on R_D)

Procedure:

- Implement a common-gate amplifier, as shown in Figure .
- Construct the circuit in circuit Figure . Be sure to use the correct polarity for the coupling capacitors, or the circuit may not function properly.
- Current source is to be replaced with 10k ohms resistor
- With the power supply on, the function generator connected to the input port, and the oscilloscope set to observe the input voltage *Vin* , adjust the amplitude of the function generator such that *Vin* is a 10mV sinusoid at 1kHz. Then measure and record the AC voltage gain *Vout / Vin*

Analysis:

Determine the gate , drain and source voltage . perform all necessary calculations .Let Vt= 1V . justify that the circuit can be used as an amplifier

Observations:

1. DC analysis

Parameters	Measured value	Calculated value	Mode Of transistor
V_G			
V_S			
V_D			

2. AC Analysis (Apply 20mV peak to peak sinusoidal input from function generator, measure output voltage)

V_I	Vgs	Vo
10mV		
50mV		
100mV		

3. Determine voltage gain (for any 2 observations)

4. Draw input and output voltage waveform

Results:

The gain of the common gate amplifier with load is: ________________

The gain of the common gate amplifier without load is: _______________

The phase shift between input and output signal of common gate amplifier is ____________

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Laboratory Session No. ___________ Date: ____________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

LAB SESSION 12

Objective:
To illustrate the operation of Simple MOS Mirror

Equipment Required:
• Protoboard

- Protoboard
- Function Generator
- Digital Multimeter
- Power Supply
- Resistors
- Transistors: 1 x 2N7000
- Capacitors

Theory:
Focus initially on N-MOS transistor Q1 which is connected in the so-called "diode connection." That is, the drain and gate are shorted together so that the drain node is at the same potential as the gate. Hence, the drain-to-source voltage is equal to the gate-to-source voltage (i.e., VDS = VGS). From the theory of the MOSFET, we know that VGS must exceed the threshold voltage Vt of the FET for drain current to flow. The characteristic curve for the "diode connection" is shown below. [Reference: Figure 5.14 on page 268 of Sedra & Smith.]

The goal for a current mirror is to establish a stable Iref value and then to mirror (or replicate) current Iref in other branches of the circuit. In other words, we want I0 to equal Iref regardless of the applied value of VDS of the mirroring transistor. This assumes identical transistor geometries of course. What causes a current mirror to deviate from Iref = I0? An error or deviation can result from (1) the mirroring transistor's finite output drain-to-source resistance r0, (2) a parametric mismatch between transistors Q1 and Q2, and (3) a temperature difference between transistors Q1 and Q2. In integrated circuits the transistors are physically close together for thermal matching and they are fabricated simultaneously on the same wafer. So, they should be well matched and thermally coupled as well as physically possible.

Let us analyze how a finite output resistance causes I_0 to deviate from I_{ref}. To do this we write the equations for the drain currents of transistors Q_1 & Q_2. These equations are

Select Value of Resistor R_{ref}:
To set the value of resistor R_{ref} requires knowing the reference current I_{ref} – for our experiment we choose 3 mA. Thus, R_{ref} can be determined from 3 mA (R_{ref}) = $V_{DD} – V_{GS}$. Let V_{GS}=2V. Thus, you will want to compensate for this in adjusting the reference current to 3mA (assume we want to set it to better than a 2% error from the 3 mA target value). Figure 1 shows MOS Mirror implementation for practical analysis.

For the range of load resistances provided measure the new I_o in each case.

Circuit Diagram:

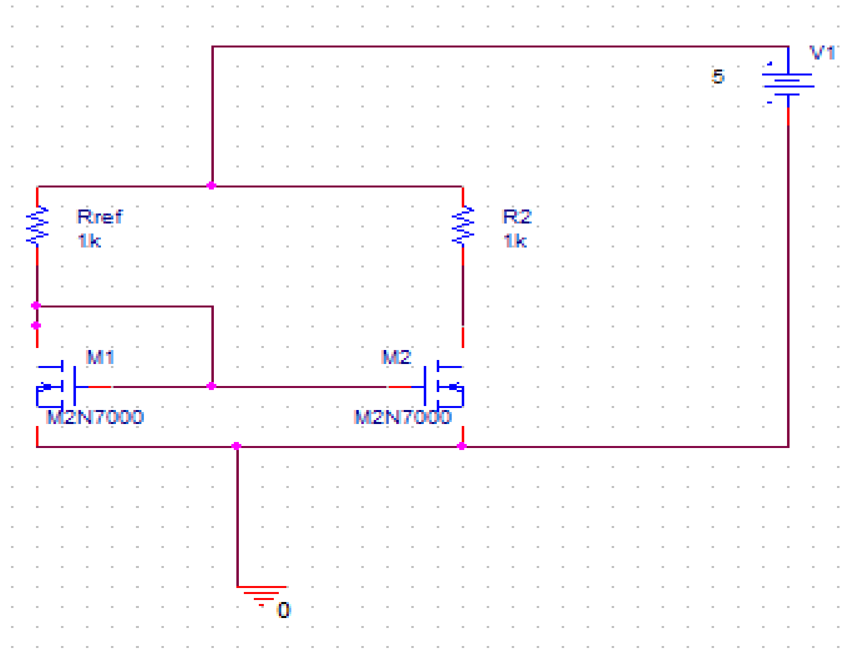

Figure 1: Simple MOS Mirror

Procedure:

- Implement the circuit in figure 2 for Simple MOS Mirror.
- Vary R_{ref} & observe readings for I_{ref} & I_o.

S.No	Rref	Iref	Io
1			
2			
3			
4			
5			

- Vary R2 and observe readings for Iref & Io.

S.No	R2	Iref	Io	VGS2	VDS2	Mode of transistor
1						
2						
3						
4						
5						

Calculations:

Make calculation of Io for the observed value of Iref. Also calculate the percentage error.

Result:

F/OBEM 01/05/00

NED University of Engineering & Technology
Department of ____**ELECTRONIC**__ Engineering
Course Code and Title: ____**EL-236 ELECTRONIC DEVICES & CIRCUITS**____

Psychomotor Domain Assessment Rubric-Level P3					
Skill Sets	Extent of Achievement				
	0	1	2	3	4
Equipment Identification Sensory skill to ***identify*** equipment and/or its component for a lab work.	Not able to identify the equipment.	--	--	--	Able to identify equipment as well as its components.
Equipment Use Sensory skills to ***demonstrate*** the use of the equipment for the lab work.	Doesn't demonstrate the use of equipment.	Slightly demonstrates the use of equipment.	Somewhat demonstrates the use of equipment.	Moderately demon strates the use of equipment.	Fully demonstrates the use of equipment.
Procedural Skills ***Displays*** skills to act upon sequence of steps in lab work.	Not able to either learn or perform lab work procedure.	Able to slightly understand lab work procedure and perform lab work.	Able to somewhat understand lab work procedure and perform lab work.	Able to moderately understand lab work procedure and perform lab work.	Able to fully understand lab work procedure and perform lab work.
Response Ability to ***imitate*** the lab work on his/her own.	Not able to imitate the lab work.	Able to slightly imitate the lab work.	Able to somewhat imitate the lab work.	Able to moderately imitate the lab work.	Able to fully imitate the lab work.
Observation's Use ***Displays*** skills to use the observations from lab work for experimental verifications and illustrations.	Not able to use the observations from lab work for experimental verifications and illustrations.	Slightly able to use the observations from lab work for experimental verifications and illustrations.	Somewhat able to use the observations from lab work for experimental verifications and illustrations.	Moderately able to use the observations from lab work for experimental verifications and illustrations.	Fully able to use the observations from lab work for experimental verifications and illustrations.
Safety Adherence Adherence to ***safety*** procedures.	Doesn't adhere to safety procedures.	Slightly adheres to safety procedures.	Somewhat adheres to safety procedures.	Moderately adheres to safety procedures.	Fully adheres to safety procedures.
Equipment Handling ***Equipment care*** during the use.	Doesn't handle equipment with required care.	Rarely handles equipment with required care.	Occasionally handles equipment with required care.	Often handles equipment with required care.	Handles equipment with required care.
Group Work ***Contributes*** in a group based lab work.	Doesn't participate and contribute.	Slightly participates and contributes.	Somewhat participates and contributes.	Moderately participates and contributes.	Fully participates and contributes.

Laboratory Session No. ___________ Date: _____________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	

OPEN-ENDED LAB

Design cascaded amplifier circuits (BJT or MOSFET or combination of both), with any choice of combination.
Few suggested configurations are:

CE-CE, CS-CG

Each student must submit simulations and hardware work, with observations noted with cascaded configuration. These observations must reflect theoretical knowledge. All hardware and software observations are to be presented in a report

Total Marks (10)
Marks Distribution for OEL:

Simulations: 3 Marks
Hardware: 5 Marks
Report : 2 Marks

F/OBEM 01/05/00

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	0	1	2	3	4
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Equipment Use Sensory skills to ***demonstrate*** the use of the equipment for the lab work.	Doesn't demonstrate the use of equipment.	Slightly demonstrates the use of equipment.	Somewhat demonstrates the use of equipment.	Moderately demon strates the use of equipment.	Fully demonstrates the use of equipment.
Procedural Skills ***Displays*** skills to act upon sequence of steps in lab work.	Not able to either learn or perform lab work procedure.	Able to slightly understand lab work procedure and perform lab work.	Able to somewhat understand lab work procedure and perform lab work.	Able to moderately understand lab work procedure and perform lab work.	Able to fully understand lab work procedure and perform lab work.
Response Ability to ***imitate*** the lab work on his/her own.	Not able to imitate the lab work.	Able to slightly imitate the lab work.	Able to somewhat imitate the lab work.	Able to moderately imitate the lab work.	Able to fully imitate the lab work.
Observation's Use ***Displays*** skills to use the observations from lab work for experimental verifications and illustrations.	Not able to use the observations from lab work for experimental verifications and illustrations.	Slightly able to use the observations from lab work for experimental verifications and illustrations.	Somewhat able to use the observations from lab work for experimental verifications and illustrations.	Moderately able to use the observations from lab work for experimental verifications and illustrations.	Fully able to use the observations from lab work for experimental verifications and illustrations.
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Laboratory Session No. ___________ Date: ____________________

Weighted CLO (Psychomotor Score)	
Remarks	
Instructor's Signature with Date:	