Zahid Ali Siddiqui
MS-Computer Engineering
BE-Electronic Engineering
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AREA OF INTEREST

Self Aware Systems, Low power digital circuits, Fault Tolerant FPGA Architecture, FPGA based system development, Totally Self-checking systems, Microcontroller and Embedded Systems, Data Encryption, general purpose algorithms' acceleration using GPU.

QUALIFICATION

CHOSUN UNIVERSITY (South Korea), MS Computer Engineering 2011-2013
Completed with 96.22% Marks (CGPA: 4.33/4.5)

NED University of Eng. & Tech. (Karachi), BE Electronics 2006-2009
Completed with 81% Marks (CGPA: 3.7/4.0)

Adamjee Govt. Science College (Karachi), FSc Pre-Engineering 2003-2005
Completed with 82.5% Marks

PIA Model Secondary School (Karachi), Matric Science Group 2002-2003
Completed with 86% Marks

PROFESSIONAL EXPERIENCE

Research Assistant @ Computer Sys Lab (Chosun University, S. Korea) **2011-2013**
Worked on Fault Tolerant FPGA architecture, Self-checking ALU design, Error Detecting Codes, Viterbi CODEC on FPGA and GPU, PSK signal correlation, AES Encryption-Decryption, entropy encoding for JPEG compression

Enarex Inc. (South Korea) **Total 6 months during 2011-2013**
Worked as internee. Did programming on AVR microcontroller for control circuitries of boiler, washing machine and air conditioner

NED University of Eng. & Tech, (Karachi) **(April 2010-Present)**
Lecturer in the department of Electronic Engineering

PAFKIET University of Eng. & Tech, (Karachi) **(September 2013-Present)**
FPGA developer for ICT R&D funded project on FACE Recognition

TUSDEC (Karachi) **(2010-2012)**
FPGA course instructor (Part time)

MS RESEARCH & THESIS

Online Error Detection and Reconfiguration of n-bit ALU using Scalable Error Detecting Codes on FPGA

BE FINAL YEAR PROJECT

SOC design of Counting & Sorting System of Steel Sheets using 8052MCU with HMI for Pakistan Steel Mill

MISCELLANEOUS PROJECTS

- FPGA based face recognition using PCA for video surveillance (under progress)
- Modified Berger codes with enhanced detection capability (research based project)
- Online Error Mitigation technique for SRAM based FPGA using Partial Reconfiguration
- Design of AES Encryptor on FPGA
- MOS level Self-checking checker design for SEDC codes
- Viterbi decoder design on GPU & FPGA : Performance Evaluation
- Clicker based student attendance and database management system using FPGA
- Network simulator of CSMA/CA with BEB algorithm
- Line Following Robot using PIC microcontroller
- Robotic Arm using AVR microcontroller

SKILL SET

- Proficient on Xilinx and Altera FPGAs, Nvidia GPU, AVR/ PIC/ 805X Microcontrollers, Siemens PLC
- Worked with Quartus II, Xilinx ISE, Modelsim, Multisim, Proteous, Matlab, Labview and several IDE's
- Circuit Designing Softwares : Cadence, Mentor Graphics, Orcade, Pspice, NI multisim
- Language Set : Verilog, Assembly, CUDA, C, Matlab, Ladder
- Excellent English language skills (IELTS score 7.0)
- Korean Language : Survival level speaking, understanding, reading and writing

AWARDS/HONORS

- Global IT scholarship awarded by NIPA (S. Korea) Sep 2011-Aug 2013
- Secured 2nd position in Paper writing competition SPEC 2009
- Secured 2nd position in Student Project Exhibition & Competition 2007
- Awarded with shield by PIA senior staff association for securing 84% marks in HSC exams 2005
- Awarded with Gold medal for securing 2nd highest mark in SSC exams 2003

CONFERENCE PAPERS

[1] Zahid Ali Siddiqui & Jeong-A Lee, "A Comparative Study of SEDC and Berger coding scheme for designing concurrent error detection in FPGA Look-up Tables," Proc. of KCC 2013, Korea, June 2013.

[2] Zahid Ali Siddiqui, Park Hui Jong & Jeong-A Lee, "Online Error Detection in SRAM based FPGA using Scalable Error Detecting Codes," 5th IEEE Asian Symposium on Quality Electronic Design, pp. 321-324, Aug. 2013.

[3] Zahid Ali Siddiqui, Park Hui Jong & Jeong-A Lee, "Area-Time Efficient Self-checking ALU based on Scalable Error Detection Coding," 16th IEEE Euromicro Digital System Design Conference, pp. 870-877, Sep. 2013.

[4] Zahid A. S., Ahmed. M, S. M. Danish & M. Faizan Shirazi, "Design of low cost embedded system for automation of parallel processing plant," IEEE Int. conf. on *Advanced Mechatronic Systems (ICAMechS)*, pp. 362-366, 11-13 Aug. 2011.

JOURNAL PAPERS

[1] Jeong-A Lee, Zahid Ali Siddiqui, S. Natarajan, Jeong-Gun Lee, "Self-checking Look-up Tables using Scalable Error Detection Coding," in Journal of Semiconductor Technology and Science (**SCI-E**), vol-13, No. 5, pp. 415-422, Oct. 2013.

[2] Zahid Ali Siddiqui, Jeong-A Lee, "Area-Time Efficient Self-checking checker for Scalable Error Detecting Codes," in Integration- The VLSI Journal Elsevier (**SCI-E**), Nov. 2013. **(under review)**

[3] Zahid Ali Siddiqui, Jeong-A Lee, "Strongly Fault Secure n-bit ALU design using SEDC codes on FPGA," in Journal of Microprocessor and Microsystems Elsevier (**SCI-E**), Aug. 2013. **(under review)**

[4] Zahid Ali Siddiqui, Jiun Lee & Jeong-A Lee, "FPGA-GPU comparison for different applications," in Journal of the Chinese Institute of Engineering (**SCI**), Jan. 2014. **(to be submit)**