SONIYA SHAFI
Computer Systems Engineer

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ABOUT ME

Experienced **Computer Systems Engineer** with 3 years of experience in the IC design industry. Demonstrates a blend of strong technical skills, leadership qualities, and excellent communication abilities. Proven expertise in leading cross-functional teams to deliver high-performance integrated circuits while optimizing design workflows for efficiency and scalability. Proficient in Verilog, SystemVerilog, Python, and C++, with a track record of driving innovation and mentoring team members to achieve project success.

EDUCATION

Masters of Engineering

NED University of Engineering and Technology
2023-2025

Bachelors in Computer Systems Engineering

NED University of Engineering and Technology
2018-2022

TECHNICAL SKILLS

- SystemVerilog
- Verilog
- Assembly
- C++
- Python
- RTL design and functional verification
- SystemVerilog testbench architecture
- Python-based verification using cocotb
- Advanced RTL debugging and root-cause analysis
- Coverage model architecture and UCIS-based reporting
- Performance analysis and optimization
- Hardware-software correlation
- In-depth understanding of RISC-V ISA
- Strong expertise in RISC-V Vector Extension

PROFESSIONAL EXPERIENCE

Manager | IC Design & Verification Engineer

XCELERIUM Inc. (USA-based Semiconductor Company)   *2022 – Present*

Leadership & Management Responsibilities

- Managing and mentoring a team of engineers across RTL design, verification, and architecture development
- Technical lead and decision maker for multiple design and verification efforts
- Driving project execution, task prioritization, and technical reviews
- Coordinating with cross-functional and geographically distributed teams

RTL Design & Architecture Development

- Contributed to the design and verification of complex compute architectures
- Designed RTL components with focus on correctness, scalability, and performance
- Participated in architectural definition and refinement of compute subsystems
- Evaluated area and performance trade-offs for different architectural choices

Verification & Debugging

- Designed and maintained SystemVerilog-based verification environments
- Developed cocotb testbenches for Python-driven verification
- Led complex RTL debugging efforts, identifying and resolving functional issues
- Ensured comprehensive verification coverage across architectural corner cases

Functional Coverage

- Designed and implemented functional coverage models using FC4SC
- Defined coverage strategies aligned with architectural intent
- Analyzed coverage results and drove coverage closure
- Integrated coverage reporting into verification workflows

Software Modeling & HW/SW Correlation

- Developed C++ software reference models corresponding to RTL architectures
- Ensured cycle-level and functional alignment between software models and hardware
- Used software models for early validation, performance estimation, and debugging

Algorithm Development & Validation

- Implemented and validated algorithms including:
  - **Fast Fourier Transform (FFT)**
  - **Digital converters**
  - **Digital filtering algorithms**
  - **Matrix Multiplications**
- Verified algorithmic correctness and performance across software and hardware domains

KEY TECHNICAL STRENGTHS

Strong architecture-level understanding beyond block-level design

Expert-level RTL verification and debugging skills

Ability to design scalable verification and coverage infrastructures

Deep understanding of RISC-V vector execution models

Proven leadership and ownership in complex engineering projects